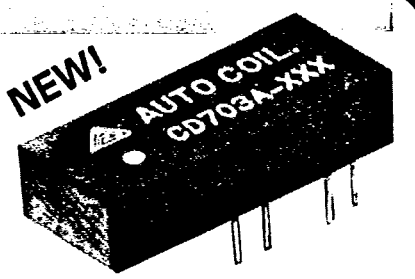
T-47-17

CD703 Series
TTL Digital Programmable Delay Module, 3 BIT

- Programmable in 8 delay steps
- TTL input and output
- Precise and stable delays
- Reliable hybrid construction
- No external components required
- Fan out 10TTL loads
- Operating temperature 0° to 70°C
- Storage temperature -55° to +125°C



16 PIN DIP

Electrical Characteristics:

VIH	(High level input voltage)	2.0 to 5.0V
IIH	(High level input current)	40 μA Max.
VIL	(Low level input voltage)	0.8 V Max.
IIL	(Low level input current)	-0.4 ma Max.
VOH	(High level output voltage)	2.5 V Min.
VOL	(Low level output voltage)	0.5 V Max.
VCC	(Supply voltage)	5.0 V ± 0.25 V DC
ICC	(Supply current)	75 ma Max.

Mechanical Specifications:

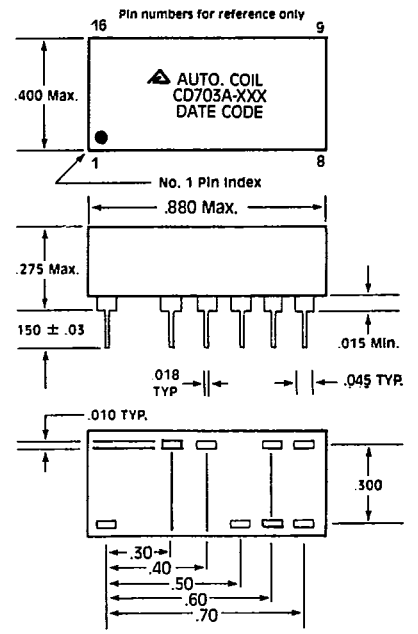
Case: Epoxy filled D.A.P.
Leads: Alloy 42 or equiv.
solder coated
Marking: White expoxy ink

Also Available:

Intermediate delays
Military versions

Specifications subject to change without notice.

All digital delay modules can be operated at conditions other than specified.
Since accuracies may be slightly affected, we suggest that the module be evaluated under specific operating conditions.



Nominal Delays (in NS) ± 1 NS or 5% Whichever is Greater

Automatic Coil Part Number	Incremental Delay/Step	Total Δ T_D	Residual Delay	Total Delay
CD703A-101	0.5	3.5	7.0	10.5
CD703A-102	1.0	7.0	7.0	14.0
CD703A-103	2.0	14.0	7.0	21.0
CD703A-104	3.0	21.0	7.0	28.0
CD703A-105	4.0	28.0	7.0	35.0
CD703A-106	5.0	35.0	7.0	42.0
CD703A-107	10.0	70.0	7.0	77.0
CD703A-108	15.0	105.0	7.0	112.0
CD703A-109	20.0	140.0	7.0	147.0
CD703A-110	40.0	280.0	7.0	287.0
CD703A-111	50.0	350.0	7.0	357.0

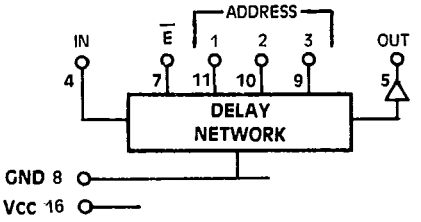
Truth Table

$\overline{\text{Enable}}$	Address (Bit #) 3	2	1	Delay (PIN 5)
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	X	X	X	0

1 = HIGH
0 = LOW
X = DON'T CARE
To = RESIDUAL DELAY

T_1 to T_7 Multiplier of incremental delay

Output rise times (TPLH) 4.0 NS max. (0.75 to 2.4 V level).



Test Conditions:

1) All measurements are made @ 25°C
2) VCC is maintained @ 5.0 VDC
3) All measurements are made with no loads on output
4) Delays are measured @ 1.5V level
5) Delays & tolerances for leading edges only (TPLH) – falling edges (TPHL) closely matched to TPLH

Input Conditions:

1) Pulse amplitude: 3.20V
2) Input rise time: 3.0 NS (10 to 90%)
3) Pulse width: 2 × total delay
4) Duty cycle: < 25%

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