Military Standard Products

UT7M628 Radiation-Hardened 8K x 16 ROM

Preliminary Data Sheet

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

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FEATURES

- ☐ 70ns maximum address access time
- ☐ Asynchronous operation
- ☐ CMOS-compatible output levels
- ☐ Three-state data bus
- ☐ Low operating and standby current
- ☐ User-defined chip select, byte select, and output enable polarity
- ☐ Full military operating temperature range, -55°C to +125°C, screened to specific test methods listed in Table I MIL-STD-883 Method 5004 for Level S or Level B
- ☐ Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 1.0E6 rads(Si)
  - Dose rate upset: 1.0E9 rads(Si)/sec
  - Dose rate survival: 1.0E-12 rads(Si)/sec
- ☐ Latchup immune
- ☐ Packaging options:
  - 40-pin 100-mil center DIP (.610 x 2.0)
- ☐ 5-volt operation
- ☐ High-density 128K-bit CMOS ROM utilizing UTMC's high performance 64K-bit ROM
- ☐ Organized 8K x 16, separate control of upper byte (Q15 through Q8) and lower byte (Q7 through Q0)
- ☐ Post-radiation AC/DC performance characteristics guaranteed to MIL-STD-883 Method 1019 testing

INTRODUCTION

The UT7M628 ROM is a high performance, asynchronous, radiation-hardened, 8K x 16 memory device. The UT7M628 features fully static operation requiring no external clocks or timing strobes.

Comprised of two 8K x 8 ROMs, the system designer has the flexibility to access either the upper byte or lower byte of any word. The maximum access time is 70ns over the full military temperature range.

Advanced CMOS processing along with a device select/de-select function result in a high performance, power saving SRAM. Inputs UB, LB, and CS control this unique feature, negation of UB or LB disables all or segements of the 128K-bit memory. Negation of CS deselects the entire 128K-bit memory. The combination of radiation-hardness, fast access time, and low power consumption make the UT7M628 ideal for high-speed systems designed for operation in radiation environments.

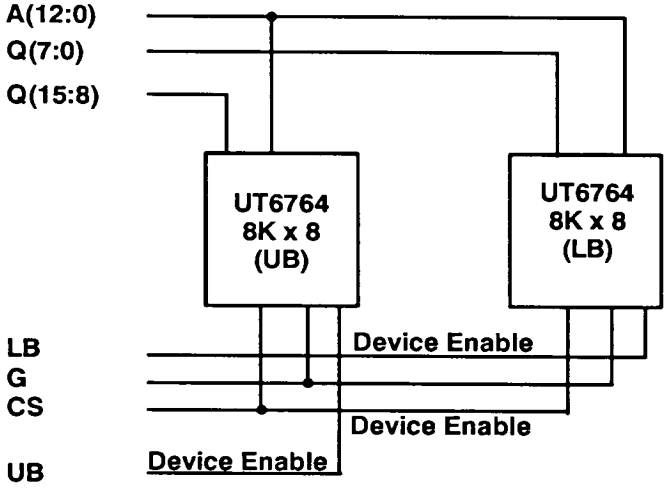


Figure 1. ROM Block Diagram

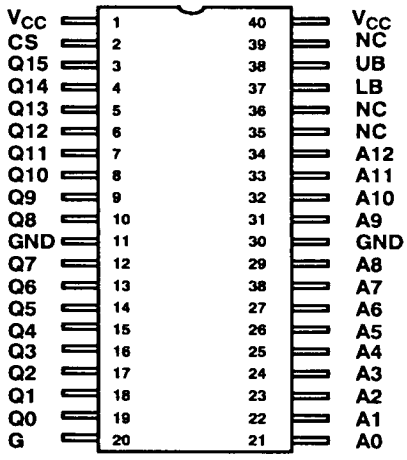


Figure 2. ROM Pinout

PIN NAMES

A(12:0)	Address [1]	G	Output Enable [2]
Q(15:0)	Data Output	V_{DD}	Power
LB	Byte Select	V_{SS}	Ground
UB	Byte Select	CS	Chip Select

Notes:
1. A12 most significant bit; A0 least significant bit.
2. The polarity of the chip select, byte select, and output enable is user-defined.

DEVICE OPERATION

The UT7M628 has four control inputs called Upper Byte (UB), Lower Byte (LB), Chip Select (CS), and Output Enable (G); thirteen address input, A(12:0); and sixteen data lines, Q(15:0). Inputs LB and UB in conjunction with CS control the selection of the 8K x 8 memory blocks. For byte wide systems (i.e., x 8) inputs LB and UB function as high order address bits. Systems implementing word organization (i.e., x 16) use inputs LB and HB as device selects along with CS. Input CS is a global device select that requires assertion to gain access (read) to the ROM. During a read cycle, assert G to enable the outputs. Asserting CS and either or both UB or LB selects the device, resulting in a rise of I_{DD} to its active value, and the decode of address input A(12:0) to select one of 8,192 memory locations. Please note that LB and UB function as device selects, negation of both these inputs disables the entire ROM.

Table 1. Device Operation Truth Table

$\overline{G}$	CS	UB	LB	I/O Mode	Mode
X [1]	negated	X	X	3-state	Stand-by
X	X	negated	negated	3-state	Stand-by
negated	asserted	X	X	3-state	Read [2]
asserted	asserted	X	X	Data out	Read [3]

Notes:
1. "X" is defined as a "don't care."
2. Device active; outputs disabled. If UB=LB then I/O Mode is 3-state and Mode is stand-by.
3. Read mode. If UB=LB then I/O Mode is 3-state and Mode is stand-by.

READ CYCLE

A combination of UB and/or LB, CS, and G asserted defines a read cycle. Read access time is measured from the latter assertion of device select, byte select (UB and/or LB), Output Enable, or valid address to valid data output.

Read Cycle 1, the Address Access read in figure 3a, is initiated by a change in address inputs while the device is selected and G asserted. Valid eight or sixteen-bit data appears on data outputs after the specific t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device selects and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

Figure 3b shows Read Cycle 2, the Device Select-controlled Access. For this cycle, G remains asserted, and the address bus remains stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight or sixteen-bit word addressed by A(12:0) is accessed and appears at the data outputs.

Figure 3c shows Read Cycle 3, the Output Enable-controlled Access. For this cycle assert CS and either or both UB and LB, address inputs are stable before G is enabled. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

CHIP SELECT

User-defined chip select, upper and lower byte select, and output enable polarity provides a flexible system interface. Input polarity (i.e., active high vs. active low) is mask defined. Possible combinations include ($\overline{G}$, $\overline{LB}$, $\overline{UB}$, $\overline{CS}$), ($\overline{G}$, $\overline{LB}$, $\overline{UB}$, CS), ($\overline{G}$, $\overline{LB}$, UB, $\overline{CS}$), ($\overline{G}$, $\overline{LB}$, UB, CS), ($\overline{G}$, LB, UB, $\overline{CS}$), ($\overline{G}$, LB, $\overline{UB}$, CS), ($\overline{G}$, LB, UB, $\overline{CS}$), ($\overline{G}$, LB, UB, CS), (G, $\overline{LB}$, $\overline{UB}$, $\overline{CS}$), (G, $\overline{LB}$, $\overline{UB}$, CS), (G, $\overline{LB}$, UB, $\overline{CS}$), (G, $\overline{LB}$, UB, CS), (G, LB, $\overline{UB}$, $\overline{CS}$), (G, LB, $\overline{UB}$, CS), (G, LB, UB, $\overline{CS}$), (G, LB, UB, CS).

RADIATION HARDNESS

The UT7M628 ROM incorporates two UTMC 8K x 8 ROMs designed for operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

Table 2. Radiation Hardness Design Specifications [1]

Total Dose	1.0E6	rads(Si)
Dose Rate Upset	1.0E9	rads(Si)/s 20ns pulse
Dose Rate Survival	1.0E12	rads(Si)/s 20ns pulse
Neutron Fluence	3.0E14	n/cm^2

Notes:
1. The ROM will not latchup during radiation exposure under recommended operating conditions.

ABSOLUTE MAXIMUM RATINGS [1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.5 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.5V to V_{DD} + 0.5
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	2W
T_J	Maximum junction temperature	+150°C
Θ_{JC}	Thermal resistance, junction-to-case	10°C/W
I_{LU}	Latchup immunity	± 150 mA
I_I	DC input current	± 10 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	4.5 to 5.5V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*
(V_{DD} = 5.0V ± 10%; -55°C < Tc < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2.2		V
V_{IL}	Low-level input voltage			0.8	V
V_{OL}	Low-level output voltage	I_{OL} = 8mA, V_{DD} = 4.5V		0.4	V
V_{OH}	High-level output voltage	I_{OH} = -8mA, V_{DD} = 4.5V	2.4		V
C_{IN} [1]	Input capacitance	f = 1MHz @ 0V, V_{DD} = 4.5V		30	pF
C_O [1]	Output capacitance	f = 1MHz @ 0V, V_{DD} = 4.5V		40	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}	-20	20	µA
I_{OZ}	Three-state output leakage current TTL outputs	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V $\overline{G}$ = 5.5V	-10	10	µA
I_{OS} [2,3]	Short-circuit output current	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	 -90	90	mA mA
I_{DD}(OP)	Supply current operating @ f = 1MHz (x16) @ f = 14MHz (x16)	CMOS inputs (i.e., I_{OUT} = 0) V_{DD} = 5.5V V_{DD} = 5.5V		 80 300	 mA mA
I_{DD}(SB) **pre-rad** **post-rad**	Supply current standby @ f = 0Hz	CMOS inputs (i.e., I_{OUT} = 0) CS = negated V_{DD} = 5.5V or UB and LB negated		 400 6	 µA mA

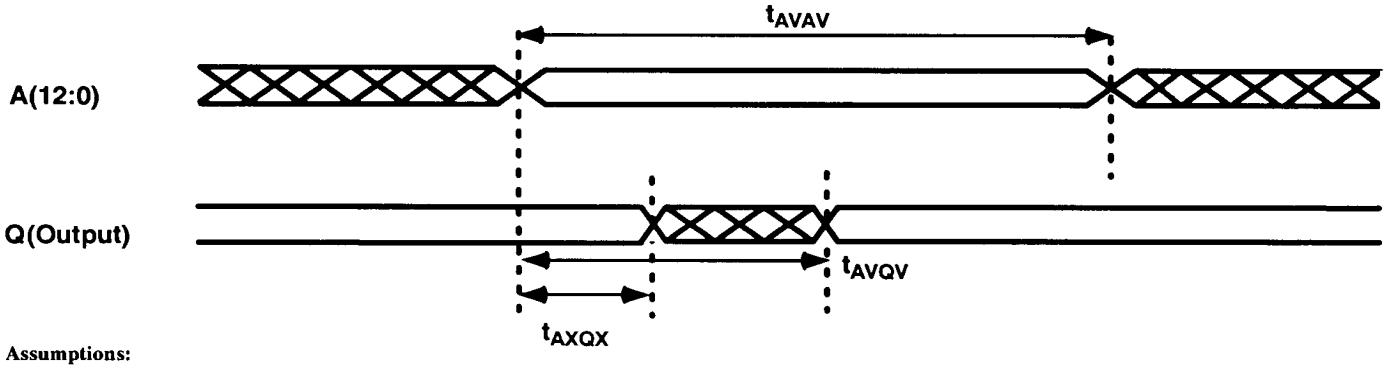
Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).
1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

AC CHARACTERISTICS READ CYCLE (Pre/Post-Radiation)*
(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AVAV}	Read cycle time	70		ns
t_{AVQV}	Read access time		70	ns
t_{AXQX}	Output hold time	5		ns
t_{GTQX}	G-controlled output enable time	0		ns
t_{GTQV}	G-controlled output enable time (Read Cycle 3)		15	ns
t_{GFQZ}	G-controlled output three-state time		15	ns
t_{STQX} [1]	Chip Select-controlled output enable time	0		ns
t_{STQV} [2]	Chip Select-controlled access time		70	ns
t_{SFQZ} [2]	Chip Select-controlled output three-state time		20	ns

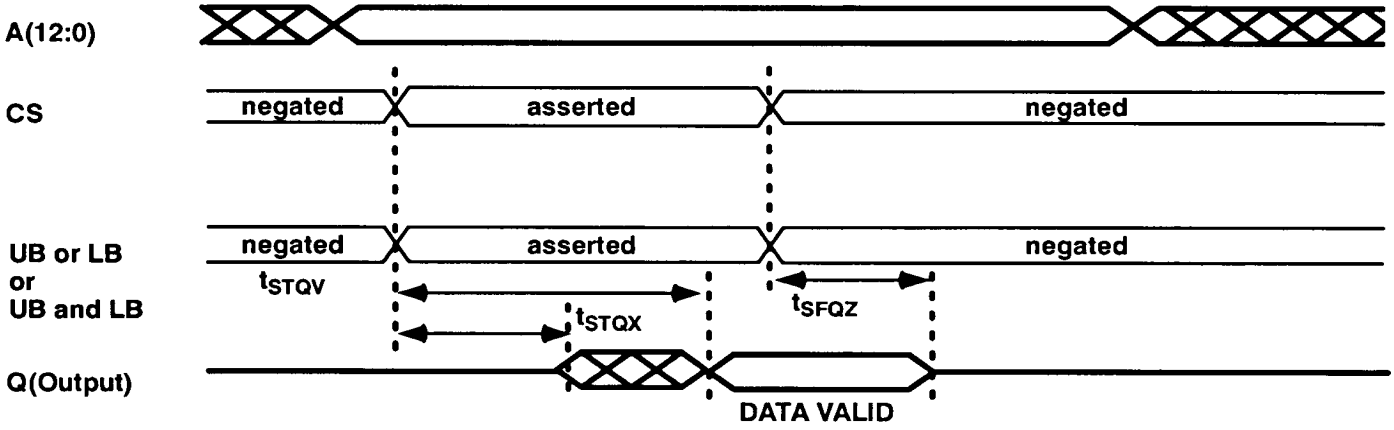
Notes:
* Post-radiation performance guaranteed at 25°C to meet MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

1. The ST (select true) notation refers to the rising edge of CS, UB, or LB, whichever comes last.
2. The SF (select false) notation refers to the negating edge of CS and UB or LB, whichever comes first.



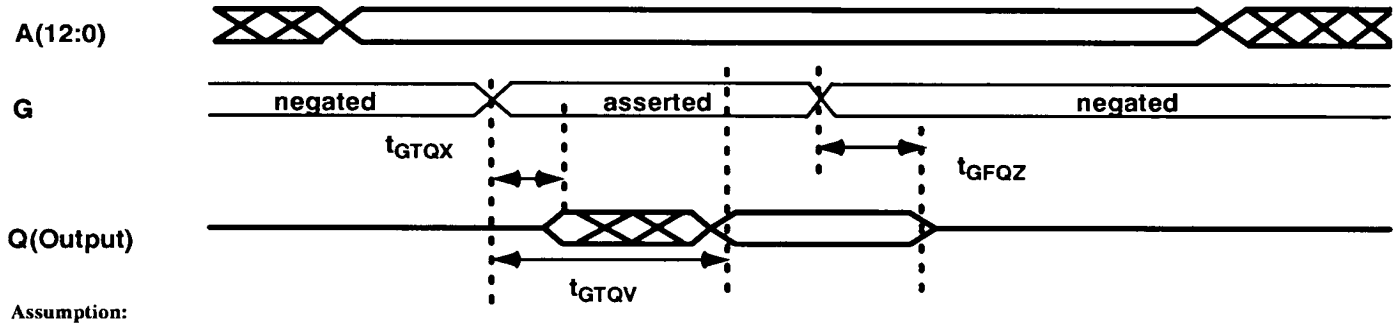
Assumptions:
1. G asserted.
2. CS and UB and LB asserted, or CS and UB or LB asserted.

Figure 3a. ROM Read Cycle 1: Address Access



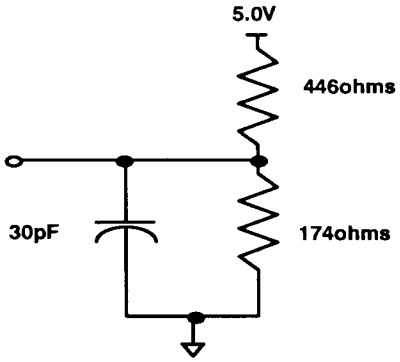
Assumption:
1. G asserted.

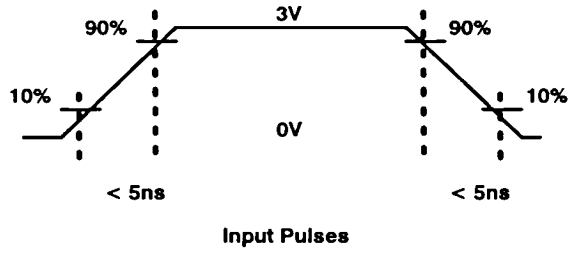
Figure 3b. ROM Read Cycle 2: Chip Select Access



Assumption:
1. CS and UB and Lb asserted, or CS and UB or LB asserted.

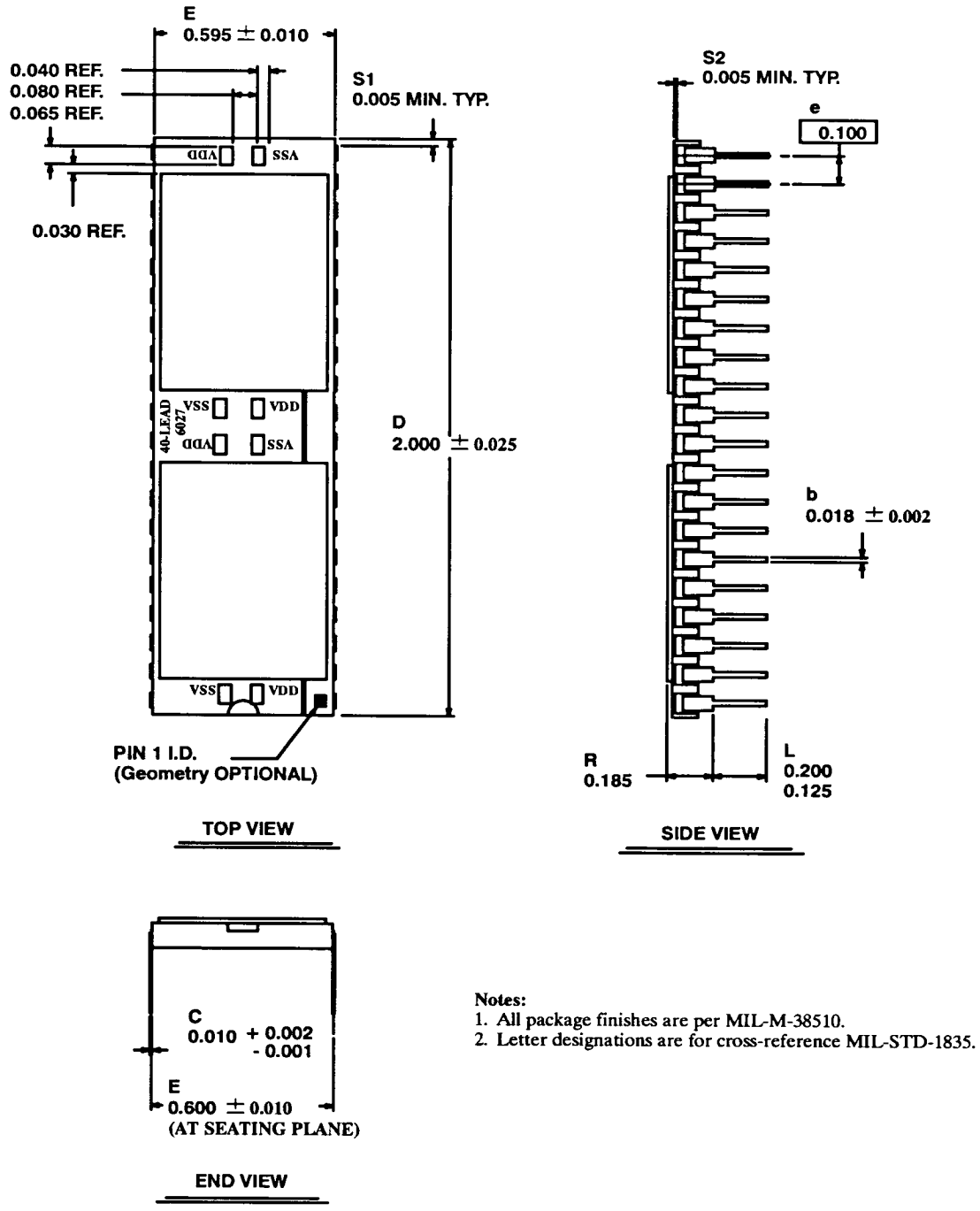
Figure 3c. ROM Read Cycle 3: Output Enable Access





Notes:
1. 40pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point. (i.e., 1.4V)
3. Or equivalent output load circuit.

Figure 4. AC Test Loads and Input Waveforms



Notes:
1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference MIL-STD-1835.

Figure 5. 40-pin Side-Brazed DIP

ORDERING INFORMATION

To order the UT7M628 ROM, use the following part number guide:

UT7M628-70 * * *

- (R) Radiation-Hardened 1.0E5 rads(Si)
- (H) Radiation-Hardened 1.0E6 rads(Si)
- (B) MIL-STD-883 compliant
- (C) Modified high-reliability flow, -55°C to 125°C
- (P) Prototype
  (radiation performance not guaranteed)
- (S) Screened to MIL-STD-883C Level S requirements per
  Method 5004 and Group A only of Method 5005
- (P) 40-pin Ceramic Side-Brazed DIP
  CDIP2-T40, MIL-STD-1835

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