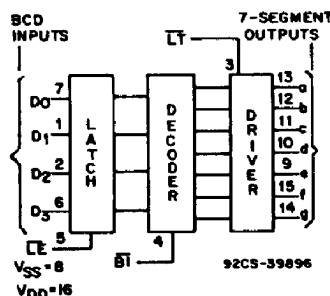
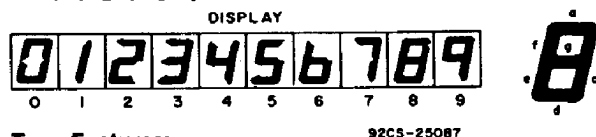


High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

BCD-to-7 Segment Latch/ Decoder/Drivers



Type Features:

- High-output sourcing capability—7.5 mA @ 4.5 V, 10 mA @ 6 V (HC4511)
- Input latches for BCD code storage
- Lamp test and blanking capability

The RCA CD54/74HC4511 and CD54/74HCT4511 are BCD-to-7 segment latch/decoder/drivers having four address inputs (D₀-D₃), active "Low" blanking and lamp test inputs, and a latch enable input which, when "High", enables the latches to store the BCD inputs. When Latch Enable is "Low", the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

The CD54HC/HCT4511 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4511 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

LE	BI	L ^T	D ₃	D ₂	D ₁	D ₀	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	X	L	H	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	L	H	L	L	L	H	L	H	H	L	L	L	L	1
L	L	H	L	L	H	L	H	H	L	H	L	H	H	2
L	L	H	H	L	L	H	H	H	H	L	L	H	H	3
L	L	H	H	L	H	L	L	L	H	L	L	H	H	4
L	L	H	H	L	H	L	H	L	H	H	L	H	H	5
L	L	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	L	H	H	L	L	L	H	H	H	L	L	H	H	9
L	L	H	H	L	L	H	L	L	L	L	L	L	L	Blank
L	L	H	H	L	L	H	L	L	L	L	L	L	L	Blank
L	L	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	L	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	L	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	-	-	-	-	-	-	-	.

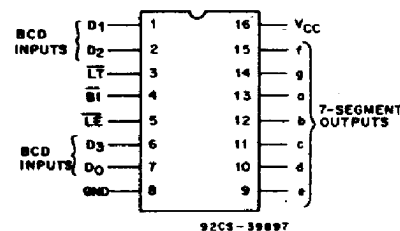
X = Don't Care

*Depends on BCD code previously applied when $\overline{LE} = L$

Note: Display is blank for all illegal input codes (BCD > HLLH)

Family Features:

- Fanout (over temperature range):
Standard outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- Wide operating temperature range:
CD74HC/HCT: -40 to $+85^{\circ}\text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC types:
2 to 6 V operation
High noise immunity:
 $N_{IL}=30\%$, $N_{IH}=30\%$ of V_{CC} ; @ $V_{CC}=5\text{ V}$
- CD54HCT/CD74HCT types:
4.5 to 5.5 V operation
Direct LSTTL input logic compatibility
 $V_{IL}=0.8\text{ V max.}$, $V_{IH}=2\text{ V min.}$
CMOS input compatibility
 $I_1 \leq 1\text{ }\mu\text{A}$ @ V_{OL} , V_{OH}



TERMINAL ASSIGNMENT

This data sheet is applicable to the CD54HC4511 and CD74HCT4511. The CD54HCT4511 was not acquired from Harris Semiconductor.
See SCHS214 for information on the CD74HCT4511.

CD54/74HC4511 CD54/74HCT4511

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	 -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	 ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	 ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	 ± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	 ± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	 500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	 Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F,H)	 500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F,H)	 Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	 400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	 Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F,H	 -55 to $+125^\circ\text{C}$
PACKAGE TYPE E,M	 -40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	 -65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	 $+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)	
with solder contacting lead tips only	 $+300^\circ\text{C}$

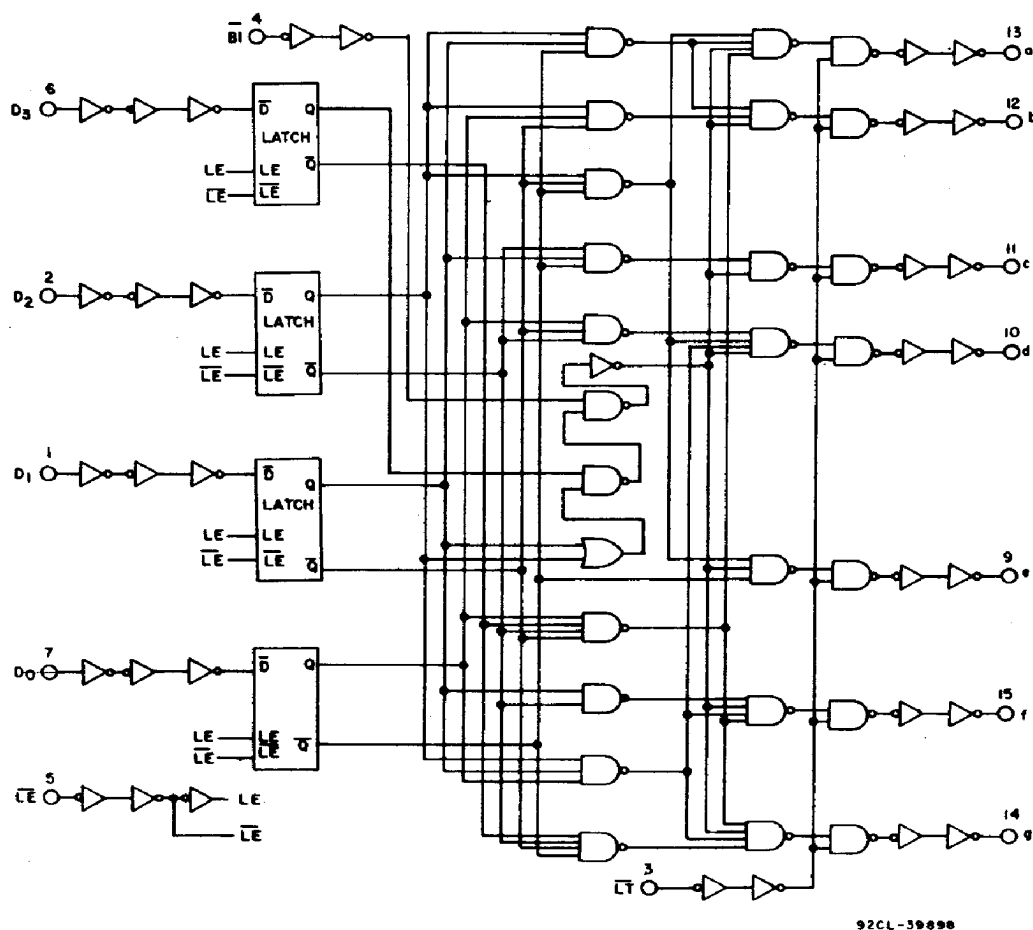


Fig. 1 - Logic diagram.

CD54/74HC4511

CD54/74HCT4511

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4511/CD54HC4511										CD74HCT4511/CD54HCT4511										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V _i V	I _o mA	V _{cc} V	+25° C			-40/ +85° C		-55/ +125° C		V _i V	V _{cc} V	+25° C			-40/ +85° C		-55/ +125° C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—										
			6	—	—	1.8	—	1.8	—	1.8	—										
High-Level Output Voltage V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V	
CMOS Loads			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V _{IL}										V _{IL}										
Non-Standard Output	or V _{IH}	-7.5	4.5	3.98	—	—	3.84	—	3.7	—	or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V	
		-10	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V	
CMOS Loads			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V _{IL}										V _{IL}										
Standard Output	or V _{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V	
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I _i	V _{cc} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{cc} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current I _{cc}	V _{cc} or Gnd	0	6	—	—	8	—	80	—	160	V _{cc} or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{cc} *											V _{cc} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA	

*For dual-supply systems theoretical worst case ($V_i = 2.4$ V, $V_{cc} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{LT}$, LE	1.5
$\overline{BI}$, Dn	0.3

*Unit Load is ΔI_{cc} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4511

CD54/74HCT4511

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V_i , V_o	0	V_{CC}	V
Operating Temperature, T_A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r , t_f :			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS ($V_{CC}=5$ V, $T_A=25^\circ$ C, Input t_r , $t_f=6$ ns)

CHARACTERISTIC	C_L (pF)	TYPICAL VALUES		UNITS
		HC	HCT	
Propagation Delay:				
D_n to Output	15	25	25	ns
$\overline{LE}$ to Output	15	23	23	
$\overline{BI}$ to Output	15	18	18	
$\overline{LT}$ to Output	15	13	13	
Power Dissipation Capacitance*	C_{PD}	114	110	pF

* C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$ where f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

PRE-REQUISITE FOR SWITCHING FUNCTION

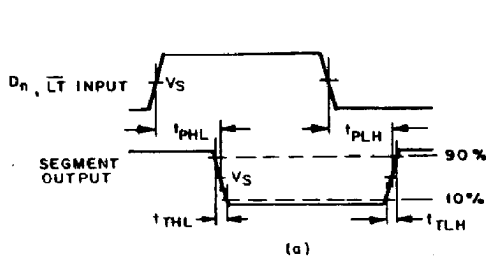
CHARACTERISTIC	TEST CONDITIONS V _{CC} (V)	LIMITS												UNITS	
		25°C				-40°C to +85°C				-55°C to +125°C					
		HC		HCT		74HC		74HCT		54HC		54HCT			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Setup Time, D _n to L $\overline{E}$	t _{SU}	2	80	—	—	—	100	—	—	—	120	—	—	ns	
		4.5	16	—	16	—	20	—	20	—	24	—	24		—
		6	14	—	—	—	17	—	—	—	20	—	—		—
Hold Time, D _n to L $\overline{E}$	t _H	2	3	—	—	—	3	—	—	—	3	—	—	ns	
		4.5	3	—	5	—	3	—	5	—	3	—	5		—
		6	3	—	—	—	3	—	—	—	3	—	—		—
Latch Enable Pulse Width,	t _W	2	80	—	—	—	100	—	—	—	120	—	—	MHz	
		4.5	16	—	16	—	20	—	20	—	24	—	24		—
		6	14	—	—	—	17	—	—	—	20	—	—		—

CD54/74HC4511

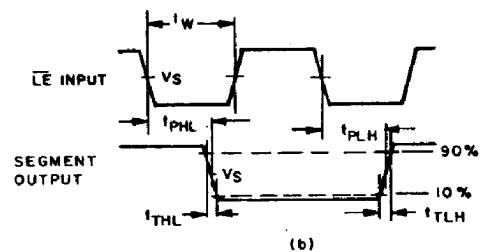
CD54/74HCT4511

SWITCHING CHARACTERISTICS ($C_L=50$ pF, Input $t_i=6$ ns)

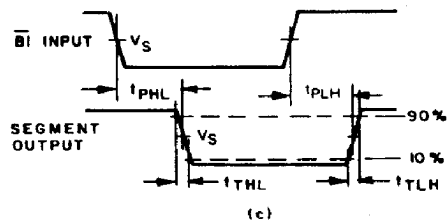
CHARACTERISTIC		V _{CC}	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, D _n to Output	t _{PLH}	2	—	300	—	—	—	375	—	—	—	450	—	—	ns
	t _{PHL}	4.5	—	60	—	60	—	75	—	75	—	90	—	90	
		6	—	51	—	—	—	64	—	—	—	77	—	—	
LE to Output	t _{PLH}	2	—	270	—	—	—	340	—	—	—	405	—	—	ns
	t _{PHL}	4.5	—	54	—	54	—	68	—	68	—	81	—	81	
		6	—	46	—	—	—	58	—	—	—	69	—	—	
BI to Output	t _{PLH}	2	—	220	—	—	—	275	—	—	—	330	—	—	ns
	t _{PHL}	4.5	—	44	—	44	—	55	—	55	—	66	—	66	
		6	—	37	—	—	—	47	—	—	—	56	—	—	
LT to Output	t _{PLH}	2	—	160	—	—	—	200	—	—	—	240	—	—	ns
	t _{PHL}	4.5	—	32	—	33	—	40	—	41	—	48	—	50	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
Transition Time	t _{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t _{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C _i		—	10	—	10	—	10	—	10	—	10	—	10	pF



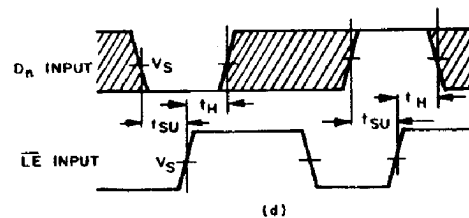
Input (D_n , $\overline{LT}$) to output propagation delays and output transition times



Input ($\overline{LE}$) to output propagation delays and latch enable pulse width



Input ($\overline{BI}$) to output propagation delays.



Note

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveforms showing the data set-up and hold times for D_n input to $\overline{LE}$ input.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

Fig. 2 - AC waveforms.

92CM-39899