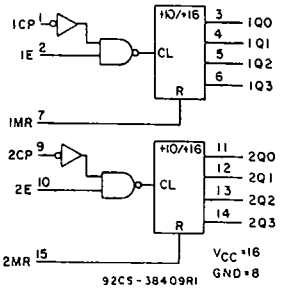
T-45-23-05

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

File Number 1665

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual Synchronous Counters

CD54/74HC/HCT4518 — BCD
CD54/74HC/HCT4520 — Binary

Type Features:

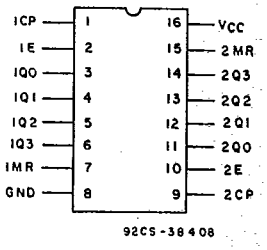
- *Positive or Negative Edge Triggering*
- *Synchronous Internal Carry Propagation*

The RCA CD54/74HC4518 and CD54/74HCT4518 are dual BCD up-counters. The RCA CD54/74HC4520 and CD54/74HCT4520 are dual binary up-counters. Each device consists of two independent internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or the negative-going transition of CLOCK. The counters are cleared by high levels on the MASTER RESET lines. The counter can be cascaded in the ripple mode by connecting Q3 to the ENABLE input of the subsequent counter while the CLOCK input of the latter is held low.

The CD54HC/HCT4518 and CD54HC/HCT4520 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT4518 and CD74HC/HCT4520 are supplied in a 16-lead plastic dual-in-line packages (E suffix), and in 16-lead surface mount plastic dual-in-line packages (M suffix). The CD54/74HC/HCT4518/4520 are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

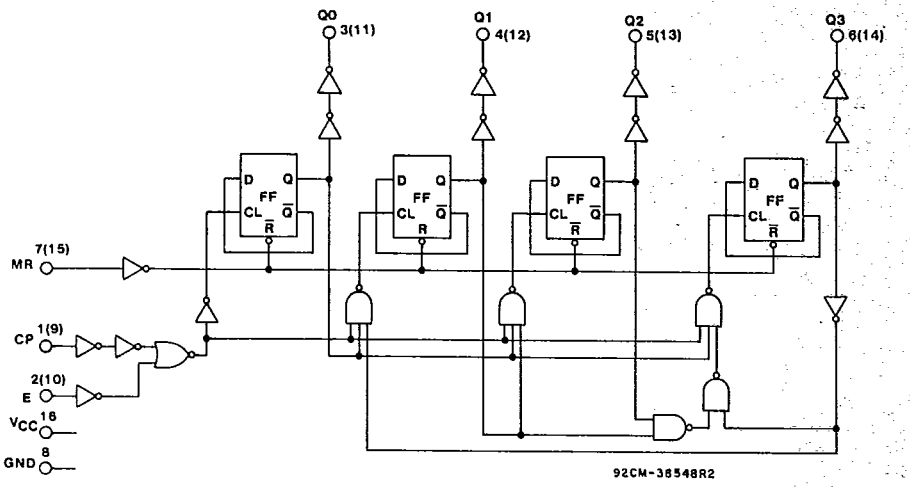


Fig. 1 — CD54/74HC/HCT4518 Logic Diagram

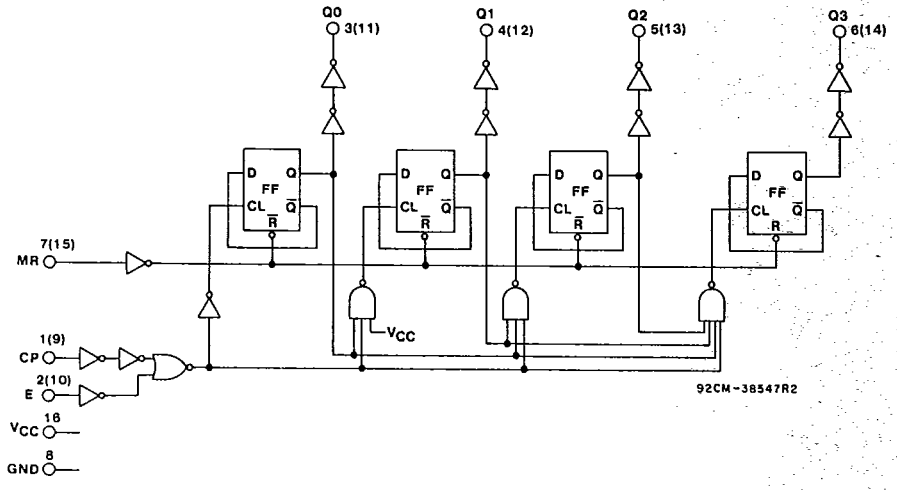


Fig. 2 — CD54/74HC/HCT4520 Logic Diagram

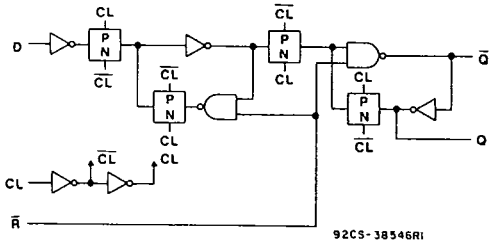


Fig. 3 - Detail of each D Flip-Flop

TRUTH TABLE			
CP	E	MR	ACTION
↗	H	L	Increment Counter
L	↘	L	Increment Counter
↘	X	L	No Change
X	↗	L	No Change
↗	L	L	No Change
H	↘	L	No Change
X	X	H	Q0 thru Q3 = L

X = Don't Care H = High State L = Low State

↗ = low-to-high transition

↘ = high-to-low transition

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} + 0.5V$) ..... ±25mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}) ..... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4518/CD54HC4518 CD74HC4520/CD54HC4520										CD74HCT4518/CD54HCT4518 CD74HCT4520/CD54HCT4520								UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES		TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES	
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
MR	1.2
CP	0.25
ENABLE	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL HC	TYPICAL HCT	UNITS
Maximum Clock Frequency	15	f_{MAX}	60	50	MHz
Propagation Delay CP to Qn	15	t_{PLH} t_{PHL}	20	22	ns
Enable to Qn	15	t_{PLH} t_{PHL}	20	23	ns
MR to Qn	15	t_{PLH} t_{PHL}	12	14	ns
Power Dissipation Capacitance*	—	C_{PD}	33	33	pF

*C_{PD} is used to determine the dynamic power consumption, per counter.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where
f_i = input frequency,
f_o = output frequency,
C_L = output load capacitance
V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	SYMBOL	V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	24	—	20	—	20	—	17	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	
Clock Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
MR Pulse Width	t_W	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
		4.5	20	—	20	—	25	—	25	—	30	—	30	—	
		6	17	—	—	—	21	—	—	—	26	—	—	—	
Setup Time Enable to CP	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Removal Time MR to CP	t_{REM}	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	
Setup Time CP to Enable	t_{SU}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Removal Time MR to Enable	t_{REM}	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
		4.5	0	—	0	—	0	—	0	—	0	—	0	—	
		6	0	—	—	—	0	—	—	—	0	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay, CP to Qn	t_{PLH} t_{PHL}	2	—	240	—	—	—	300	—	—	—	360	—	—	ns
		4.5	—	48	—	53	—	60	—	66	—	72	—	80	
		6	—	41	—	—	—	51	—	—	—	61	—	—	
Enable to Qn	t_{PLH} t_{PHL}	2	—	240	—	—	—	300	—	—	—	360	—	—	ns
		4.5	—	48	—	55	—	60	—	69	—	72	—	83	
		6	—	41	—	—	—	51	—	—	—	61	—	—	
MR to Qn	t_{PHL}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time	t_{THL} t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4518, CD54/74HCT4518
CD54/74HC4520, CD54/74HCT4520

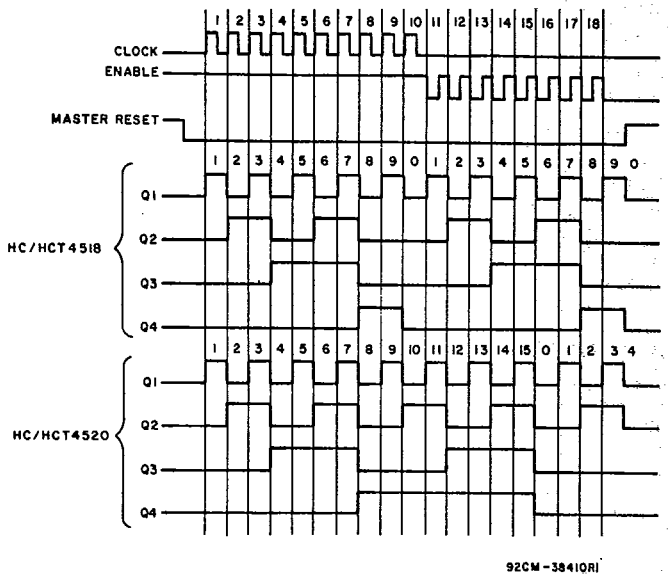


Fig. 4 — Timing Diagrams for CD54/74HC/HCT4518/4520.

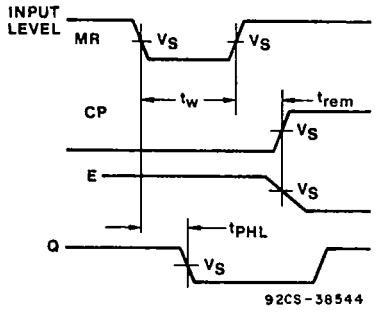


Fig. 5 — Master reset pulse width. Master reset to output delay and master reset to clock recovery times.

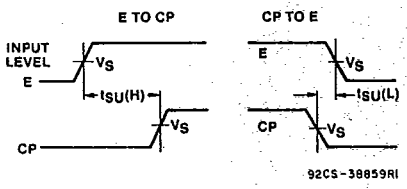


Fig. 6 — Setup Times: E to CP and CP to E.

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V