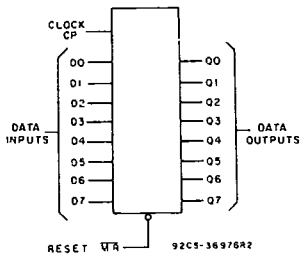
T-46-07-11

CD54/74HC273
CD54/74HCT273

File Number **1479**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal D Flip-Flop with Reset

Type Features:
- *Common clock and asynchronous master reset*
- *Positive-edge triggering*
- *Buffered inputs*
- *Typical f_{max} = 60 MHz @ V_{CC} = 5 V, C_L = 15pF, T_A = 25°C*

The RCA CD54/74HC273 and the CD54/74HCT273 high speed Octal D-Type Flip-Flops with a direct clear input are manufactured with silicon-gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits.

Information at the D input is transferred to the Q outputs on the positive-going edge of the clock pulse. All eight Flip-Flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All eight Q outputs are reset to a logic 0.

The CD54HC273 and CD54HCT273 are supplied in 20-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC273 and CD74HCT273 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:
- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

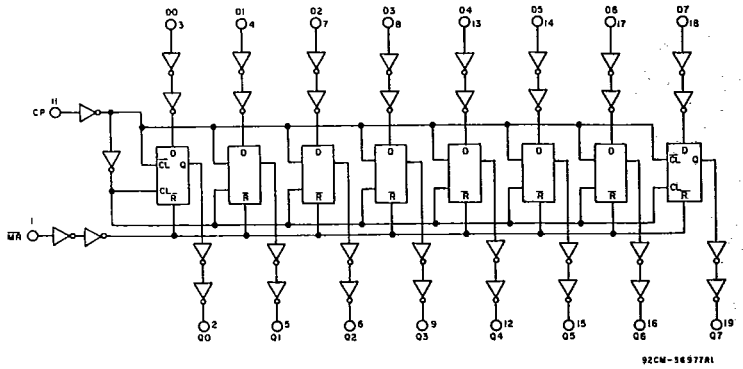


Fig. 1 - Logic diagram.

CD54/74HC273
CD54/74HCT273

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} +0.5$ V ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_o < V_{CC} +0.5 V$) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT, PER PIN (I_{CC}): ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
RESET (MR)	CLOCK CP	DATA Dn	Q
L	X	X	L
H	⌐	H	H
H	⌐	L	L
H	L	X	Qo

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
⌐ = Transition from Low to High Level
Qo = The Level of Q Before the Indicated Steady-State Input Conditions were Established

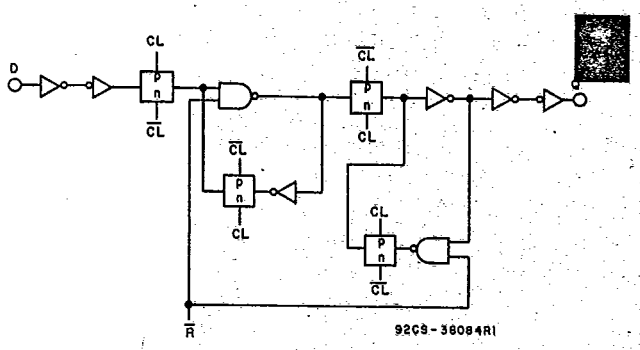


Fig. 2 - Flip-Flop detail.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, tr, tf			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

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CD54/74HCT273

STATIC ELECTRICAL CHARACTERISTICS

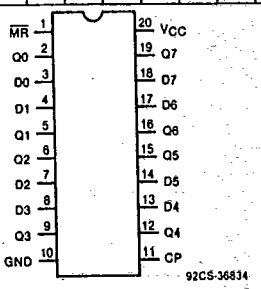
CHARACTERISTIC	CD74HC273/CD54HC273										CD74HCT273/CD54HCT273								UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES	
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
$\overline{MR}$	1.5
Data	0.4
CP	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.



TERMINAL ASSIGNMENT

CD54/74HC273
CD54/74HCT273

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITION V_{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency f_{max} Fig. 3	2	6		—		5		—		4		—		MHz
	4.5	30		25		25		20		20		16		
	6	35		—		29		—		23		—		
$\overline{MR}$ Pulse Width t_w Fig. 4	2	60		—		75		—		90		—		ns
	4.5	12		12		15		15		18		18		
	6	10		—		13		—		15		—		
Clock Pulse Width t_w Fig. 3	2	80		—		100		—		120		—		ns
	4.5	16		20		20		25		24		30		
	6	14		—		17		—		20		—		
Set-up Time Data to Clock t_{su} Fig. 5	2	60		—		75		—		70		—		ns
	4.5	12		12		15		15		18		18		
	6	10		—		13		—		15		—		
Hold Time Data to Clock t_H Fig. 5	2	3		—		3		—		3		—		ns
	4.5	3		3		3		3		3		3		
	6	3		—		3		—		3		—		
Removal Time $\overline{MR}$ to Clock t_{REM}	2	50		—		65		—		75		—		ns
	4.5	10		10		13		13		15		15		
	6	9		—		11		—		13		—		

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay, Clock to Q	t_{PLH} t_{PHL}	15	12	12	ns
Maximum Clock Frequency	f_{max}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	25	25	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma\, C_L V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage.

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SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25°C				-40°C to +85°C				-55°C to +125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2		150		—		190		—		225		—	
Clock to Output	t_{PHL}	4.5		30		30		38		38		45		45	ns
Fig. 3		6		26		—		30		—		38		—	
Propagation Delay		2		150		—		190		—		225		—	
$\overline{MR}$ to Output	t_{PHL}	4.5		30		32		38		40		45		48	ns
Fig. 4		6		26		—		33		—		38		—	
Output Transition	t_{TLH}	2		75		—		95		—		110		—	
Time	t_{THL}	4.5		15		15		19		19		22		22	ns
Fig. 6		6		13		—		16		—		19		—	
Input Capacitance	C_I	—		10		10		10		10		10		10	pF

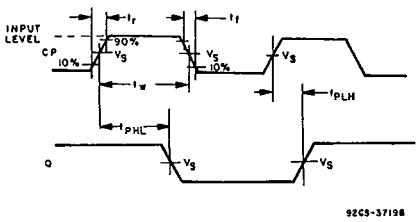


Fig. 3 - Clock to output delays and clock pulse width.

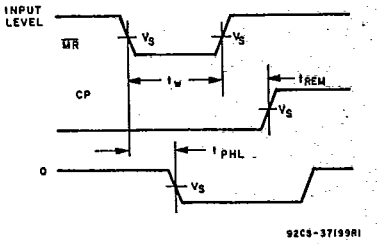
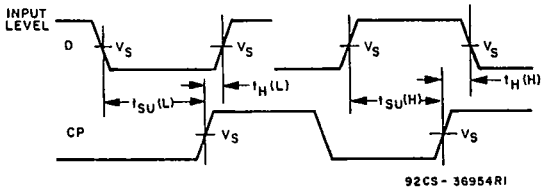


Fig. 4 - Master reset pulse width. Master reset to output delay and master reset to clock recovery time.



	54,74HC	54,74HCT
Input Level	V_{CC}	3 V
V_S	50 V_{CC}	1.3 V

Fig. 5 - Data set-up and hold times.

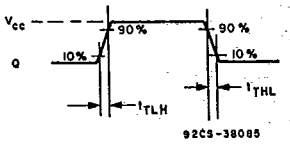


Fig. 6 - Transition times.