PRELIMINARY

W250-03

FTG for VIA Apollo Pro-266

Features

- **Maximized EMI Suppression using Cypress's Spread Spectrum Technology**
- **System frequency synthesizer for VIA Apollo Pro-266**
- **Supports Intel® Pentium® II and Pentium® III class processor**
- **Three copies of CPU output**
- **Nine copies of PCI output**
- **One 48-MHz output for USB**
- **One 24-MHz or 48-MHz output for SIO**
- **Two buffered reference outputs**
- **Three copies of APIC output**
- **Supports frequencies up to 200 MHz**
- **SMBus interface for programming**
- **Power management control inputs**
- **Available in 48-pin SSOP**

Key Specifications

CPU Cycle-to-Cycle Jitter: ..... 250 ps
CPU to CPU Output Skew: ..... 175 ps
PCI Cycle to Cycle Jitter: ..... 500 ps
PCI to PCI Output Skew: ..... 500 ps

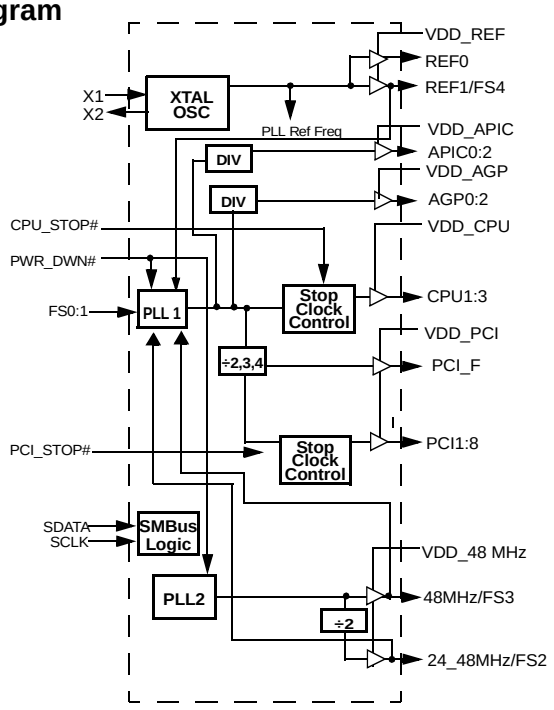
Table 1. Pin Selectable Frequency

Input Address					CPU, (MHz)	AGP	PCI (MHz)	Spread Spectrum
FS4	FS3	FS2	FS1	FS0				
0	0	0	0	0	200.0	66.6	33.3	OFF
0	0	0	0	1	190.0	63.3	31.7	OFF
0	0	0	1	0	180.0	60.0	30.0	OFF
0	0	0	1	1	170.0	56.7	28.3	OFF
0	0	1	0	0	166.0	83.0	41.5	OFF

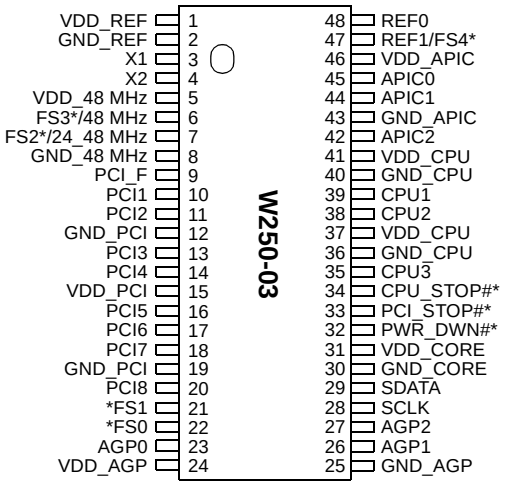
Table 1. Pin Selectable Frequency (continued)

Input Address					CPU, (MHz)	AGP	PCI (MHz)	Spread Spectrum
FS4	FS3	FS2	FS1	FS0				
0	0	1	0	1	160.0	80.0	40.0	OFF
0	0	1	1	0	150.0	75.0	37.5	OFF
0	0	1	1	1	145.0	72.5	36.3	OFF
0	1	0	0	0	140.0	70.0	35.0	OFF
0	1	0	0	1	136.0	68.0	34.0	OFF
0	1	0	1	0	130.0	65.0	32.5	OFF
0	1	0	1	1	124.0	62.0	31.0	OFF
0	1	1	0	0	66.6	66.6	33.3	OFF
0	1	1	0	1	100.0	66.6	33.3	OFF
0	1	1	1	0	118.0	78.7	39.3	OFF
0	1	1	1	1	133.3	66.6	33.3	OFF
1	0	0	0	0	66.8	66.8	33.4	±0.25%
1	0	0	0	1	100.2	66.8	33.4	±0.25%
1	0	0	1	0	115.0	76.7	38.3	OFF
1	0	0	1	1	133.6	66.8	33.4	±0.25%
1	0	1	0	0	66.8	66.8	33.4	±0.5%
1	0	1	0	1	100.2	66.8	33.4	±0.5%
1	0	1	1	0	110.0	73.3	36.7	OFF
1	0	1	1	1	133.6	66.8	33.4	±0.5%
1	1	0	0	0	105.0	70.0	35.0	OFF
1	1	0	0	1	90.0	60.0	30.0	OFF
1	1	0	1	0	85.0	56.7	28.3	OFF
1	1	0	1	1	78.0	78.0	39.0	OFF
1	1	1	0	0	66.6	66.6	33.3	-0.5%
1	1	1	0	1	100.0	66.6	33.3	-0.5%
1	1	1	1	0	75.0	75.0	37.5	OFF
1	1	1	1	1	133.3	66.6	33.3	-0.5%

Block Diagram



Pin Configuration[1]



Note:
1. Signals marked with '*' have internal pull-up resistors.

Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CPU1:3	39, 38, 35	O	***CPU Clock Output:*** Frequency is set by the FS0:4 input or through serial input interface. The CPU1:3 output are gated by the CLK_STOP# input.
CPU_STOP#*	34	I	***CPU Output Control:*** 3.3V LVTTL compatible input that stop CPU1:3 clocks.
PCI1:8	10, 11, 13, 14, 16, 17, 18, 20	O	***PCI Clock Outputs 1 through 8:*** Frequency is set by FS0:4 inputs or through serial input interface, see *Table 1* and *Table 5* for details. Output voltage swing is controlled by voltage applied to VDD_PCI.
PCI_STOP#*	33	O	***PCI_STOP# Input:*** 3.3V LVTTL compatible input that stops PCI1:8.
PCI_F	9	O	***Free-Running PCI Clock Output:*** Output voltage swing is controlled by the voltage applied to VDD_PCI. See *Table 1.* and *Table 5.* for detailed frequency information.
PWR_DWN#*	32	I	***PWR_DWN# Input:*** LVTTL-compatible input that places the device in power-down mode when held LOW.
APIC0:2	45, 44, 42	O	***APIC Clock Output:*** APIC clock outputs. The output voltage swing is controlled by VDD_APIC.
48MHz/FS3*	6	I/O	***48-MHz Output/Frequency Select 3:*** 48 MHz is provided in normal operation. In standard PC systems, this output can be used as the reference for the Universal Serial Bus host controller. This pin also serves as a power-on strap option to determine device operating frequency as described in *Table 1*.
24_48MHz/ FS2*	7	I/O	***24_48-MHz Output/Frequency Select 2:*** In standard PC systems, this output can be used as the clock input for a Super I/O chip. The output frequency is controlled by Configuration Byte 3 bit[6]. The default output frequency is 24 MHz. This pin also serves as a power-on strap option to determine device operating frequency as described in *Table 1*.
REF1/FS4*	47	I/O	***Reference Clock Output 1/Frequency Select 4:*** 3.3V 14.318-MHz output clock. This pin also serves as a power-on strap option to determine device operating frequency as described in *Table 1*. Upon power-up, FS4 input will be latched which will set clock frequencies as described in *Table 1*.
REF0	48	O	***Reference Clock Output 0:*** 3.3V 14.318 MHz output clock.
SCLK	28	I	Clock pin for serial interface circuitry.
SDATA	29	I/O	Data pin for serial interface circuitry.
X1	3	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
X2	4	I	***Crystal Connection:*** An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.
FS0,FS1	22, 21	I	***FS0, FS1 Inputs:*** Latched frequency select inputs. These latched input serve as a power-on strap option to determine device operating frequency as described in *Table 1.*
AGP0:2	23, 26, 27	O	***AGP Outputs:*** Output frequency is set by FS0:4 inputs or through serial interface.
VDD_REF, VDD_48MHz, VDD_PCI, VDD_AGP, VDD_CORE	1, 5,15, 24, 31	P	***Power Connection:*** Power supply for core logic, PLL circuitry, PCI outputs, reference outputs, 48-MHz output, and 24_48-MHz output, connect to 3.3V supply.
VDD_CPU, VDD_APIC	41, 46, 37	P	***Power Connection:*** Power supply for APIC and CPU1 output buffers, connect to 2.5V.
GND_REF, GND_48MHz, GND_PCI, GND_AGP, GND_CORE, GND_CPU, GND_APIC	2, 8, 12, 19, 25, 30, 36, 40, 43	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.

Serial Data Interface

The serial data interface can be used to configure internal register settings that control particular device functions. Upon power-up, the W250-03 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 2* summarizes the control functions of the serial data interface.

Operation

Data is written to the W250-03 in eleven bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections through software. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Spread Spectrum Enabling	Enables or disables spread spectrum clocking.	For EMI reduction.
Output Three-state	Puts clock output into a high impedance state.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the W250-03 to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W250-03 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the W250-03, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the W250-03, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to *Table 4*	The data bits in Data Bytes 0–7 set internal W250-03 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to *Table 4*, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		
11	Data Byte 7		

Writing Data Bytes

Each bit in Data Bytes 0–7 controls a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. *Table 4* gives the bit formats for registers located in Data Bytes 0–7.

Table 5 details additional frequency selections that are available through the serial data interface.

Table 4. Data Bytes 0–7 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	--	--	(Reserved)	--	--	0
6	--	--	SEL_2	See *Table 5*		0
5	--	--	SEL_1	See *Table 5*		0
4	--	--	SEL_0	See *Table 5*		0
3	--	--	Hardware/Software Frequency Select	Hardware	Software	0
2	--	--	SEL_4	See *Table 5*		1
1	--	--	SEL_3	See *Table 5*		0
0	--	--		Normal	Three-stated	0
Data Byte 1						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	35	CPU3	Clock Output Disable	Low	Active	1
2	38	CPU2	Clock Output Disable	Low	Active	1
1	39	CPU1	Clock Output Disable	Low	Active	1
0	42	APIC2	Clock Output Disable	Low	Active	1
Data Byte 2						
7	20	PCI8	Clock Output Disable	Low	Active	1
6	18	PCI7	Clock Output Disable	Low	Active	1
5	17	PCI6	Clock Output Disable	Low	Active	1
4	16	PCI5	Clock Output Disable	Low	Active	1
3	14	PCI4	Clock Output Disable	Low	Active	1
2	13	PCI3	Clock Output Disable	Low	Active	1
1	11	PCI2	Clock Output Disable	Low	Active	1
0	10	PCI1	Clock Output Disable	Low	Active	1
Data Byte 3						
7	--	--	(Reserved)	--	--	0
6	--	SEL_48MHz	SEL 48MHz as the output frequency for 24_48MHz	24 MHz	48 MHz	0
5	6	48MHz	Clock Output Disable	Low	Active	1
4	7	24_48MHz	Clock Output Disable	Low	Active	1
3	9	PCI_F	Clock Output Disable	Low	Active	1
2	27	AGP2	Clock Output Disable	Low	Active	1
1	26	AGP1	Clock Output Disable	Low	Active	1

Table 4. Data Bytes 0–7 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
0	23	AGP0	Clock Output Disable	Low	Active	1
Data Byte 4						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0
Data Byte 5						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	44	APIC1	Clock Output Disable	Low	Active	1
4	45	APIC0	Clock Output Disable	Low	Active	1
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	47	REF1	Clock Output Disable	Low	Active	1
0	48	REF0	Clock Output Disable	Low	Active	1
Data Byte 6						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0
Data Byte 7						
7	--	--	(Reserved)	--	--	0
6	--	--	(Reserved)	--	--	0
5	--	--	(Reserved)	--	--	0
4	--	--	(Reserved)	--	--	0
3	--	--	(Reserved)	--	--	0
2	--	--	(Reserved)	--	--	0
1	--	--	(Reserved)	--	--	0
0	--	--	(Reserved)	--	--	0

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes

Input Conditions					Output Frequency			
Data Byte 0, Bit 3 = 1								
Bit 2 SEL_4	Bit 1 SEL_3	Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU	AGP	PCI	Spread Spectrum
0	0	0	0	0	200.0	66.6	33.3	OFF
0	0	0	0	1	190.0	63.3	31.7	OFF
0	0	0	1	0	180.0	60.0	30.0	OFF
0	0	0	1	1	170.0	56.7	28.3	OFF
0	0	1	0	0	166.0	83.0	41.5	OFF
0	0	1	0	1	160.0	80.0	40.0	OFF
0	0	1	1	0	150.0	75.0	37.5	OFF
0	0	1	1	1	145.0	72.5	36.3	OFF
0	1	0	0	0	140.0	70.0	35.0	OFF
0	1	0	0	1	136.0	68.0	34.0	OFF
0	1	0	1	0	130.0	65.0	32.5	OFF
0	1	0	1	1	124.0	62.0	31.0	OFF
0	1	1	0	0	66.6	66.6	33.3	OFF
0	1	1	0	1	100.0	66.6	33.3	OFF
0	1	1	1	0	118.0	78.7	39.3	OFF
0	1	1	1	1	133.3	66.6	33.3	OFF
1	0	0	0	0	66.8	66.8	33.4	±0.25%
1	0	0	0	1	100.2	66.8	33.4	±0.25%
1	0	0	1	0	115.0	76.7	38.3	OFF
1	0	0	1	1	133.6	66.8	33.4	±0.25%
1	0	1	0	0	66.8	66.8	33.4	±0.5%
1	0	1	0	1	100.2	66.8	33.4	±0.5%
1	0	1	1	0	110.0	73.3	36.7	OFF
1	0	1	1	1	133.6	66.8	33.4	±0.5%
1	1	0	0	0	105.0	70.0	35.0	OFF
1	1	0	0	1	90.0	60.0	30.0	OFF
1	1	0	1	0	85.0	56.7	28.3	OFF
1	1	0	1	1	78.0	78.0	39.0	OFF
1	1	1	0	0	66.6	66.6	33.3	–0.5%
1	1	1	0	1	100.0	66.6	33.3	–0.5%
1	1	1	1	0	75.0	75.0	37.5	OFF
1	1	1	1	1	133.3	66.6	33.3	–0.5%

Absolute Maximum Ratings [2]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
ESD_{PROT}	Input ESD Protection	2 (min.)	kV

DC Electrical Characteristics: T_A = 0°C to +70°C, 3.3V, V_{DD} = 3.3V±5%, 2.5V, V_{DD} = 2.5V±5%

Parameter	Description		Test Condition	Min.	Typ.	Max.	Unit
Supply Current							
I_{DD}	3.3V Supply Current		CPU1:3 = 133 MHz [3]		TBD		mA
I_{DD}	2.5V Supply Current				TBD		mA
Logic Inputs							
V_{IL}	Input Low Voltage			GND – 0.3		0.8	V
V_{IH}	Input High Voltage			2.0		V_{DD} + 0.3	V
I_{IL}	Input Low Current[4]					–25	µA
I_{IH}	Input High Current[4]					10	µA
Clock Outputs							
V_{OL}	Output Low Voltage		I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage		I_{OH} = –1 mA	3.1			V
V_{OH}	Output High Voltage	CPU1:3, APIC0:2	I_{OH} = –1 mA	2.2			V
I_{OL}	Output Low Current	CPU1:3	V_{OL} = 1.25V	27	57	97	mA
		PCI_F, PCI1:8	V_{OL} = 1.5V	20.5	53	139	mA
		AGP0:2	V_{OL} = 1.5V	40	85	140	mA
		APIC 0:2	V_{OL} = 1.25V	40	85	140	mA
		REF0:1	V_{OL} = 1.5V	25	37	76	mA
		48 MHz	V_{OL} = 1.5V	25	37	76	mA
		24 MHz	V_{OL} = 1.5V	25	37	76	mA
I_{OH}	Output High Current	CPU1:3	V_{OH} = 1.25V	25	55	97	mA
		PCI_F, PCI1:8	V_{OH} = 1.5V	31	55	139	mA
		AGP0:2	V_{OL} = 1.5V	40	85	140	mA
		APIC0:2	V_{OH} = 1.25V	40	87	155	mA
		48 MHz	V_{OH} = 1.5V	27	44	94	mA
		24 MHz	V_{OH} = 1.5V	25	37	76	mA

Notes:

2. **Multiple Supplies**: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. All clock outputs loaded with 6" 60Ω transmission lines with 22-pF capacitors.
4. Inputs have internal pull-up resistors.

DC Electrical Characteristics: T_A = 0°C to +70°C, 3.3V, V_{DD} = 3.3V±5%, 2.5V, V_{DD} = 2.5V±5% (continued)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Crystal Oscillator						
V_{TH}	X1 Input Threshold Voltage[5]	V_{DDQ3} = 3.3V		1.65		V
C_{LOAD}	Load Capacitance, Imposed on External Crystal[6]			18		pF
$C_{IN,X1}$	X1 Input Capacitance[7]	Pin X2 unconnected		28		pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

AC Electrical Characteristics

T_A = 0°C to +70°C, 3.3V, V_{DD}= 3.3V±5%, 2.5V, V_{DD}= 2.5V± 5% f_{XTL} = 14.31818 MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum is disabled.

CPU Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/ Comments	CPU = 66.6 MHz			CPU = 100 MHz			CPU = 133 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_P	Period	Measured on rising edge at 1.25	15		15.5	10		10.5	7.5		8.0	ns
t_H	High Time	Duration of clock cycle above 2.0V	5.2			3.0			1.87			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.0			2.8			1.67			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.0V	1		4	1		4	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.0V to 0.4V	1		4	1		4	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.25V	45		55	45		55	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.			250			250			250	ps
t_{SK}	Output Skew	Measured on rising edge at 1.25V			175			175			175	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3			3			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20			20			20		Ω

Notes:

5. X1 input threshold voltage (typical) is 3.3V/2.
6. The W250-03 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
7. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

PCI Clock Outputs, PCI0:5 (Lump Capacitance Test Load = 30 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
t_P	Period	Measured on rising edge at 1.5V	30			ns
t_H	High Time	Duration of clock cycle above 2.4V	12			ns
t_L	Low Time	Duration of clock cycle below 0.4V	12			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			500	ps
t_O	CPU to PCI Clock Skew	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.	1.5		4	ns
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		Ω

AGP Clock Outputs (Lump Capacitance test Load = 30 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
t_P	Period	Measured on rising edge at 1.5V	15			ns
t_H	High Time	Duration of clock cycle above 2.4V	5.25			ns
t_L	Low Time	Duration of clock cycle below 0.4V	5.05			ns
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	1		4	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	1		4	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
t_{JC}	Jitter, Cycle-to-Cycle	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.			500	ps
t_{SK}	Output Skew	Measured on rising edge at 1.5V			250	ps
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		30		Ω

APIC Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated from PCI divided by 2		PCI/2		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		20		Ω

REF Clock Outputs (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Frequency generated by crystal oscillator		14.318		MHz
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)

Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		48.008		MHz
f_D	Deviation from 48 MHz	(48.008 – 48)/48		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/17 = 48.008 MHz)		57/17		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)

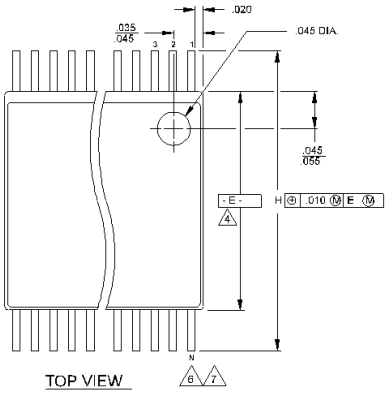
Parameter	Description	Test Condition/Comments	Min.	Typ.	Max.	Unit
f	Frequency, Actual	Determined by PLL divider ratio (see m/n below)		24.004		MHz
f_D	Deviation from 24 MHz	(24.004 – 24)/24		+167		ppm
m/n	PLL Ratio	(14.31818 MHz x 57/34 = 24.004 MHz)		57/34		
t_R	Output Rise Edge Rate	Measured from 0.4V to 2.4V	0.5		2	V/ns
t_F	Output Fall Edge Rate	Measured from 2.4V to 0.4V	0.5		2	V/ns
t_D	Duty Cycle	Measured on rising and falling edge at 1.5V	45		55	%
f_{ST}	Frequency Stabilization from Power-up (cold start)	Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization.			3	ms
Z_o	AC Output Impedance	Average value during switching transition. Used for determining series termination value.		40		Ω

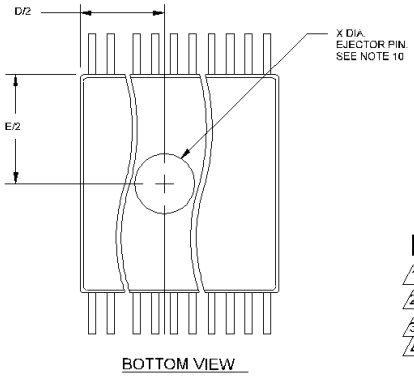
Ordering Information

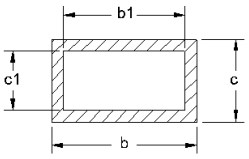
Ordering Code	Package Name	Package Type
W250-03	H	48-pin SSOP (300 mils)

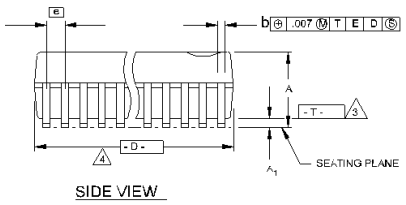
Package Diagram

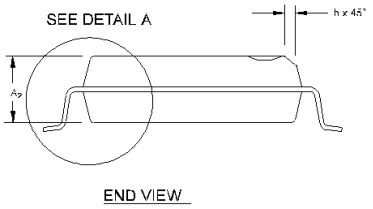
48-Pin Small Shrink Outline Package (SSOP, 300 mils)

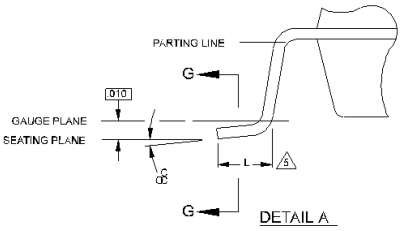












NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. CONTROLLING DIMENSION: INCHES.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 INCHES AND .010 INCHES FROM THE LEAD TIPS.
12. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-118, VARIATIONS AA, AB, EXCEPT CHAMFER DIMENSION h. JEDEC SPECIFICATION FOR h IS .015"/.025".

SYMBOL	COMMON DIMENSIONS				NOTE	4			6
				h, L	VARI-ATIONS	D			N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.095	.102	.110		AA	.620	.625	.630	48
A_1	.008	.012	.016		AB	.720	.725	.730	56
A_2	.088	.090	.092						
b	.008	.010	.0135						
b_1	.008	.010	.012						
c	.005	-	.010						
c_1	.005	.006	.0085						
D	SEE VARIATIONS			4					
E	.292	.296	.299						
e	.025 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			6					
X	.085	.093	.100	10					
α	0°	5°	8°						

THIS TABLE IN INCHES

Summary of nominal dimensions in inches:

Body Width: 0.296
Lead Pitch: 0.025
Body Length: 0.625
Body Height: 0.102

SYMBOL	COMMON DIMENSIONS				NOTE	4			6
				h, L	VARI-ATIONS	D			N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.41	2.59	2.79		AA	15.75	15.88	16.00	48
A_1	0.20	0.31	0.41		AB	18.29	18.42	18.54	56
A_2	2.24	2.29	2.34						
b	0.203	0.254	0.343						
b_1	0.203	0.254	0.305						
c	0.127	-	0.254						
c_1	0.127	0.152	0.216						
D	SEE VARIATIONS			4					
E	7.42	7.52	7.59						
e	0.635 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			6					
X	2.16	2.36	2.54	10					
α	0°	5°	8°						

THIS TABLE IN MILLIMETERS

Document Title: W250-03 FTG for VIA Apollo Pro-266 Document Number: 38-07254				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110519	01/07/02	SZV	Change from Spec number: 38-01080 to 38-07254
*A	122856	12/14/02	RBI	Power up requirements added to Operating Conditions Information