

File Number 1770

CD54/74HC85

CD54/74HCT85

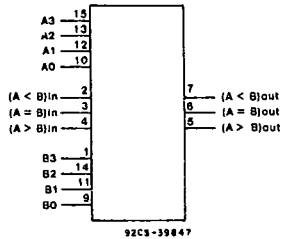
HARRIS SEMICONDUCTOR

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High-Speed CMOS Logic

T-45-17-00



FUNCTIONAL DIAGRAM

4-Bit Magnitude Comparator

Type Features:

- Buffered inputs and outputs
- Typical propagation delay = 13 ns (Data to Output)
@ $V_{CC} = 5V$, $C_L = 15 pF$, $T_A = 25^\circ C$
- Serial or Parallel expansion without external gating.

The RCA-CD54/74HC/HCT85 are high-speed magnitude comparators that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

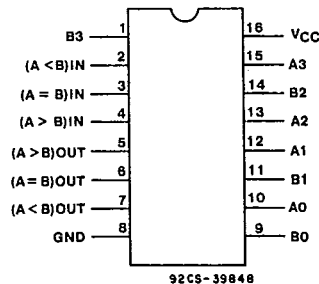
These 4-bit devices compare two binary, BCD, or other monotonic codes and present the three possible magnitude results at the outputs ($A > B$, $A < B$, and $A = B$). The 4-bit input words are weighted (A_0 to A_3 and B_0 to B_3), where A_3 and B_3 are the most significant bits.

The HC/HCT85 are expandable without external gating, in both serial and parallel fashion. The upper part of the truth table indicates operation using a single device or devices in a serially-expanded application. The parallel expansion scheme is described by the last three entries in the truth table. Circuits for serial and parallel comparison of 12 bits are shown in figures 3 and 4, respectively.

The CD54HC/HCT85 are supplied in 16-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT85 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT/HCU: -40 to $+85^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source Is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 V$ Max., $V_{IH} = 2 V$ Min.
CMOS Input Compatibility $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC85 CD54/74HCT85

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):

(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 50 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+80^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE (T_{stg}):

LEAD TEMPERATURE (DURING SOLDERING):	-65 to $+150^\circ\text{C}$
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At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)	
with solder contacting lead tips only	$+300^\circ\text{C}$

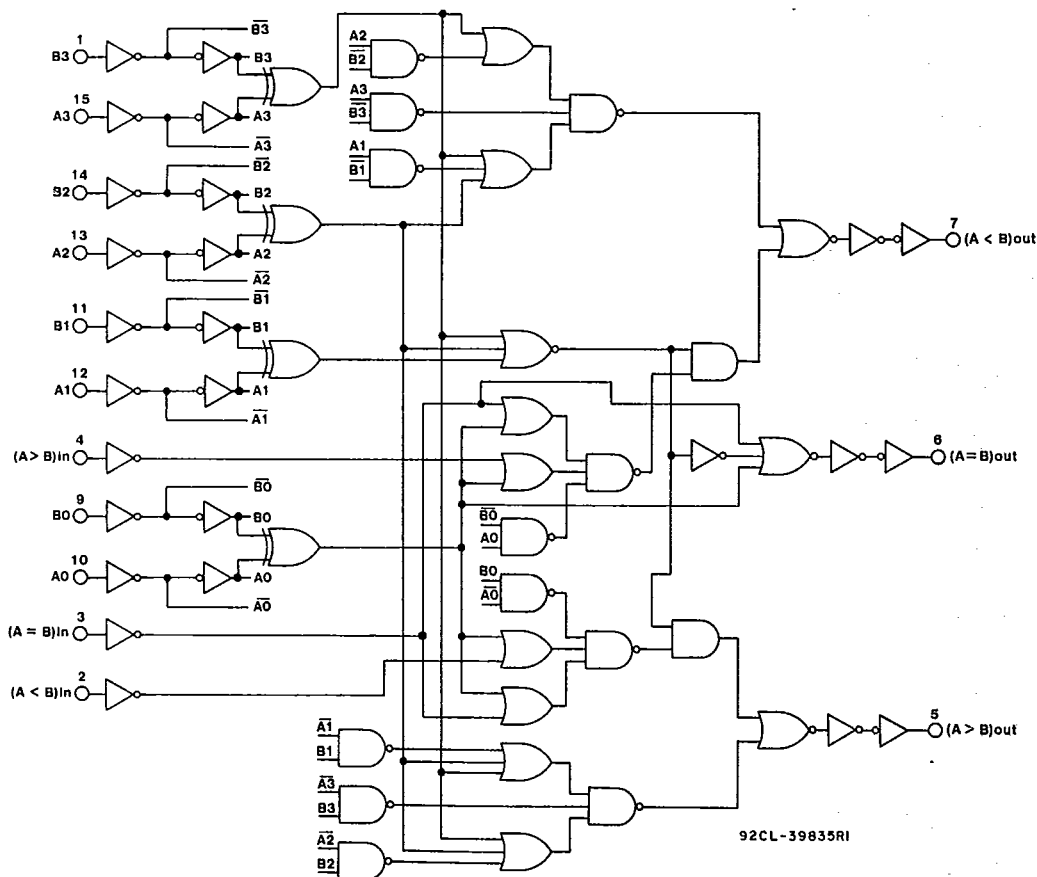


Fig. 1 - Logic diagram

CD54/74HC85

CD54/74HCT85

TRUTH TABLE

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

single device
or
series cascading

parallel cascading

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC} .* CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_i , V_o	0	V_{CC}	V
Operating Temperature T_A : CD74 Types CD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall Times t_r , t_f at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC85

CD54/74HCT85

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC85/CD54HC85										CD74HCT85/CD54HCT85										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage	V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	2	—	—	2	—	2	—	V
				4.5	3.15	—	—	3.15	—	3.15	—		to								
				6	4.2	—	—	4.2	—	4.2	—		5.5								
Low-Level Input Voltage	V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5	—	—	0.8	—	0.8	—	0.8	V
				4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	—	—	—	—	—	
				6	—	—	1.8	—	1.8	—	1.8	—	5.5	—	—	—	—	—	—	—	
High-Level Output Voltage	V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
CMOS Loads				4.5	4.4	—	—	4.4	—	4.4	—		4.5	—	—	—	—	—	—	—	
				6	5.9	—	—	5.9	—	5.9	—		V _{IH}	—	—	—	—	—	—	—	
TTL Loads	V _{IL} or V _{IH}											V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
				-4	4.5	3.98	—	—	3.84	—	3.7	—		—	—	—	—	—	—	—	
				-5.2	6	5.48	—	—	5.34	—	5.2	—		V _{IH}	—	—	—	—	—	—	
Low-Level Output Voltage	V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
				4.5	—	—	0.1	—	0.1	—	0.1		—	—	—	—	—	—	—	—	
				6	—	—	0.1	—	0.1	—	0.1		V _{IH}	—	—	—	—	—	—	—	
TTL Loads	V _{IL} or V _{IH}											V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
				4	4.5	—	—	0.26	—	0.33	—		—	—	—	—	—	—	—	—	
				5.2	6	—	—	0.26	—	0.33	—		V _{IH}	—	—	—	—	—	—	—	
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin, 1 unit load	ΔI _{CC} *											V _{CC} -2.1 4.5 to 5.5	—	100	360	—	450	—	490	μA	

* For dual-supply systems theoretical worst case ($V_i = 2.4$ V, $V_{cc} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
A0-A3, B0-B3 and (A=B) in	1.5
(A>B) in, (A<B) in	1

*Unit Load is ΔI_{cc} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay An, Bn to (A>B)out, (A<B)out	t_{PLH} t_{PHL}	15	16	15	ns
An, Bn to (A=B) out			14	17	ns
(A>B)in, (A<B)in (A=B)in to (A>B)out, (A<B)out			11	12	ns
(A=B) in to (A=B)out			9	13	ns
Power Dissipation Capacitance*	C_{PD}	—	24	26	pF

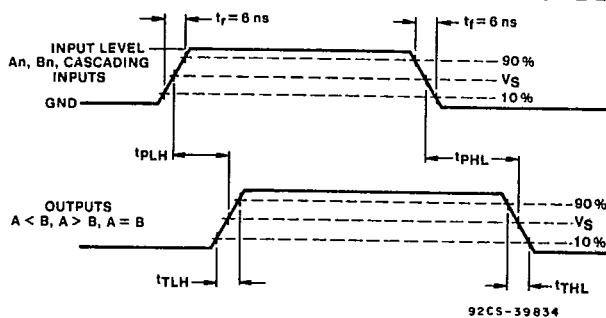
* C_{PD} is used to determine the dynamic power consumption, per package.
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage
SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	TEST CONDITION V _{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delay t _{PLH} An, Bn to (A>B)out, t _{PHL} (A<B)out	2 4.5 6	— — —	195 39 33	— — —	— 37 —	— 47 42	245 — —	— 46 —	— — —	— 59 50	— — —	— 56 —	ns	
An, Bn to (A=B)out	2 4.5 6	— — —	175 35 30	— — —	— 40 —	— 44 37	240 — —	— 50 —	— — —	265 53 45	— — —	— 60 —	ns	
(A>B)in, (A<B)in, (A=B)in to (A>B)out, (A<B)out	2 4.5 6	— — —	140 28 24	— — —	— 30 —	— 35 30	175 — —	— 38 —	— — —	210 42 36	— — —	— 45 —	ns	
(A=B)in to (A=B)out	2 4.5 6	— — —	120 24 20	— — —	— 31 —	— 30 26	150 — —	— 39 —	— — —	180 36 31	— — —	— 47 —	ns	
Output t _{TLH} Transition t _{THL} Time	2 4.5 6	— — —	75 15 13	— — —	— 15 —	— 19 16	95 — —	— 19 —	— — —	110 22 19	— — —	— 22 —	ns —	
Input C _i Capacitance	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC85 CD54/74HCT85

HARRIS SEMICOND SECTOR

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	54/74HC	54/74HCT
Input Level	V _{CC}	3 V
Switching Voltage, V _s	50% V _{CC}	1.3 V

Fig. 2 - Transition times, propagation delay times

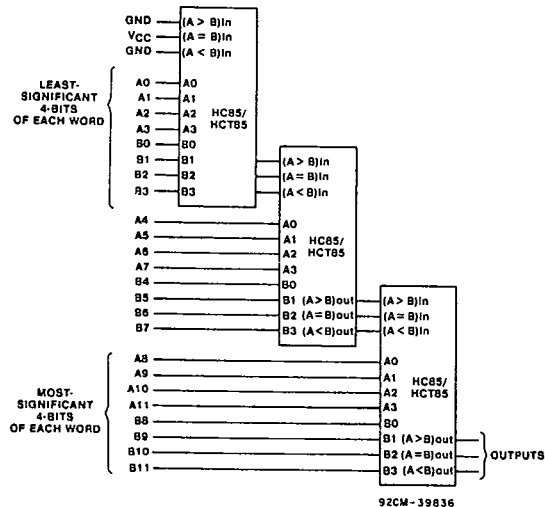


Fig. 3 - Series cascading --- comparing 12-bit words.

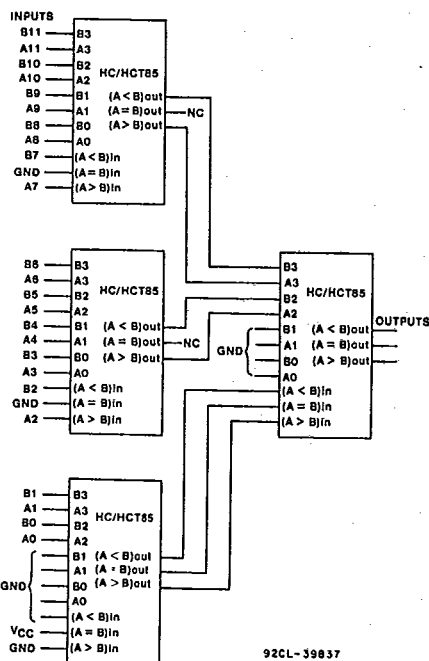


Fig. 4 - Parallel cascading --- comparing 12-bit words.