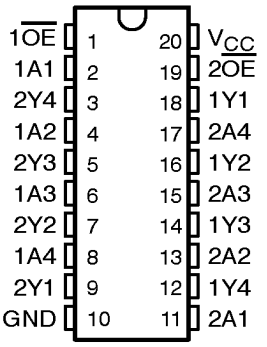
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **750-ps Maximum Output Skew Between All Outputs**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Packaged in Shrink Small-Outline Package (SSOP)**

DB PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The CDC3244 is designed specifically for low-voltage 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The CDC3244 provides a low-cost solution in applications that require skews of less than 750 ps.

The CDC3244 is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

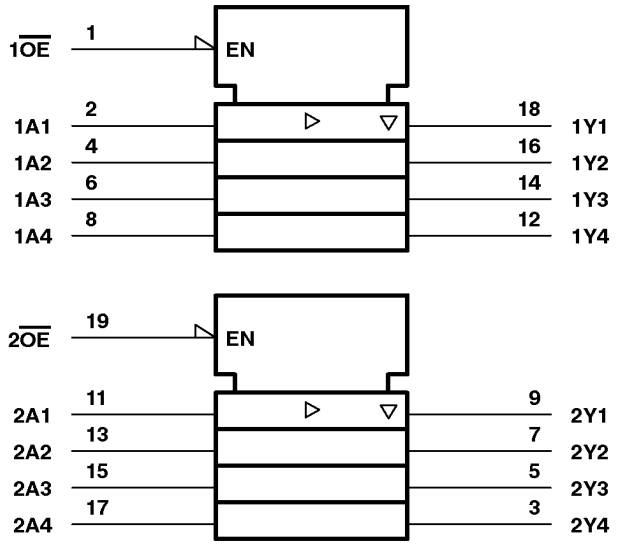
The CDC3244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

FUNCTION TABLE
(each driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

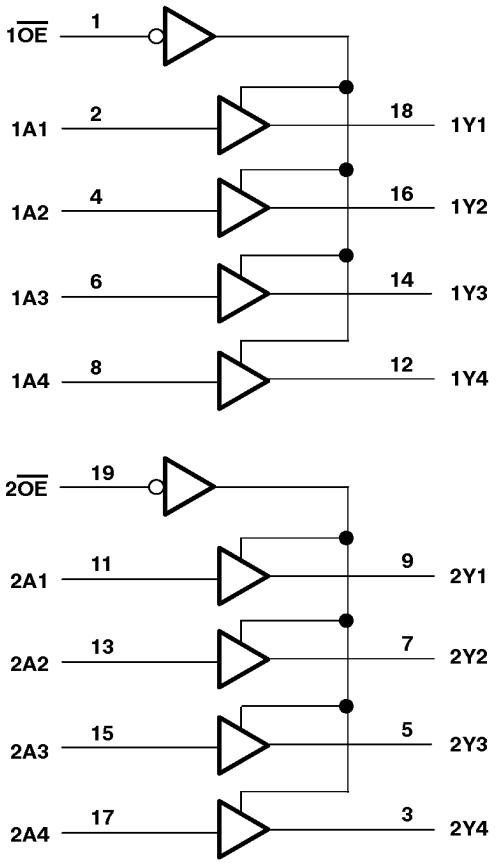
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V
Current into any output in the low state, I_O . . . . . 128 mA
Current into any output in the high state, I_O (see Note 2) . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) . . . . . 0.6 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
f_{clock}	Clock frequency				MHz
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 μA		V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			
	V_{CC} = 3 V,	I_{OH} = –32 mA		2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 μA				0.2	V
		I_{OL} = 24 mA				0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4	
		I_{OL} = 32 mA				0.5	
		I_{OL} = 64 mA				0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10	μA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1	
		V_I = V_{CC}	Data pins			1	
		V_I = 0				–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				±100	μA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			μA
		V_I = 2 V		–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5	μA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5	μA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19	mA
			Outputs low		8.6	12	
			Outputs disabled		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2	mA
C_i	V_I = 3 V or 0				4		pF
C_o	V_O = 3 V or 0				8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.5	4.1		5	ns
t_{PHL}			1	2.5	4.1		5.2	
t_{PZH}	$\overline{OE}$	Y	1	2.7	5.2		6.3	ns
t_{PZL}			1.1	3.1	5.2		6.7	
t_{PHZ}	$\overline{OE}$	Y	1.9	3.9	5.6		6.3	ns
t_{PLZ}			1.8	3.2	5.1		5.6	
$t_{sk(o)}$	A	Y			750		750	ps

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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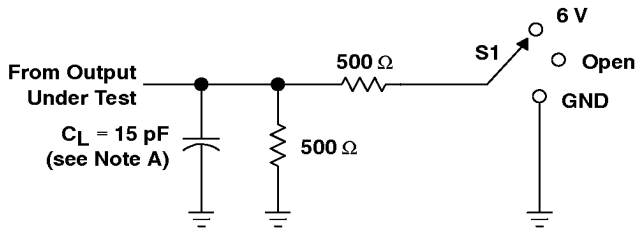
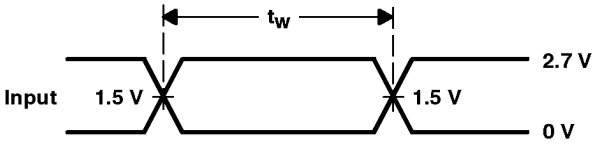
PARAMETER MEASUREMENT INFORMATION
CLOCK DRIVER CIRCUITS

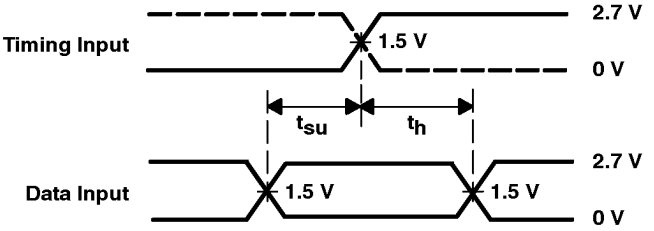


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

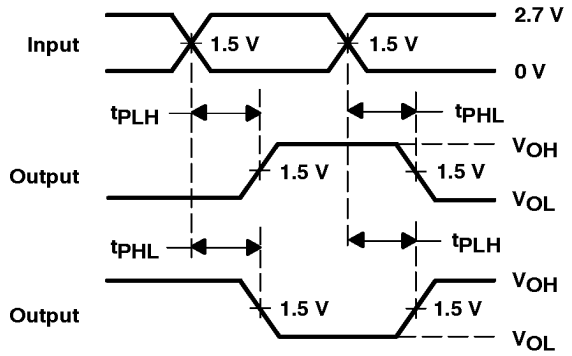
LOAD CIRCUIT FOR OUTPUTS



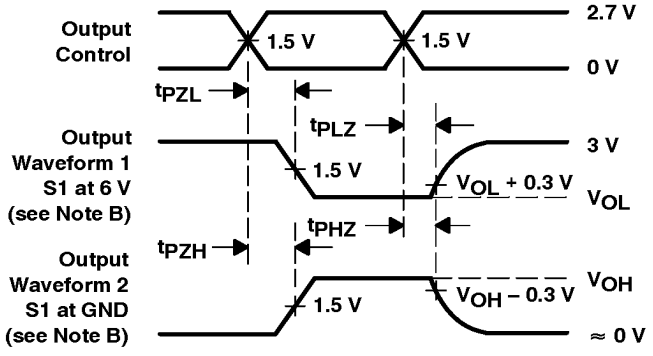
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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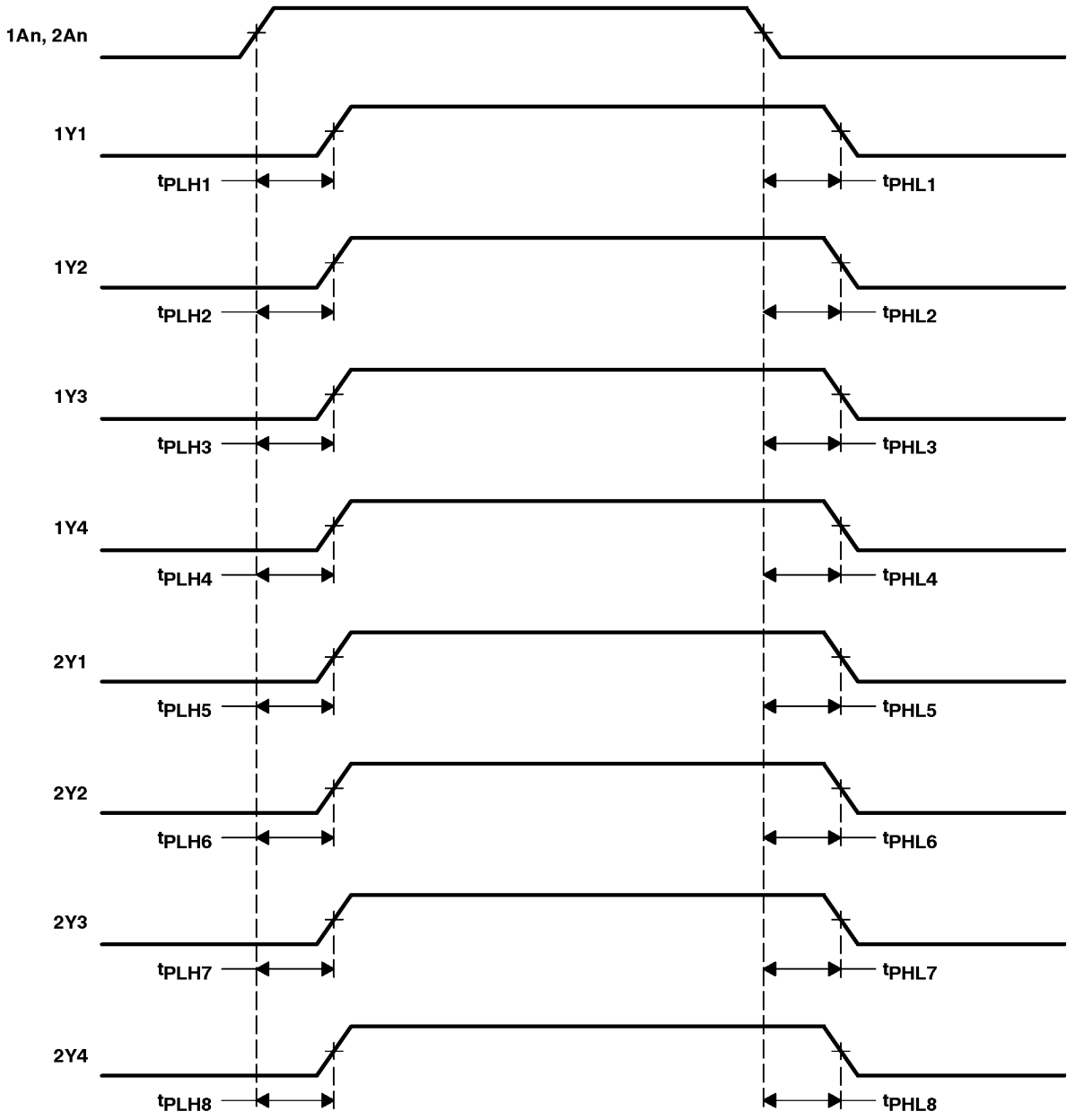
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8)
The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$