



2Mx64 3.3V Simultaneous Operation Flash Multi-Chip Package

**Preliminary*

FEATURES

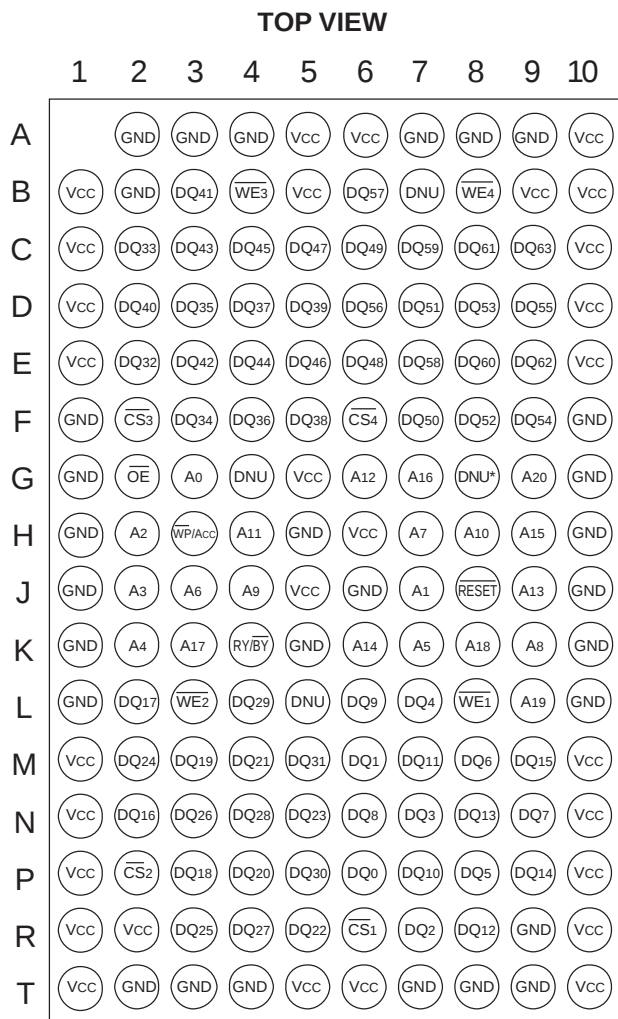
- Access Times of 100, 120, 150ns
- Packaging
 - 159 PBGA, 13x22mm - 1.27mm pitch
- 1,000,000 Erase/Program Cycles
- Sector Architecture
 - Bank 1 (8Mb): eight 4K word, fifteen 32K word
 - Bank 2 (24Mb): forty-eight 32K word
- Bottom boot block
- Zero Power Operation
- Organized as 2Mx64 or 2x2Mx32
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt for Read and Write Operations
- Simultaneous Read/Write Operation:
 - Data can be continuously read from one bank while executing erase/program functions in another bank
 - Zero latency between read and write operations
- Erase Suspend/Resume
 - Suspends erase operations to allow programming in same bank
- Data Polling and Toggle Bits
 - Provides a software method of detecting the status of program or erase cycles
- Unlock Bypass Program command
 - Reduces overall programming time when issuing multiple program command sequences
- Ready/Busy output (RY/BY)
 - Hardware method for detecting program or erase cycle completion
- Hardware reset pin (RESET)
 - Hardware method of resetting the internal state machine to the read mode
- WP/ACC input pin
 - Write protect (WP) function allows protection of two outermost boot sectors, regardless of sector protect status
 - Acceleration (ACC) function accelerates program timing
- Sector Protection
 - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
 - Temporary Sector Unprotect allows changing data in protected sectors in-system

Note: For programming information refer to Flash Programming W72M64V-XBX Application Note.

** Preliminary datasheet. This datasheet describes a product that is not characterized or qualified and is subject to change without notice.*



FIG 1: PIN CONFIGURATION FOR W72M64V-XBX

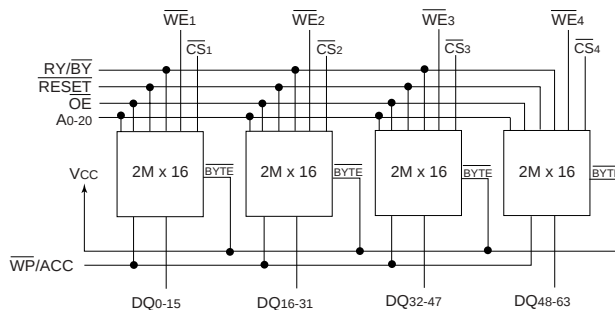


PIN DESCRIPTION

DQ0-63	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{\text{WE}}1-4$	Write Enables
$\overline{\text{CS}}1-4$	Chip Selects
$\overline{\text{OE}}$	Output Enable
$\overline{\text{RESET}}$	Hardware Reset
$\overline{\text{WP/ACC}}$	Hardware Write Protect/Acceleration
R $\overline{\text{Y}}/\text{B}\overline{\text{Y}}$	Ready/Busy Output
VCC	Power Supply
GND	Ground
DNU	Do Not Use

* Ball G8 is DNU on this device and will become A21 on the W74M64V-XBX

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V _{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to V _{CC} +0.5	V
Storage Temperature Range	-55 to +150	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
WE ₁₋₄ capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	25	pF
CS ₁₋₄ capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	25	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	12	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	25	pF
RESET capacitance	C _{RS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
RY/BY capacitance	C _{RB}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
WP/Acc capacitance	C _{WA}	V _{IN} = 0 V, f = 1.0 MHz	30	pF

This parameter is guaranteed by design but not tested.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Pattern Data	150°C	10	Years
Retention Time	125°C	20	Years

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 3.6V, V _{IN} = GND to V _{CC}	-10	10	μA
Output Leakage Current	I _{LO}	V _{CC} = 3.6V, V _{OUT} = GND to V _{CC}	-10	10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{CS} = \overline{V_{IL}}$, OE = V _{IH} , f = 5MHz		65	mA
V _{CC} Active Current for Program or Erase (2,3)	I _{CC2}	$\overline{CS} = \overline{V_{IL}}$, OE = V _{IH} , $\overline{WE} = \overline{V_{IL}}$		120	mA
V _{CC} Standby Current (2)	I _{CC3}	$\overline{CS} = \overline{RESET} = V_{CC} \pm 0.3V$		20	μA
V _{CC} Reset Current (2)	I _{CC4}	RESET = V _{SS} ± 0.3V		20	μA
Automatic Sleep Mode (2,4)	I _{CC5}	V _{IH} = V _{CC} ± 0.3V; V _{IL} = V _{SS} ± 0.3V		20	μA
V _{CC} Active Read-While-Program Current (1,2)	I _{CC6}	$\overline{CS} = \overline{V_{IL}}$, OE = V _{IH}		180	mA
V _{CC} Active Program-While-Erase Current (1,2)	I _{CC7}	$\overline{CS} = \overline{V_{IL}}$, OE = V _{IH}		180	mA
V _{CC} Active Program-While-Erase-Suspended Current (2,5)	I _{CC8}	$\overline{CS} = \overline{V_{IL}}$, OE = V _{IH}		140	mA
Acc Accelerated Program Current	I _{ACC}	$\overline{CS} = \overline{V_{IL}}$, OE = V _{IH} Acc Pin V _{CC} Pin		40	mA
				120	
Input Low Voltage	V _{IL}		-0.5	0.8	V
Input High Voltage	V _{IH}		0.7 x V _{CC}	V _{CC} + 0.3	V
Voltage for WP/Acc Sector Protect/Unprotect and Program Acceleration	V _{HH}	V _{CC} = 3.0V + 0.3V	8.5	9.5	V
Voltage for Autoselect and Temporary Sector Unprotect	V _{ID}	V _{CC} = 3.0V + 0.3V	8.5	12.5	V
Output Low Voltage	V _{OL}	I _{OL} = 4.0 mA, V _{CC} = 3.0V		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.0 mA, V _{CC} = 3.0V	0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage (5)	V _{LKO}		2.3	2.5	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with OE at V_{IH}.
2. Maximum I_{CC} specifications are tested with V_{CC} = V_{CC} MAX
3. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30ns.
5. Not 100% tested.

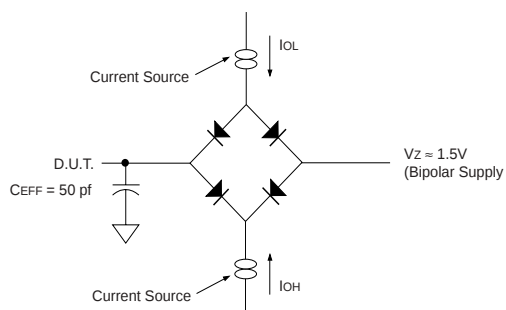


AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{CS}$ CONTROLLED ($V_{CC} = 3.3V \pm 0.3V$, $T_A = -55^\circ C$ to $+125^\circ C$)

Parameter	Symbol	-100		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV} t _{WC}	100		120		150		ns
Write Enable Setup Time	t _{WLLEL} t _{WS}	0		0		0		ns
Chip Select Pulse Width	t _{ELEH} t _{CP}	45		50		50		ns
Address Setup Time	t _{AVWL} t _{AS}	0		0		0		ns
Data Setup Time	t _{DVEH} t _{DS}	45		50		50		ns
Data Hold Time	t _{EHDX} t _{DH}	0		0		0		ns
Address Hold Time	t _{ELAX} t _{AH}	45		50		50		ns
Chip Select Pulse Width High	t _{EHLEL} t _{CPH}	30		30		30		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}		300		300		300	μs
Sector Erase Time (2)	t _{WHWH2}		15		15		15	sec
Read Recovery Time Before Write (3)	t _{GHLEL}	0		0		0		ns
Chip Programming Time (4)			108		108		108	sec

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 0.7 sec.
3. Guaranteed by design, but not tested.
4. Typical value is 36 sec. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.

FIG 2: AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - WE CONTROLLED

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	100		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	50		50		65		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	50		50		65		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	50		50		65		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	30		30		35		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}		300		300			300	μs
Sector Erase (2)	t _{WHWH2}		15		15			15	sec
Read Recovery Time before Write (3)	t _{GHWL}		0		0		0		ns
VCC Setup Time	t _{VCS}		50		50		50		μs
Chip Programming Time (4)				108		108		108	sec
Address Setup Time to $\overline{\text{OE}}$ low during toggle bit polling		t _{ASO}	15		15		15		ns
Address Hold Time From $\overline{\text{CS}}$ or $\overline{\text{OE}}$ high during toggle		t _{AHT}	0		0		0		ns
Output Enable High during toggle bit polling		t _{OEPH}	20		20		20		ns
Latency Between Read and Write Operations		t _{SR/W}	0		0		0		ns
Write Recovery Time from RY/ $\overline{\text{BY}}$		t _{RB}	0		0		0		ns
Program/Erase Valid to RY/ $\overline{\text{BY}}$		t _{BUSY}	90		90		90		ns

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 0.7 sec.
3. Guaranteed by design, but not tested.
4. Typical value is 36 sec. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

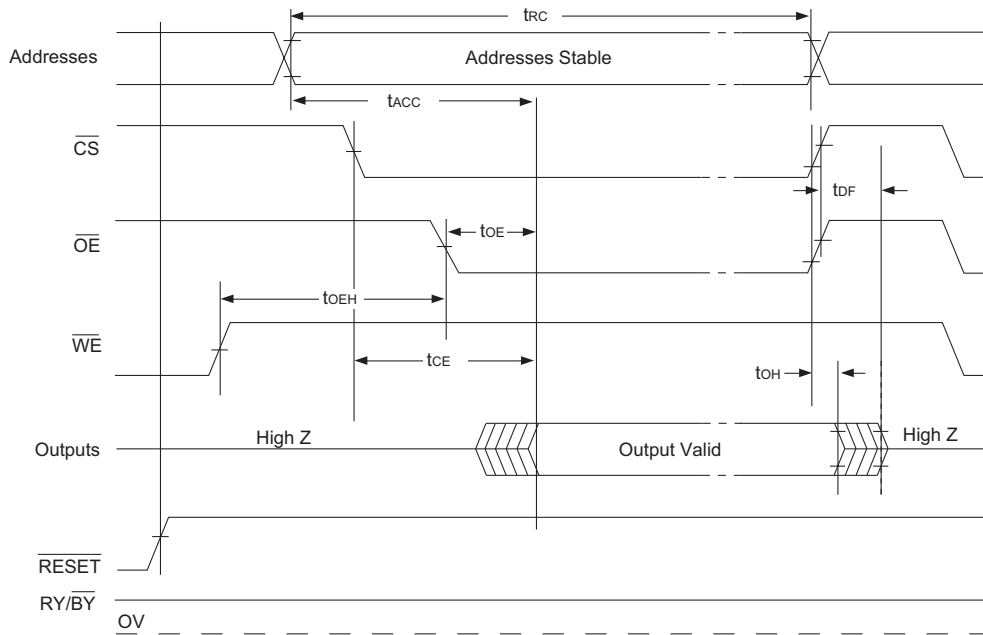
(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	100		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		100		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		100		120		150	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	t _{EHQZ}	t _{DF}		20		20		20	ns
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		20		20	ns
Output Hold from Addresses, $\overline{\text{CS}}$ or $\overline{\text{OE}}$ Change, Whichever occurs first	t _{AXQX}	t _{OH}	0		0		0		ns
Output Enable Hold Time (1)	Read	t _{OEH}	0		0		0		
	Toggle and Data Polling		10		10		10		

1. Guaranteed by design, not tested.



FIG 3: AC WAVEFORMS FOR READ OPERATIONS





AC CHARACTERISTICS – HARDWARE RESET (RESET)

Parameter	Symbol	-100		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	
RESET Pin Low (During Embedded Algorithms) to Read Mode (See Note)	t_{ready}		20		20		20	μs
RESET Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	t_{ready}		500		500		500	ns
RESET Pulse Width	t_{RP}	500		500		500		ns
RESET High Time Before Read (See Note)	t_{RH}	50		50		50		ns
RESET Low to Standby Mode	t_{RPD}	20		20		20		μs
RY/BY Recovery Time	t_{RB}	0		0		0		ns

Note: Not tested.

FIG 4: RESET TIMINGS NOT DURING EMBEDDED ALGORITHMS

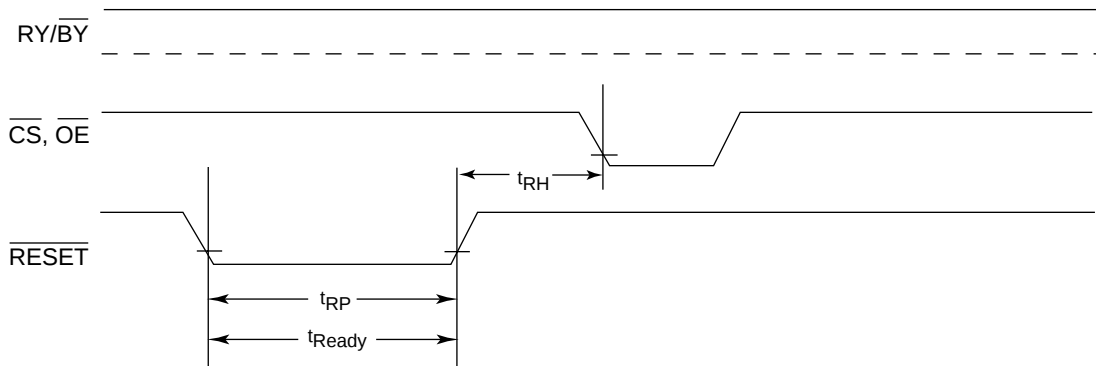


FIG 5: RESET TIMINGS DURING EMBEDDED ALGORITHMS

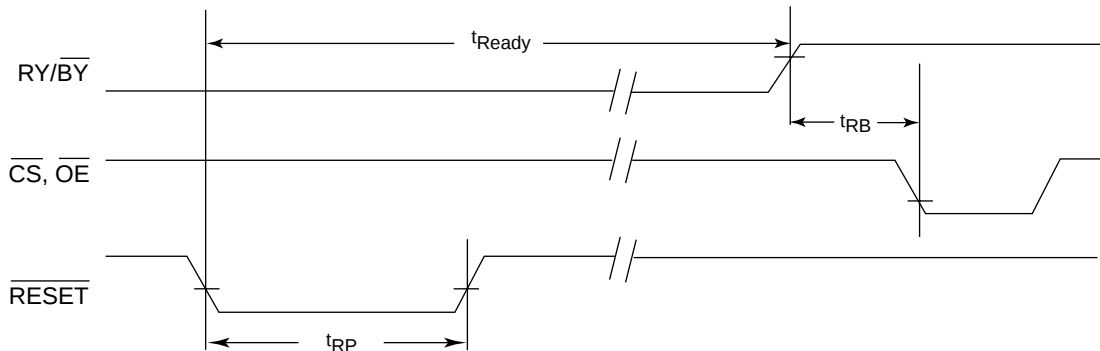
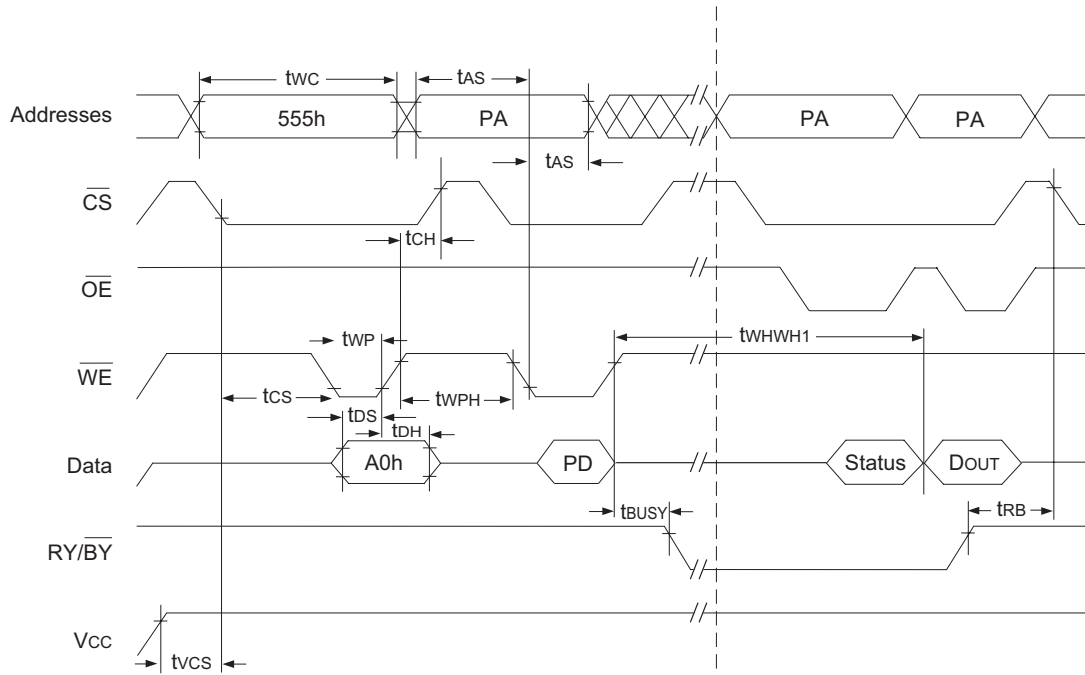




FIG 6: PROGRAM OPERATION



NOTES:

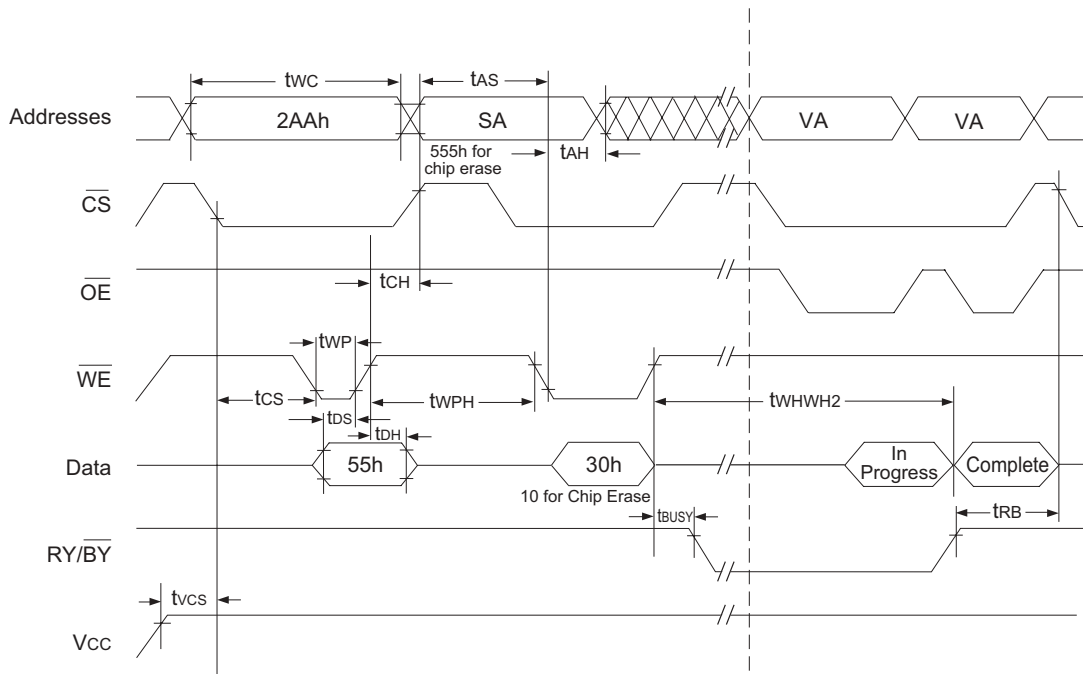
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. Dout is the output of the data written to the device.
4. Figure indicates last two bus cycles of four bus cycle sequence.



FIG 7: ACCELERATED PROGRAM TIMING DIAGRAM



FIG 8: CHIP/SECTOR ERASE OPERATION TIMINGS



Notes:

1. SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data



FIG 9: BACK TO BACK READ/WRITE CYCLE TIMINGS

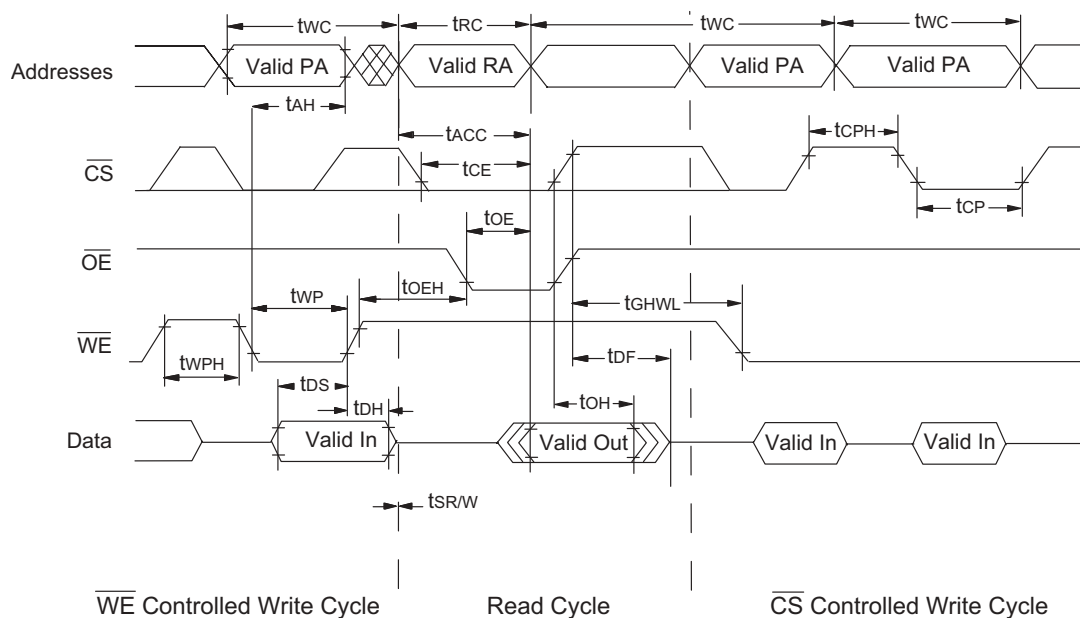
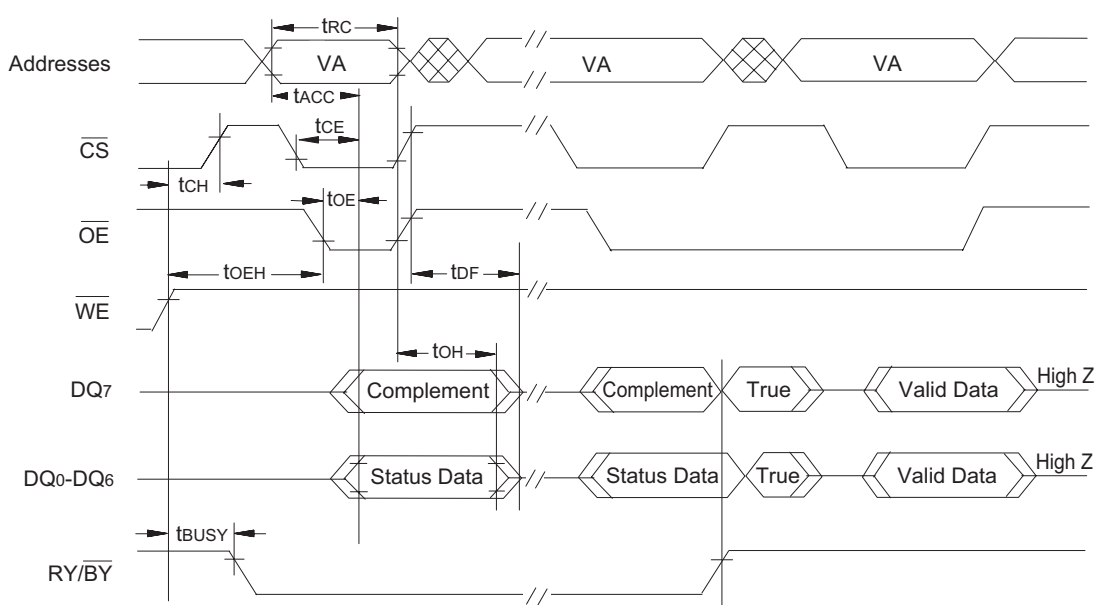


FIG. 10: DATA POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)



NOTE: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

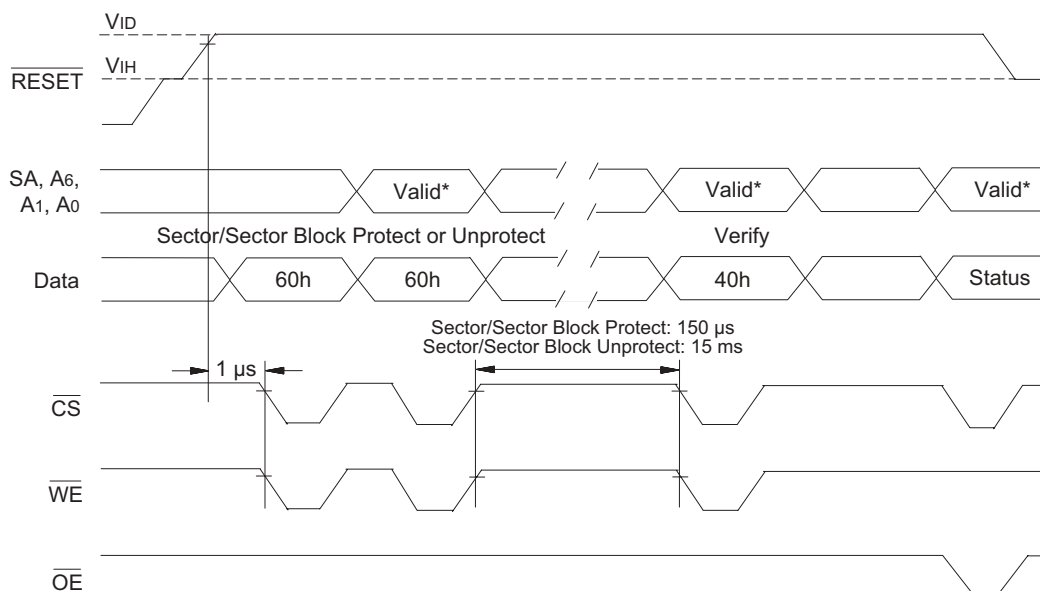
[illegible]

The timing diagram illustrates the sequence of operations for the Erase function. It features three signal lines: $\overline{WE}$, DQ6, and DQ2. The $\overline{WE}$ signal is active low and shows a series of pulses corresponding to the 'Enter Embedded Erasing' phase. The DQ6 signal shows a series of pulses during the 'Erase' phase. The DQ2 signal shows a series of pulses during the 'Erase Suspend Read' phase. The diagram is divided into several phases: 'Enter Embedded Erasing', 'Erase Suspend', 'Enter Erase Suspend Program', 'Erase Suspend Read', 'Erase Suspend Program', 'Erase Suspend Read', 'Erase Resume', and 'Erase Complete'. The 'Erase Suspend' and 'Erase Suspend Read' phases are marked with a double slash (//) indicating a break in the signal line.

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FIG 13: SECTOR/SECTOR BLOCK PROTECT AND UNPROTECT TIMING DIAGRAM



NOTES:

For sector protect, A₆ = 0, A₁ = 1, A₀ = 0. For sector unprotect, A₆ = 1, A₁ = 1, A₀ = 0.

AC CHARACTERISTICS – ALTERNATE CS CONTROLLED ERASE AND PROGRAM OPERATIONS

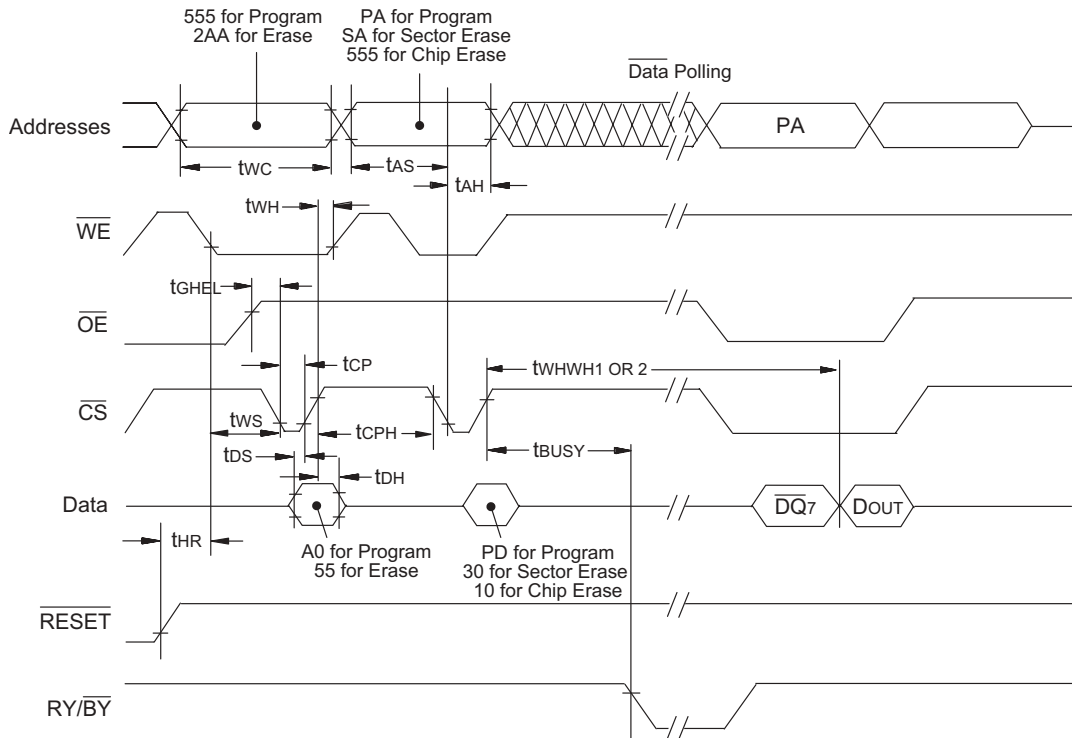
Parameter		Description		Speed Options			Unit	
JEDEC	Std			100	120	150		
t _{AVAV}	t _{WC}	Write Cycle Time (1)		Min	90	120	150	ns
t _{AVWL}	t _{AS}	Address Setup Time		Min	0	0	0	ns
t _{ELAX}	t _{AH}	Address Hold Time		Min	45	50	50	ns
t _{DVEH}	t _{DS}	Data Setup Time		Min	45	50	50	ns
t _{EHDX}	t _{DH}	Data Hold Time		Min	0	0	0	ns
t _{GHEL}	t _{GHEL}	Read Recovery Time Before Write ($\overline{\text{OE}}$ High to $\overline{\text{WE}}$ Low)		Min	0	0	0	ns
t _{WLEL}	t _{WS}	$\overline{\text{WE}}$ Setup Time		Min	0	0	0	ns
t _{EHWH}	t _{WH}	$\overline{\text{WE}}$ Hold Time		Min	0	0	0	ns
t _{ELEH}	t _{CP}	$\overline{\text{CS}}$ Pulse Width		Min	45	50	50	ns
t _{EHLE}	t _{CPH}	$\overline{\text{CS}}$ Pulse Width High		Min	30	30	30	ns
t _{WHWH1}	t _{WHWH1}	Programming Operation	Byte	Typ	9	9	9	μs
t _{WHWH1}	t _{WHWH1}	Accelerated Programming Operation, Word or Byte		Typ	7	7	7	μs
t _{WHWH2}	t _{WHWH2}	Sector Erase Operation		Typ	0.7	0.7	0.7	sec

NOTE:

1. Not tested.



FIG 14: ALTERNATE $\overline{\text{CS}}$ CONTROLLED WRITE (ERASE/PROGRAM) OPERATION TIMINGS



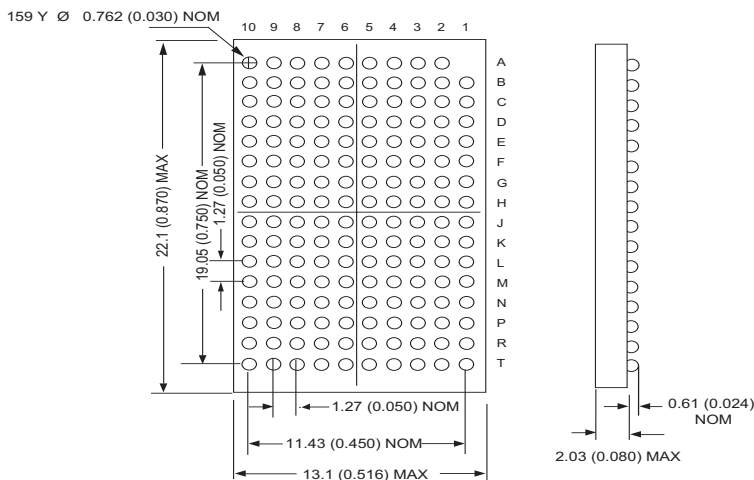
NOTES:

1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3. $\overline{\text{DQ7}}$ is the complement of the data written to the device. DOUT is the data written to the device.



PACKAGE: 159 PBGA

BOTTOM VIEW



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

ORDERING INFORMATION

WHITE ELECTRONIC DESIGNS CORP. _____

Flash _____

ORGANIZATION, 2M x 64 _____
User configurable as 2 x 2M x 32

3.3V Power supply _____

ACCESS TIME (ns) _____
100 = 100ns
120 = 120ns
150 = 150ns

PACKAGE TYPE: _____
B = 159 Plastic BGA, 13mm x 22mm

DEVICE GRADE: _____
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

W 7 2M64 V XXX B X



Document Title

2M x 64 Simultaneous Operation Flash Multi-Chip Package

Revision History

<u>Rev #</u>	<u>History</u>	<u>Release Date</u>	<u>Status</u>
Rev 0	Initial Release	November 2002	Advanced
Rev 1	Update (pg 1, 14, 15) 1.1 Change status to preliminary 1.2 Change mechanical drawing to new style	November 2003	Preliminary