# W82C485/487/489

Winbond

## High Color Graphics Palette

### DISTINCTIVE CHARACTERISTICS

- 16-bit XGA format for 64K on-screen Colors
- 15-bit TARGA format for 32K on-screen Colors
- Functionally compatible with 11C485/487/489 and W82C476/478
- Power-Down Mode
- Fast settling time and low glitch outputs for crisp displays. Glitchless "SNOW FREE" operation

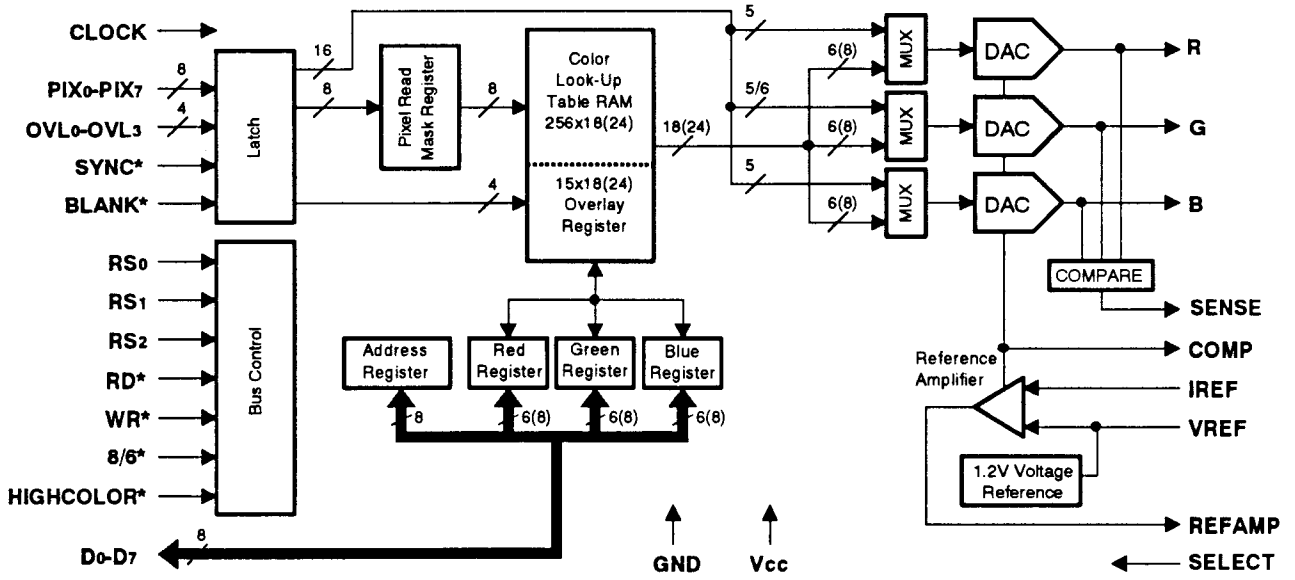
### TARGET APPLICATIONS

Graphics systems supporting 256, 32K, or 64K simultaneous color applications for DTP, Color image processing, color prepress, and MS Windows®.

Super VGA, PS/2®, 8514/a® and Macintosh® compatible display adapters with resolutions up to 1280x1024 pixels non-interlaced.

Mid- and Hi-End MS Windows® PC's, Graphics Workstations, and XWindows terminals .

### BLOCK DIAGRAM




### GENERAL DESCRIPTION

The W82C485/487/489 devices are a family of 16-bit CMOS High Color Palettes which may be used in VGA, SuperVGA, XGA or TARGA compatible video display adapters. When used in IBM XGA video display adapters, the 16-bit XGA color format data is displayed with a full 64K (65,536) simultaneous colors using the W82C485/487/489. The 15-bit TARGA format is displayed with a full 32K (32,768) simultaneous colors. In the 16-bit XGA data format, 5 bits are allocated for the Red color, 6 bits for Green, and 5 bits for blue, while TARGA allocates 5-5-5, respectively. With the W82C485/487/489 High Color Palettes, low-cost VGA/SVGA/Macintosh graphics boards can be designed that provide high resolution color displays for applications like Microsoft Windows, color pre-press, Desktop Publishing, image processing, and Multimedia. With a full 64K color display capability, users will obtain high color fidelity of displayed images, with almost "true color" quality at low cost. For backward compatibility with previous VGA software and hardware, the

W82C485/487/489 support the default 8-bit (256 color) "pseudo color" mode of typical VGA systems using the W82C476/8 or Bt476/8. With the high-speed versions available from Winbond, monitor resolutions up to 1024x768, 1280x1024 and above may be supported, with interlaced and non-interlaced refresh rates.

The superset product of the High Color Family is the W82C489. The W82C489 has triple DAC outputs selectable as 6- or 8-bit DAC resolution. In addition to the 15/16-bit High Color/XGA modes, the W82C489 has a 256x24 look-up-table RAM, allowing Windowing software and display adapters to display 256 simultaneous colors from a selection of 16.8M colors in 256-color (pseudo color) mode. The overlay registers, 15x24 may be used for cursor, text overlay, or sprite support, and provide an additional 15 simultaneous colors.

The W82C485 has all of the features of the W82C489, except the DAC outputs have a resolution of 6-bits, and the device contains a 256x18 color look-up table and a 15x18 overlay register table.

EGA and other Personal Computer display modes may be emulated, and cursors, gridlines and menus generated using the palette or 15 overlay registers on the W82C485/489. The W82C485 and W82C489 generate synch on all three video channels, support either external voltage or current references, and have a programmable pedestal (0 or 7.5 IRE).

The W82C487 is a 6-bit only device similar to the W82C485, but does not have overlay registers, or synch information on the video outputs. The W82C487 displays 256 simultaneous colors out of a palette of 256K (262,143) colors in pseudo color mode.

| | W82C485 | W82C487 | W82C489 |
|---|---|---|---|
| DAC Outputs | 6-bits only | 6-bits only | 6/8 bits |
| Overlay Register? | Yes | No | Yes |
| Programmable Pedestal? | Yes | No | Yes |
| Synch on Outputs? | Yes | No | Yes |
| Package | 44PLCC | 44PLCC & 28PDIP | 44 PLCC |

**PRODUCT QUICK QUICK SELECTOR GUIDE**

The entire W82C485/487/489 Family of products have a proprietary **Power-Down Mode** that allows the devices to be used in Laptop and Notebook computer applications requiring "sleep mode" or low power operation. To simplify the board-level design, the W82C485/487/489 include an on-chip voltage reference. To ease debugging and diagnostics a SENSE output is generated from on-chip analog comparators.

The W82C485/487/489 Family is backward-compatible with the pin-out and functionality of the Sierra 11C485/487/489 HiColor Palettes. In pseudo-color (8-bit) mode, the W82C485/487/489 is pin-out and software compatible with the Winbond W82C476/478 and Bt471/476/478 palettes. Available in versions with pixel rates as high as 80 and 100MHz, the W82C485/487/489 incorporates special proprietary circuitry to minimize output glitch energy, to minimize the DAC output settling time, and to reduce output-to-output skew. The result is a visually "crisper" and "cleaner" display on the monitor, especially at high pixel rates.

A fast microprocessor interface on the W82C485/487/489 allows for zero-Wait State interfacing to '386 and '486 microprocessors, minimizing the interface circuitry, and speeding up access to the color palettes during palette updates. A unique "**SNOW FREE**" feature minimizes corruption of the DAC outputs during simultaneous access to the palette RAM by the microprocessor and display hardware during screen refresh. Without this feature, a normal color palette would display "snow" or "hash" on the monitor during palette updates.

The W82C485/487/489 outputs may drive video monitors **without external buffers**, and the outputs are compatible with RS343A (into a doubly-terminated 75Ω load), and RS170 (into a singly-terminated 75Ω load). The W82C485/489 have programmable pedestals (0 or 7.5 IRE), and can operate with external current or voltage references.

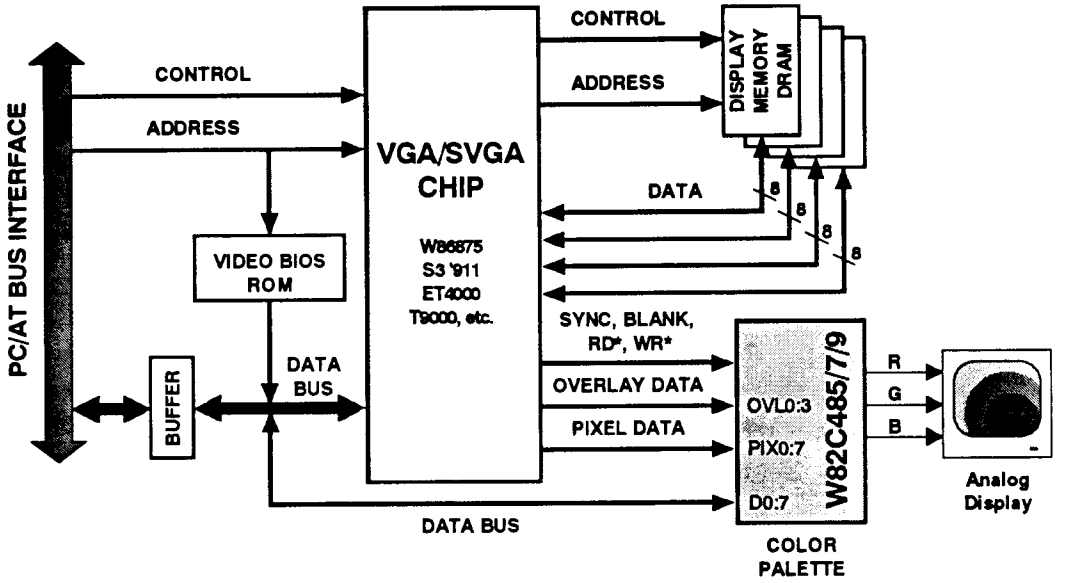



**FIGURE 1. EXAMPLE SYSTEM APPLICATION DIAGRAM**

## FUNCTIONAL DESCRIPTION

The W82C485/487/489 Color Palettes provide for the easy implementation of the color-mapping and analog circuitry required in Personal Computer (PC) and Workstation designs, with screen resolutions as high as 1024x768 and 1280x1024 pixels or greater. **FIGURE 1** shows an example PC display subsystem using the W82C485/487/489.

The look-up-table RAM translates the 8-bit pixel data in pseudo-color mode from the video frame buffer into three programmable color values for the Red, Green, and Blue DAC outputs. In High Color mode, the 15- or 16-bit data drives the DACs directly. These RS343A/RS170-compatible DAC outputs are used to drive the RGB signals to the monitor.

The functionality of the W82C485/487/489 may be divided into three sections: the **MICROPROCESSOR INTERFACE**, **DISPLAY MEMORY INTERFACE**, and the **VIDEO INTERFACE**.

### MICROPROCESSOR INTERFACE

The W82C485/487/489 has a general-purpose microprocessor bus interface which can easily connect to 8-, 16-, or 32-bit microprocessors through the 8-bit data bus and control signals. The microprocessor interface is used to read and write to the 256 color **Look-Up-Table (LUT)** RAM locations, the 15 **Overlay Registers (OLR)**, the **Pixel Read Mask Register**, the **Command Register**, and the **Address Register**. With the incorporation of a proprietary fast bus interface and special on-board logic, a microprocessor may access the W82C485/487/489 in a **single cycle** at up to 20MHz (50ns per read/write cycle). This fast bus operation allows for zero-wait-state interfacing to fast microprocessors, especially when placing the W82C485/487/489 directly on the CPU motherboard.

Read/Write access to the microprocessor interface, LUT RAM or overlay registers of the W82C485/487/489 may be completely asynchronous to the pixel clock and do not need to be synchronized to the pixel clock. Because of on-board proprietary arbitration logic, the W82C485/487/489 has **"SNOW FREE"** operation during microprocessor access: since both the microprocessor and normal operation of the display refresh may try to access the LUT RAM at the same time, the W82C485/487/489 internally arbitrates these accesses, and stabilizes the DAC outputs during microprocessor accesses, resulting in a cleaner, noise-free display during LUT updates. **"SNOW FREE"** Operation is explained in a later section (**"VIDEO INTERFACE"**).

The microprocessor interface operation is controlled by the $RS_0$-$RS_2$ control inputs, and the RD*, WR* Read/Write control inputs. The RD* signal serves as the control signal for Read operations, and the WR* signal controls Write operations. For either Read or Write cases, the falling edge of RD* or WR* begins the operations. To Read or Write to a register on the W82C485/487/489, only one RD* or WR* cycle is required, with no wait cycles required between subsequent accesses.

To read or write to the LUT RAM or OLR at a specific location, the Address Register must be loaded (written to) first as an address pointer, and then the data is read from or written to the LUT or OLR location. Operation of the Address Register and its contents is described below, and in **TABLE 3**.

The $RS_0$-$RS_2$ inputs are sampled at the beginning of a Read or Write cycle, and these signals determine the destination of the operation to be performed, as shown in **TABLE 1**.

| $RS_2$ | $RS_1$ | $RS_0$ | OPERATION |
|---|---|---|---|
| 0 | 0 | 0 | Address Pointer Register, LUT* RAM Write-Mode |
| 0 | 1 | 1 | Address Pointer Register, LUT RAM Read-Mode |
| 0 | 0 | 1 | Color Palette RAM LUT |
| 0 | 1 | 0 | Pixel Read Mask Register |
| 1 | 0 | 0 | Address Pointer Register, Overlay Write-Mode |
| 1 | 1 | 1 | Address Pointer Register, Overlay Read-Mode |
| 1 | 0 | 1 | Overlay Registers |
| 1 | 1 | 0 | Command Register |

*Note: LUT: "Look-Up-Table RAM"*

**TABLE 1. $RS_0$-$RS_2$ DECODING**

### READING COLOR LUT OR OLR DATA

In order to begin reading from any location of the 256-entry LUT RAM or Overlay Registers, an 8-bit address pointer for the desired location must first be loaded into the Address Register. This is performed by setting the $RS_0$-$RS_2$ inputs to the proper value indicated in **TABLE 1** to select the appropriate Address Register mode (Overlay Read-Mode or LUT Address Register Read-Mode). Next, the microprocessor reads three consecutive times (each time selecting the $RS_0$-$RS_2$ values to select the Color Palette RAM LUT or Overlay Registers): once each for reading the Red, Green, and Blue values in the LUT or Overlay Register location.

When the third and final Read cycle is completed, the selected Address Register is auto-incremented to point to the next location in the LUT RAM (or Overlay Register). The microprocessor may then read from this **next** location by again performing three consecutive reads for Red, Green, and Blue, or may set a new Address location through the proper Address register, repeating the process above. **TABLE 2** shows the detailed operation of the various control signals during Read/Write accesses.

### Writing Color LUT or OLR Data

Writing to any location of the 256-entry LUT RAM or Overlay Registers begins by first loading an 8-bit address pointer for the desired destination location into the proper Address Register. This is performed by setting the $RS_0$-$RS_2$ inputs to the proper value indicated in **Table 1** to select the appropriate Address Register mode (Overlay Write-Mode or LUT Address Register Write-Mode). The microprocessor then writes three consecutive times (each time selecting the $RS_0$-$RS_2$ values to select the Color Palette RAM LUT or Overlay Registers): once each for writing the Red, Green, and Blue values in the LUT or Overlay Register location.

| RD* | WR* | $RS_2$ | $RS_1$ | $RS_0$ | $AR_{A,B}$ | Function | Operation |
|---|---|---|---|---|---|---|---|
| | | | | | | **Look-Up-Table Write Sequence:** | |
| 1 | ↓ | 0 | 0 | 0 | XX | ❶ Write Address Register | D(7:0) → AR(7:0); 0 → ARa,b |
| 1 | ↓ | 0 | 0 | 1 | 00 | ❷ Write Red value | D(7:0) → Red_reg(7:0); INC(ARa,b) |
| 1 | ↓ | 0 | 0 | 1 | 01 | ❸ Write Green value | D(7:0) → Green_reg(7:0); INC(ARa,b) |
| 1 | ↓ | 0 | 0 | 1 | 10 | ❹ Write Blue value<br>Write Color LUT<br>* (internal operation) | D(7:0) → Blue_reg(7:0); 0 → ARa,b<br>Red_reg(7:0) → R(7:0); Green_reg(7:0) → G(7:0); Blue-reg(7:0) → B(7:0); INC(AR(7:0)) |
| | | | | | | **Overlay Register Write Sequence:** | |
| 1 | ↓ | 1 | 0 | 0 | XX | ❶ Write Address Register | D(7:0) → AR(7:0); 0 → ARa,b |
| 1 | ↓ | 1 | 0 | 1 | 00 | ❷ Write Red value | D(7:0) → Red_reg(7:0); INC(ARa,b) |
| 1 | ↓ | 1 | 0 | 1 | 01 | ❸ Write Green value | D(7:0) → Green_reg(7:0); INC(ARa, b) |
| 1 | ↓ | 1 | 0 | 1 | 10 | ❹ Write Blue value<br>Write Overlay<br>* (internal operation) | D(7:0) → Blue_reg(7:0); 0 → ARa, b<br>Red_reg(7:0) → R(7:0); Green_reg(7:0) → G(7:0); Blue-reg(7:0) → B(7:0); INC(AR(7:0)) |
| | | | | | | **Look-Up-Table Read Sequence:** | |
| 1 | ↓ | 0 | 1 | 1 | XX | ❶ Read Address Register | D(7:0) → AR(7:0); 0 → ARa,b |
| ↓ | 1 | 0 | 0 | 1 | 00 | ❷ Read Red value | Red_reg(7:0) → D(7:0); INC(ARa,b) |
| ↓ | 1 | 0 | 0 | 1 | 01 | ❸ Read Green value | Green_reg(7:0) → D(7:0); INC(ARa, b) |
| ↓ | 1 | 0 | 0 | 1 | 10 | ❹ Read Blue value | Blue_reg(7:0) → D(7:0); 0 → ARa, b; INC(AR(7:0)) |
| | | | | | | **Overlay Register Read Sequence:** | |
| 1 | ↓ | 1 | 1 | 1 | XX | ❶ Read Address Register | D(7:0) → AR(7:0); 0 → ARa,b |
| ↓ | 1 | 1 | 0 | 1 | 00 | ❷ Read Red value | Red_reg(7:0) → D(7:0); INC(ARa, b) |
| ↓ | 1 | 1 | 0 | 1 | 01 | ❸ Read Green value | Green_reg(7:0) → D(7:0); INC(ARa, b) |
| ↓ | 1 | 1 | 0 | 1 | 10 | ❹ Read Blue value | Blue_reg(7:0) → D(7:0); 0 → ARa, b; INC(AR(7:0)) |

*Note: ARa,b refers to internal register pointers to the Red, Green, and Blue color values at a LUT or OLR location. Please refer to timing diagrams for edge and timing information on RD* and WR*. The internal concatenation of the three 6(8)-bit values, R(7:0), G(7:0), B(7:0) refers to the 18(24-bit) word pointed to by the address register (AR).*

**Table 2. W82C485/487/489 Read/Write Access**

When the third and final Write cycle is completed, the Red, Green, and Blue values are internally concatenated into a 24-bit word (18-bits on the W82CW82C485/487), and stored into the appropriate LUT or Overlay Register location. The selected Address Register is then auto-incremented to point to the next location in the LUT RAM (or Overlay Register). The microprocessor may then write to this **next** location by again performing three consecutive writes for Red, Green

and Blue, or may set a new Address location through the proper Address register, repeating the process above. TABLE 2 shows the operation of the various control signals during Read/Write accesses.

### ADDITIONAL MICROPROCESSOR INTERFACE INFORMATION

As discussed above, the W82C485/487/489 uses an Address Register to address the LUT and Overlay Register locations. **Table 3** shows detailed operation of the Address Register bits; during access to the Overlay Registers, only the lower four bits of the Address Register are used. In order to track the three consecutive Red, Green, and Blue Read/Write cycles required for a LUT or Overlay Register Read/Write operation, an internal modulo-3 address counter (ARa,b) auto-increments after each read/write access to the LUT or Overlay Register. This internal counter is not accessible by the microprocessor. This internal counter is internally decoded to point to the proper Red, Green, or Blue value when reading and writing, and is reset to zero (pointing back to the Red value) after a write to the Address Register. The ARa,b are not reset zero after a read access.

Following a full read/write sequence to LUT location $FF (after the Blue value read/write), the Address Register is auto-incremented and set to $00. When accessing the Overlay Register (OLR), the address register auto-increments after the Blue value read/write, but the four MSB's of the Address Register (AR4-7) are ignored, and Logically wraps from $F to $0 when accessing the Overlays. At any time, the microprocessor may read the Address Register without modifying its contents or the current read/write mode, except for the special access method for the W82C487 Command Register (below).

| AR(7:0) CONTENTS | $RS_2$ | $RS_1$ | $RS_0$ | FUNCTION |
|---|---|---|---|---|
| $00..$FF | 0 | 0 | 1 | Color LUT locations $00..$FF<br>ARa,b = 00 → Red value<br>ARa,b = 01 → Green value<br>ARa,b = 10 → Blue value |
| XXXX0000b | 1 | 0 | 1 | Reserved |
| XXXX0001b | 1 | 0 | 1 | Overlay Register 1 |
| XXXX0010b | 1 | 0 | 1 | Overlay Register 2 |
| XXXX0011b | 1 | 0 | 1 | Overlay Register 3 |
| • | • | • | • | • |
| • | • | • | • | • |
| XXXX1111b | 1 | 0 | 1 | Overlay Register 15 |

TABLE 3. ADDRESS REGISTER VALUES

### W82C485/487 DATA BUS INTERFACE

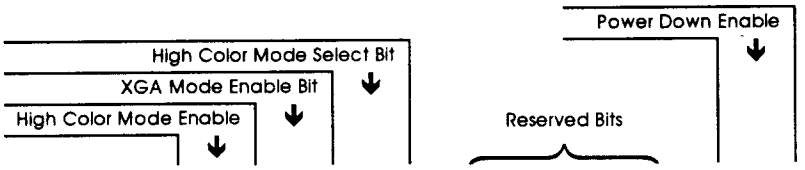
For read/write operations to the 6-bit W82C485/487 RAM LUT and Overlay Registers, and Mask Registers, the 6-bit color data from the microprocessor is contained in the six LSB's ($D_5$-$D_0$) of the data bus. The MSB Bits $D_6$ and $D_7$ are ignored during write cycles, and are set to 0 during a read cycle.

### W82C489 DATA BUS INTERFACE

On the W82C489, when the 8/6* pin is set LOW (for 6-bit operation), the data occupies the 6 LSB positions of the data bus. The MSB Bits $D_6$ and $D_7$ are ignored during write cycles in these two 6-bit cases, and are set to 0 during a read cycle. When the 8/6* pin is HIGH (for 8-bit operation), $D_0$ is the LSB of the color data, and $D_7$ is the MSB.

### COMMAND REGISTER

The Command Register is used to set the operating mode of the devices as shown below in the COMMAND REGISTER FUNCTION TABLE. The Command Register is operable in all modes, and may be written to or read by the Microprocessor at any time by applying the proper $RS_0$-$RS_2$ values. For backward compatibility with the W82C476/478 and Bt471/476/478, the Command Register is initialized to logical ZERO after power-on reset, forcing the W82C485/487/489 to function in the default 256-color Pseudo Color mode on power-on.




| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | MODE |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Pseudo Color (256 Color) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | High Color Mode 1 (32K Colors) |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | XGA Mode 1 (64K Colors) |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | High Color Mode 2 (32K Colors) |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | XGA Mode 2 (64K Colors) |
| X | X | X | X | X | X | X | 1 | Power Down Mode |

***High Color Mode Enable ($D_7$)***: *A logic ZERO in this bit enables pseudo-color mode. A Logic ONE enables High Color mode (This function is used in conjunction with bit $D_5$). Note that the HIGHCOLOR* input signal also acts in conjunction with this bit to select the color mode.*

***XGA Mode Enable ($D_6$)***: *A logic ONE in this bit enables 16-bit XGA mode (Used with $D_5$). A logic ZERO causes the device to function in 15-bit TARGA color mode.*

***High Color Mode Select ($D_5$)***: *This bit selects the timing for the $PIX_0$-$PIX_7$ inputs. If the device is in High Color Mode ($D_7$=1), a logic ZERO in this bit selects High Color Mode 1. A logic ONE selects High Color Mode 2. This bit must be a logic ZERO when High Color mode is disabled ($D_7$=0).*

***Reserved Bits ($D_4$-$D_1$)***: *Unused. These bits MUST be set to ZERO.*

***Power Down Mode ($D_0$)***: *A Logic ONE places the device in "sleep mode", turning off the video path to conserve power. The Microprocessor Interface will continue to function. A logic ZERO resumes normal operation.*

**COMMAND REGISTER FUNCTION TABLE**

#### SPECIAL COMMAND REGISTER ACCESS METHOD ON THE W82C487

The W82C487 does not have an $RS_2$ pin, so the Command Register must be accessed with a special sequence. This special access mode for the W82C487 also works properly with the W82C485 and W82C489, allowing software transparency as to which specific device is being used in the system.

1. Read the Pixel Read Mask Register ($RS_1$=1, $RS_0$=0) four consecutive times. This will set an internal flag indicating a Command Register operation.
2. The Comand Register may then be accessed as follows, for a Command Register Read or Write:
   a. **(Write)** The next write to the Pixel Read Mask Register will be redirected to the Command Register to set the Command Register contents. This terminates the sequence - any subsequent reads or writes to the Pixel Mask Register will access the Pixel Mask Register contents, not the Command Register.
   b. **(Read)** The next read from the Pixel Read Mask Register will read from Command Register contents. Any subsequent read or write to the Pixel Mask Register will access the Command Register contents.
3. The flag will be reset if there is a write to **any** address, or a read from any address other than the Pixel Read Mask Register. The flag will also be reset if any read/write access is performed to the Command Register by using the RS0-RS2 pins on the W82C485 and W82C489. The Command Register may be re-accessed by repeating (**1**) and (**2**) above. The internal flag is reset at power-on reset.

## DISPLAY MEMORY INTERFACE

In a typical system configuration (see **FIGURE 1**), the color palette is located in the path from the pixel display memory to the display monitor.

#### PSEUDO-COLOR MODE

On the W82C485/487/489, the pixel color inputs from the video display memory, $PIX_0$-$PIX_7$, and $OVL_0$-$OVL_3$, are used as addresses to the 256 locations of the Look-Up-Table RAM and the 15 Overlay Registers, respectively. These inputs are sampled on the rising edge of the pixel CLK input and are used by the color palette look-up tables to select a pixel color.

With the W82C485/487/489, the microprocessor has a method to rapidly alter the appearance of one or more colors on the display by using the pixel masking scheme. With a single write access to load the 8-bit Pixel Read Mask Register, the microprocessor can store a color masking value. With this value, the address to the LUT RAM is modified for each pixel: the $PIX_0$-$PIX_7$ inputs are logically ANDed with the contents of this register, and the resulting modified address is used to address the LUT RAM.

When the $OVL_0$-$OVL_3$ inputs are set to 0000b, the $PIX_0$-$PIX_7$ inputs (after any modification by the Pixel Read Mask Register) are used to address the LUT RAM, whose contents drive the video DACs. If a non-zero value is applied to the $OVL_0$-$OVL_3$ inputs, the DACs are driven by the contents of the addressed Overlay Registers. **TABLE 4** illustrates this operation. In this manner, using the $OVL_0$-$OVL_3$ inputs, a display system can easily implement cursors, overlay text, grids, and other overlays. Note that the $OVL_0$-$OVL_3$ inputs have no effect when the W82C485/487/489 is in High Color/XGA Mode.

The total pipeline delay times from the digital Display Inputs ($PIX_0$-$PIX_7$, $OVL_0$-$OVL_3$, SYNC*, and BLANK*) to the analog video outputs (R, G, B) in Pseudo-color mode is four pixel CLK clock cycles.

| $OVL_0$-$OVL_3$ | $PIX_0$-$PIX_7$ | Color Source Location Selected for Output to DACs |
|---|---|---|
| $0 | $00 | Color LUT RAM Location $00 |
| $0 | $01 | Color LUT RAM Location $01 |
| • | • | • |
| • | • | • |
| $0 | $FF | Color LUT RAM Location $FF |
| $1 | $XX | Overlay Register Location 1 |
| • | • | • |
| • | • | • |
| $F | $XX | Overlay Register Location 15 |

**Table 4. Pixel and Overlay Input Functions**

### High Color/XGA Modes - General Operation

When the W82C485/487/489 is placed in High Color/XGA mode, 16 bits of pixel data are taken byte-sequentially from the $PIX_0$-$PIX_7$ inputs. These two input bytes are internally concatenated to form a 15- or 16-bit word ($Z_0$-$Z_{15}$) that directly drives the three video DACs. In this mode, the Color Look Up Table, Overlay Registers, and pixel Mask Registers are bypassed.

Depending on the Color Mode, the 16-bit word ($Z_0$-$Z_{15}$) is expressed on the DACs as follows:

| | Application of 16-bit internal pixel word to DACs | | |
|---|---|---|---|
| **XGA 16-bit Format** | $Z_{15}$-$Z_{11}$ (5 bits) | $Z_{10}$-$Z_5$ (6 bits) | $Z_4$-$Z_0$ (5 bits) |
| **High Color 15-bit (Targa) Format** | $Z_{14}$-$Z_{10}$ (5 bits) | $Z_9$-$Z_5$ (5 bits) | $Z_4$-$Z_0$ (5 bits) |
| | ↓ | ↓ | ↓ |
| | Red DAC | Green DAC | Blue DAC |

*Note: The unused LSBs of the DACs are set to 0 in High Color/XGA mode.*

The timing of the sequential byte loading for the High Color mode is controlled by the Command Register (discussed above). There are two timing modes for the sequential bytes to be applied to the $PIX_0$-$PIX_7$ inputs.

### High Color/XGA Timing Mode 1

In High Color Mode 1, the two bytes are latched on opposing edges of the pixel clock, CLK. The Least Significant Byte is latched on the rising edge of the pixel clock, and the Most Significant Byte is latched on the falling edge of the pixel clock. **Figure 7b** shows that a full 16-bit word is loaded each pixel clock period. The total pipeline delay from $PIX_0$-$PIX_7$ input to DAC output is 4 CLK cycles.

### High Color/XGA Timing Mode 2

In High Color Mode 2, two subsequent pixel clocks cycles are used to load the 16 bits of information. On the first rising edge of the pixel clock, the Least Significant Byte is latched, and the second rising clock edge latches the Most Significant Byte. The sequence of LSByte/MSByte is synchronized with the BLANK* signal: the first byte latched when BLANK* goes high is the Least Significant Byte.

Because this mode requires two clock periods to load a full 16-bit data word, the input clock (CLK) must be two times the required DAC conversion rate (which is the observed video display rate). **FIGURE 7c** shows the timing relationships. To generate the correct data conversion clock from the pixel clock, the W82C485/487/489 has an internal divider. The total pipeline delay from $PIX_0$-$PIX_7$ input to DAC output is 8 CLK cycles.

## VIDEO INTERFACE

In Pseudo-Color Mode, for each cycle of the pixel clock (CLK), using the modified address formed from the $PIX_0$-$PIX_7$ and $OVL_0$-$OVL_3$ pixel inputs, a 24-bit word is read from either the LUT RAM or the Overlay Registers (an 18-bit word is read for the W82C485/487, or the W82C489 when the 8/6* input is LOW). This word value is split into three 8-bit (or 6-bit) values and converted by the three DACs into RS343A analog format. The 16-bit High Color/XGA Modes function as described above.

Note that on the W82C489, when operating in 6-bit mode (8/6* set to LOW), the full-scale output current will be about 1.5% lower than when in 8-bit mode with the same $R_{set}$ value. This is due to the loss of 2 LSBs, which are set to 0 in the 8-bit DAC outputs in 6-bit mode. One way to compensate for this is to alter the $R_{set}$ value, or adjust the voltage reference value to adjust the full-scale output.

The SYNC* and BLANK* inputs are sampled on the rising edge of CLK, and condition the RGB analog output as shown in **TABLE 5** by adding weighted currents to the outputs as shown in **FIGURE 2** and **FIGURE 3**. The SYNC* and BLANK* signals are internally delayed by four or eight pixel CLK periods (depending on the Color Mode, above), to compensate for the pipeline delay of the video stream, before conditioning the DAC outputs.

The SELECT input specifies the blanking pedestal to be used by the RGB outputs. For SELECT = logical ZERO, the blanking pedestal is 0.0 IRE; for SELECT = logical ONE, the blanking pedestal is 7.5 IRE. The W82C485/487/489 outputs are designed to individually drive up to a 37.5Ω load, such as a doubly-terminated 75Ω coaxial cable to the video display monitor, with AC coupling.

### SENSE OUTPUT

In order to allow the microprocessor to determine the presence of a CRT monitor, the W82C485/487/489 includes circuitry to detect a loaded or unloaded RGB connection. An internal comparator checks the R, G, and B outputs, and sets SENSE to logical ZERO if any one or more of the output levels exceeds the internal reference voltage level (335 mV). When using a 1.235V External Voltage Reference, this 335 mV reference has a ±5% tolerance. The tolerance is ±10% when using the Internal Voltage Reference or an External Current Reference. Note that the timing diagram in **FIGURE 5** shows that SYNC* should be logical ZERO for SENSE to be stable.

### SNOW FREE FEATURE OPERATION

When the microprocessor reads or writes to the color Look-Up-Tables or Overlay Registers during non-blanking periods, there may be a conflict with the simultaneous access of the LUT/OLR contents through the normal operation of the $PIX_0$-$PIX_7$/$OVL_0$-$OVL_3$ inputs. In other manufacturers' RAMDAC™ devices, this conflict can cause "hash" or "noise" to display on the screen. On the W82C485/487/489, a "**SNOW FREE**" feature stabilizes the DAC outputs during the microprocessor access to eliminate this visual noise. Specifically, the output of the DAC remains the same value as the last pixel value before the read/write operation began, for one CLK cycle after the Read/Write operation is completed.

| W82C485/489 WITHOUT SYNC | | W82C485/489 WITH SYNC | |
|---|---|---|---|
| mA | V | mA | V |
| 19.05 | 0.714 | 26.67 | 1.000 |
| 1.44 | 0.054 | 9.05 | 0.340 |
| 0.000 | 0.000 | 7.62 | 0.286 |
| | | 0.000 | 0.000 |

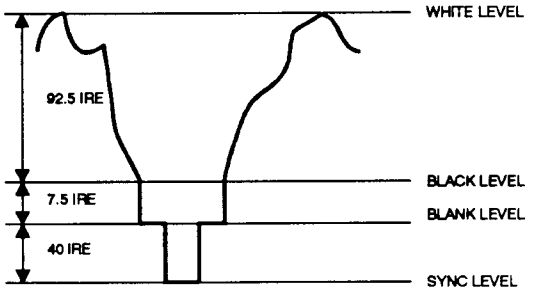



**FIGURE 2. COMPOSITE VIDEO OUTPUT SIGNALS (SELECT = $V_{CC}$)**

| W82C487 OR W82C485/489 w/o SYNC | | W82C485/489 WITH SYNC | |
|---|---|---|---|
| mA | V | mA | V |
| 17.62 | 0.660 | 25.24 | 0.950 |
| 0.000 | 0.000 | 7.62 | 0.286 |
| 0.000 | 0.000 | 0.000 | 0.000 |

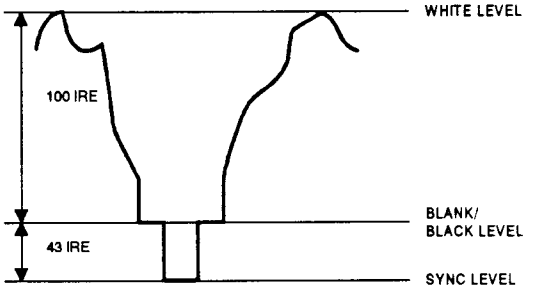



**FIGURE 3. COMPOSITE VIDEO OUTPUT SIGNALS (SELECT = GND)**

| | | | | SELECT = $V_{CC}$ | SELECT = GND | |
|---|---|---|---|---|---|---|
| DESCRIPTION | SYNC* | BLANK* | DAC INPUT DATA | $I_{OUT}$ (mA) W82C485/489 WITH SYNC | $I_{OUT}$ (mA) W82C485/489 w/o SYNC AND W82C487 | $I_{OUT}$ (mA) W82C485/489 WITH SYNC |
| WHITE | 1 | 1 | $FF | 26.67 | 17.62 | 25.24 |
| DATA | 1 | 1 | $FE..$01 | data + 9.05 | data | data + 7.62 |
| DATA-SYNC | 0 | 1 | $FE..$01 | data + 1.44 | data | data |
| BLACK | 1 | 1 | $00 | 9.05 | 0 | 7.62 |
| BLANK | 1 | 0 | $XX | 7.62 | 0 | 7.62 |
| BLACK-SYNC | 0 | 1 | $00 | 1.44 | 0 | 0 |
| SYNC | 0 | 0 | $XX | 0 | 0 | 0 |

*Note: Typical full scale Green output (G) = 26.67mA. External voltage or current reference and $R_{set}$ adjusted for 26.7mA full scale output. Typical $V_{REF}$ = 1.235V, $R_{SET}$ = 147Ω. 75Ω doubly-terminated load. Note that full-scale output may vary up to 1.5% lower on the W82C485/487 and W82C489 in 6-bit mode, due to not implementing 2LSB's (see VIDEO INTERFACE for details).*

**TABLE 5. COMPOSITE VIDEO OUTPUT TRUTH TABLE**

## PIN DESCRIPTION (GROUPED BY FUNCTION)

### MICROPROCESSOR INTERFACE SECTION

**$D_0$-$D_7$ Data and address bus (TTL Compatible Bi-directional)**
The 8-bit data bus used to read and load the internal control registers, Color Look-up Table, and Overlay Registers. Bit $D_0$ is the LSB.

**RD* Read Control Input (TTL Compatible Input)**
An active low on the RD* input initiates a read of the data from the color LUT or registers. $RS_0$-$RS_2$ are sampled and latched on the falling edge of RD*.

**WR* Write Control Input (TTL Compatible Input)**
An active low on the WR* input initiates a write of the data from the data bus to the color LUT or registers. $RS_0$-$RS_2$ are sampled and latched on the falling edge of WR*, and $D_0$-$D_7$ are sampled on the rising edge of WR*.

**$RS_0$-$RS_2$ Register Select Inputs (TTL Compatible Inputs)**
$RS_0$-$RS_2$ select the destination (Color LUT or any internal register) during a read or write cycle by the microprocessor. The value of $RS_0$-$RS_2$ determines the action performed by the read or write, as indicated in **TABLE 1**, and **TABLE 3**. $RS_2$ is not available on the W8C487.

**8/6* 8-bit/6-bit Select Input (TTL Compatible Input, Internal Pull-up Resistor)**
For the W82C489 only, the 8/6* pin controls whether 8-bits (logical ONE) or 6-bits (logical ZERO) from the data bus are used during microprocessor read and write cycles to the color LUT or Overlay Registers. In 8-bit operation, $D_7$ is the MSB, while in 6-bit operation, $D_5$ is the MSB. $D_6$ and $D_7$ are set to 00b in a 6-bit read cycle, and are ignored during a 6-bit write cycle. This pin is not implemented on the W82C485/487, and should be left No Connect on these two devices.

### TIMING SECTION

**CLK Pixel Clock (TTL Compatible Input)**
The pixel clock of the system. The rising edge of CLK latches the SYNC*, BLANK*, $PIX_0$-$PIX_7$, and $OVL_0$-$OVL_3$ inputs. The CLK input should be driven by a dedicated TTL buffer for maximum noise immunity and stability.

**BLANK* Video Composite Blank (TTL Compatible Input)**
When active (logical ZERO), the BLANK* input forces the R, G, B video outputs to the appropriate blanking levels, overriding the pixel ($PIX_0$-$PIX_7$) and Overlay ($OVL_0$-$OVL_3$) inputs, shown in **TABLE 5**. Video monitors require blanking during horizontal and vertical retrace. Blank* is sampled on the rising edge of CLK.

**SYNC* Video Synch (TTL Compatible Input)**
When active, the SYNC* input forces the R, G, and B video output current sources off, to provide SYNC pulses to the video monitor, as shown in **TABLE 5**. SYNC* should only be asserted during the blanking interval, since SYNC* does not override any other data input or control pin. This pin should be tied to GND if generation of SYNC information is not needed on the analog outputs. SYNC* is sampled on the rising edge of CLK.

## DISPLAY MEMORY INTERFACE SECTION

**$PIX_0$-$PIX_7$** **Pixel Color Data (TTL Compatible Input)**
In Pseudo Color Mode, the 8 $PIX_0$-$PIX_7$ inputs are used as addresses to select the pixel color information from one of 256 locations in the Color Palette look-up-table (LUT) RAM. In High Color/XGA Mode, $PIX_0$-$PIX_7$ are inputs for 15/16-bit color values. The $PIX_0$-$PIX_7$ values are latched on each rising edge of the pixel CLK in Pseudo Color Mode, and in High Color Mode 2. $PIX_0$-$PIX_7$ are latched on opposing edges (rising and falling edges) of the clock in High Color Mode 1. $PIX_0$ is the LSB. All unused $PIX_0$-$PIX_7$ inputs should be grounded.

**$OVL_0$-$OVL_3$** **Overlay Data (TTL Compatible Input)**
The four $OVL_0$-$OVL_3$ inputs are used to determine the overlay function, and to select which Overlay Register is used in providing the color output information, as indicated in TABLE 4. In Pseudo Color Mode, when the overlay palette is used by activating the $OVL_0$-$OVL_3$ inputs, the pixel inputs PIX0-PIX7 are ignored, and the Overlay Registers are used to drive the DACs with the OLR values. The LSB is $OVL_0$. The $OVL_0$-$OVL_3$ inputs are latched on the rising edge of each pixel CLK cycle. Any unused $OVL_0$-$OVL_3$ inputs should be grounded. In High Color/XGA Mode, the $OVL_0$-$OVL_3$ pins are ignored.

**HIGHCOLOR*** **High Color Mode Select (TTL Compatible Input)**
The logical OR of the inverse of this signal and bit $D_7$ of the Command Register determine the color mode of the W82C485/487/489. A logical ZERO selects High Color/XGA Mode, a 15 or 16-bit color mode (see COMMAND REGISTER FUNCTION TABLE). A logical ONE forces the W82C485/487/489 to 8-bit pseudo Color Mode. This pin should be tied to $V_{CC}$ to disable the High Color/XGA Modes.

## VIDEO OUTPUT SECTION

**R, G, B** *(Three Signals)* **Red, Green, Blue individual video outputs (Analog outputs)**
The three pins, R, G, B are the three high impedance analog outputs of the three video DACs, each capable of driving a doubly-terminated 75Ω RS343A cable, or a singly-terminated 75Ω RS170 cable without external buffers. All outputs have video synch outputs, and are stabilized for glitchless operation during microprocessor access to the internal registers and color palette RAM.

**$I_{REF}$** **Current Reference, Full Scale Adjust Control (Analog Input)**
The W82C485/487/489 current/voltage references for the DACs may be implemented in one of several ways, depending on the connections to this pin. The following descriptions define the EXTERNAL VOLTAGE REFERENCE mode, and EXTERNAL CURRENT REFERENCE mode.

### EXTERNAL VOLTAGE REFERENCE MODE:

A resistor, $R_{set}$ should be connected from this pin to GND when an external voltage reference is used. The $R_{set}$ resistor controls the magnitude of the full scale video output according to the following formula:

$$R_{set(\Omega)} = K * 1{,}000 * V_{REF(Volts)}/I_{OUT(mA)}$$

**EXTERNAL CURRENT REFERENCE MODE:**

If an external current reference is used, the output current ($I_{OUT}$) on each R, G, B video output is determined by the relationship:

$$I_{REF(mA)} = I_{OUT(mA)}/K$$

**REFERENCE PARAMETERS**

The table below defines the K values for doubly-terminated 75Ω loads:

| | MODE | PEDESTAL | K |
|---|---|---|---|
| **W82C489** | 6-bit | 7.5 IRE | 3.170 |
| | 8-bit | 7.5 IRE | 3.195 |
| | 6-bit | 0 IRE | 3.000 |
| | 8-bit | 0 IRE | 3.025 |
| **W82C487** | 6-bit only | 0 IRE | 2.100 |
| **W82C485** | 6-bit only | 7.5 IRE | 3.170 |
| | | 0 IRE | 3.00 |

**$V_{REF}$ Voltage Reference (Analog Input)**
When using the W82C485/487/489 with an external voltage reference, a stable 1.235V (typical) reference voltage should be supplied on this pin as a reference for the video DACs. If the W82C485/487/489 is used with an external current reference, this pin should be left floating, except for a bypass capacitor. When operating with the internal voltage reference, the $V_{REF}$ pin should be left floating except for the bypass capacitor, and should not drive any external circuitry, to reduce any induced noise on the video signal. A 0.1μF bypass/decoupling capacitor should always be connected between the $V_{REF}$ pin and $V_{CC}$, with short leads and in close proximity to the device pins.

**REFAMP Reference Amplifier Output (Analog Output)**
When using an external or internal voltage reference, this pin should be connected to the COMP pin. The REFAMP pin should be left floating if an external current reference is used.

**COMP Compensation capacitor pin (Analog Input)**
A 0.1μF ceramic decoupling capacitor should always be connected between this pin and $V_{CC}$ as close as possible to the device. When an external voltage reference is used, this pin should be connected to the REFAMP pin. When using an external current reference, this pin should be connected to $I_{REF}$.

**SELECT Select control pin (TTL compatible Input)**
The SELECT pin selects a blanking pedestal of either 0 IRE (SELECT = GND), or 7.5 IRE (SELECT = $V_{CC}$).

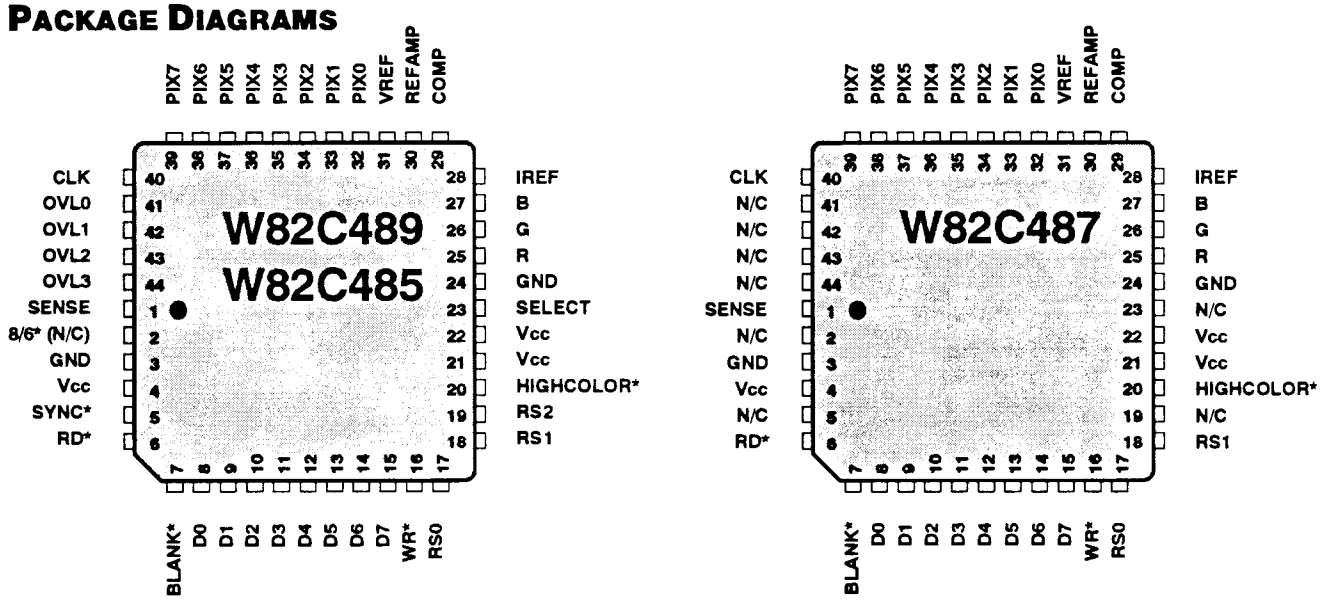
**SENSE Monitor Presence Sense (TTL compatible Input)**
As a means for the Microprocessor system to detect a load on the Red, Green, or Blue outputs, this signal is logical ZERO if any of the R, G, or B outputs exceed 335 mV. SENSE is valid when SYNC is inactive, but is not guaranteed valid when SYNC is active.

## POWER SUPPLY SECTION

**$V_{CC}$ Analog +5 Volt power supply**
All Vcc pins should be connected to +5V.

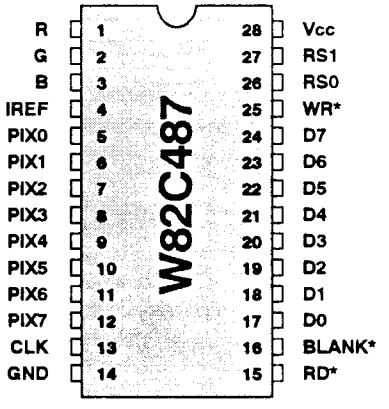
**GND Analog Ground voltage supply**
All GND pins should be connected to Ground.

## PACKAGE DIAGRAMS




*NOTE: Pin 1 is marked for orientation.*
*N/C pins may be left unconnected without affecting operation of the W82C485/487/489.*

**44-PIN J-LEAD PLASTIC (PLCC) - W82C485/487/489**
**TOP VIEW**




**28-PIN DIP (PDIP) - W82C487 ONLY**

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| **Storage Temperature** | -65 to +150°C |
| **Ambient Operating Temperature** | -55 to +125°C |
| **Junction Temperature** | +150°C |
| **Supply Voltage Measured to Ground** | -0.5 to +7.0V |
| **Voltage on any I/O pin** | GND-0.5V to $V_{CC}$+0.5V |
| **Analog Output Short Circuit to $V_{CC}$ or GND Duration** | Indefinite |
| **Soldering Temperature (5 sec, 1/4" from pin)** | 260°C |
| **Vapor Phase Soldering (1 minute)** | 220°C |

*Stresses above those listed in **ABSOLUTE MAXIMUM RATINGS** may cause permanent device damage. Functionality at or above these specification limits is not implied. Exposure to absolute maximum ratings for prolonged periods may affect device reliability.*

## RECOMMENDED OPERATING RANGE

| | |
|---|---|
| **Ambient Operating Temperature ($T_A$)** | 0 to +70°C |
| **Supply Voltage ($V_{CC}$)** | |
| For 66, 80, 100MHz devices | +4.75 to +5.25V |
| For 35, 50MHz devices | +4.5 to +5.5V |
| **Reference Voltage ($V_{REF}$)** | |
| (Voltage Reference Configuration) | +1.14 to 1.26V |
| **Current Reference ($I_{REF}$)** | |
| (Current Reference Configuration) | -3 to -10mA |
| Standard RS343A | **typical** -8.39mA |
| PS/2 Compatible | **typical** -8.88mA |
| **Output Load** | 37.5Ω |

*Recommended Operating Ranges defines the limits between which the functionality of the device is guaranteed*

## DC CHARACTERISTICS OVER OPERATING RANGE

| PARAMETER SYMBOL | PARAMETER DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | |
| $V_{IH}$ | Input High Voltage | | 2.0 | | Vcc+0.5 | V |
| $V_{IL}$ | Input Low Voltage | | GND-0.5 | | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{in}$ = 2.4V | | | 1 | μA |
| $I_{IL}$ | Input Low Current | $V_{in}$ = 0.4V | | | -1 | μA |
| $C_{IN}$ | Input Capacitance | f=1MHz; $V_{in}$ = 2.4V | | | 7 | pF |
| **DIGITAL OUTPUTS** | | | | | | |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = - 400μA | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 3.2mA | | | 0.4 | V |
| $I_{OZ}$ | 3-State Output | | | | 50 | μA |
| $C_{OUT}$ | Output Capacitance | | | | 7 | pF |

## DC Characteristics Over Operating Range (Continued)

| Parameter Symbol | Parameter Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Analog Outputs** | | | | | | |
| **Resolution:** | Each DAC, W82C485/487 (489) | | 6 (8) | 6 (8) | 6 (8) | Bits |
| **Accuracy, each DAC:** | | | | | | |
| $LIN_I$ | Integral Linearity Error, W82C485/487 (489) | | | | | |
| | W82C489 | | | | ±1 | LSB |
| | W82C487 | | | | ±½ | LSB |
| | W82C485 | | | | ±¼ | LSB |
| $LIN_d$ | Differential Linearity Error | | | | | |
| | W82C489 | | | | ±1 | LSB |
| | W82C487 | | | | ±½ | LSB |
| | W82C485 | | | | ±¼ | LSB |
| | Gray Scale Error | | | | ±5 | % Gray |
| | Monotonicity: | | | *Guaranteed* | | |
| | Coding | | | | | Binary |
| | LSB Size | | | | | |
| | W82C485/487 | | | 279.68 | | µA |
| | W82C479 | *8/6* = ONE* | | 69.1 | | µA |
| | DAC-to-DAC Matching | | | 2 | 5 | % |
| | Gray Scale Current Range | | | | 20 | mA |
| $V_{OC}$ | Output Compliance | | -1.0 | | +1.5 | V |
| $I_{VREF}$ | Voltage Reference Input Current | | | 10 | | µA |
| $R_{out}$ | Output Impedance | | | 10 | | KΩ |
| $C_{out}$ | Output Capacitance | *f=1MHz; $I_{OUT}$ = 0mA* | | | 30 | pF |
| PSSR | Power Supply Rejection Ratio | *f=1KHz; COMP = 0.1µF* | | | 0.5 | %/%$\Delta V_{CC}$ |
| **Video Output Levels - RS343A Compatibility** | | | | | | |
| | Output Current (RS343A Standard) | | | | | |
| | White Level Relative to BLANK | | 17.69 | 19.05 | 20.40* | mA |
| | White Level Relative to BLACK | | 16.74 | 17.62 | 18.50* | mA |
| | Black Level Relative to BLANK: | | | | | |
| | - W82C485/489 | *SELECT = 1* | 0.95 | 1.44 | 1.90 | mA |
| | | *SELECT = 0* | 0 | 5 | 50 | µA |
| | - W82C487 | | 0 | 0 | 0 | µA |
| | Blank Level: | | | | | |
| | - W82C485/489 | | 6.29 | 7.62 | 8.96 | mA |
| | - W82C487 | | 0 | 5 | 50 | µA |
| | Synch Level (W82C485/489 only) | | 0 | 5 | 50 | µA |

*NOTE: ***Test Conditions*** *to generate RS343A standard video signals (unless other wise specified): RECOMMENDED OPERATING CONDITIONS using external voltage reference with $R_{set}$ = 147Ω , $V_{REF}$ = 1.235V, SETUP = $V_{CC}$, 8/6* = ONE. For 28-pin DIP version of W82C487, $I_{REF}$ = -8.39mA. Since the above parameters are guaranteed over the full range, temperature coefficients are not specified or required.*

*Full-scale output levels in 6-bit DAC mode are approximately 1.5% lower than 8-bit full scale output level, due to 2 fewer LSBs (See **VIDEO INTERFACE** section).*

## AC Switching Characteristics

| Param. # | Symbol Name | Parameter Description | 120 MHz Min | 120 MHz Typ | 120 MHz Max | 80 MHz Min | 80 MHz Typ | 80 MHz Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| | $F_{max}$ | **Clock Rate** (Pseudo Color Mode) | | | 120 | | | **80** | MHz |
| | $F_{max1}$ | **Clock Rate** (High Color/XGA Mode 1) | | | | | | 50 | MHz |
| | $F_{max2}$ | **Clock Rate** (High Color/XGA Mode 2) | | | | | | 100 | MHz |
| 1 | $t_S$ | $RS_0$-$RS_2$ Setup Time | **120 MHz** | | | 10 | | | ns |
| 2 | $t_H$ | $RS_0$-$RS_2$ Hold Time | **Parameters** | | | 10 | | | ns |
| 3 | $t_P$ | RD* Asserted to Data Bus Driven | **TBD** | | | 5 | | | ns |
| 4 | $t_P$ | RD* Asserted to Data Valid | | | | | | 40 | ns |
| 5 | $t_P$ | RD* Negated to Data Bus Tri-Stated | | | | | | 20 | ns |
| 5a | | Read Data Hold Time | | | | 5 | | | ns |
| 6 | $t_S$ | Write Data Setup Time | | | | 10 | | | ns |
| 7 | $t_H$ | Write Data Hold Time | | | | 10 | | | ns |
| 8 | $t_W$ | RD*, WR* Pulse Width Low | | | | 50 | | | ns |
| 9 | $t_W$ | RD*, WR* Pulse Width High | | | | 50 | | | ns |
| | | **Pseudo Color & High Color/XGA Mode2:** | | | | | | | |
| 10 | $t_S$ | Pixel and Overlay Setup Time | | | | 3 | | | ns |
| 11 | $t_H$ | Pixel and Overlay Hold Time | | | | 3 | | | ns |
| 12 | $t_{CYC}$ | Clock Cycle Time | | | | 12.5 | | | ns |
| 13 | $t_W$ | Clock Pulse Width High | | | | 4 | | | ns |
| 14 | $t_W$ | Clock Pulse Width Low | | | | 4 | | | ns |
| | | **High Color/XGA Mode1:** | | | | | | | |
| 19 | $t_S$ | Pixel Setup Time, LSB | | | | -1.0 | | | ns |
| 20 | $t_H$ | Pixel Hold Time, LSB | | | | 7.0 | | | ns |
| 21 | $t_S$ | Pixel Setup Time, MSB | | | | -1.0 | | | ns |
| 22 | $t_H$ | Pixel Hold Time, MSB | | | | 7.0 | | | ns |
| 12 | $t_{CYC}$ | Clock Cycle Time | | | | 25 | | | ns |
| 13 | $t_W$ | Clock Pulse Width High | | | | 9 | | | ns |
| 14 | $t_W$ | Clock Pulse Width Low | | | | 9 | | | ns |
| 15 | $t_P$ | Analog Output Delay | | | | | | 30 | ns |
| 16 | $t_R$, $t_F$ | Analog Output Rise/Fall Time (Note1) | | | | | 3 | | ns |
| 17 | $t_S$ | Analog Output Settling Time (Note1) | | | | | 13 | | ns |
| | | Clock and Data Feedthrough | | | | | -30 | | dB |
| | | Glitch Impulse (Note1) | | | | | 75 | | pV-sec |
| | | DAC to DAC Crosstalk | | | | | -23 | | dB |
| | | Analog Output Skew | | | | | | 2 | ns |
| 18 | | SENSE Output Delay | | | | | 1 | | $\mu$s |
| | $I_{CC}$ | $V_{CC}$ Supply Current (Note3) | | | | | 180 | 220 | mA |
| | $I_{SB}$ | $V_{CC}$ Sleep Mode Standby Current | | | | | 3 | 5 | mA |
| Pipeline Delay (Pseudo Color & High Color/XGA Mode 1) | | | 4 | 4 | 4 | 4 | 4 | 4 | Clocks |
| Pipeline Delay (High Color/XGA Mode 2) | | | 8 | 8 | 8 | 8 | 8 | 8 | Clocks |

***Test Conditions:*** *See next Page.*

***Notes:*** *See Next Page*

## AC SWITCHING CHARACTERISTICS (CONTINUED)

| PARAM. # | SYMBOL NAME | PARAMETER DESCRIPTION | 66 MHz MIN | 66 MHz TYP | 66 MHz MAX | 50 MHz MIN | 50 MHz TYP | 50 MHz MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | $F_{max}$ | **Clock Rate** (Pseudo Color Mode) | | | **66** | | | **50** | MHz |
| | $F_{max1}$ | **Clock Rate** (High Color/XGA Mode 1) | | | 50 | | | 45 | MHz |
| | $F_{max2}$ | **Clock Rate** (High Color/XGA Mode 2) | | | 100 | | | 90 | MHz |
| 1 | $t_S$ | $RS_0$-$RS_2$ Setup Time | 10 | | | 10 | | | ns |
| 2 | $t_H$ | $RS_0$-$RS_2$ Hold Time | 10 | | | 10 | | | ns |
| 3 | $t_P$ | RD* Asserted to Data Bus Driven | 5 | | | 5 | | | ns |
| 4 | $t_P$ | RD* Asserted to Data Valid | | | 40 | | | 40 | ns |
| 5 | $t_P$ | RD* Negated to Data Bus Tri-Stated | | | 20 | | | 20 | ns |
| 5a | | Read Data Hold Time | 5 | | | 5 | | | ns |
| 6 | $t_S$ | Write Data Setup Time | 10 | | | 10 | | | ns |
| 7 | $t_H$ | Write Data Hold Time | 10 | | | 10 | | | ns |
| 8 | $t_W$ | RD*, WR* Pulse Width Low | 50 | | | 50 | | | ns |
| 9 | $t_W$ | RD*, WR* Pulse Width High | 50 | | | 50 | | | ns |
| | | **Pseudo Color & High Color/XGA Mode2:** | | | | | | | |
| 10 | $t_S$ | Pixel and Overlay Setup Time | 3 | | | 3 | | | ns |
| 11 | $t_H$ | Pixel and Overlay Hold Time | 3 | | | 3 | | | ns |
| 12 | $t_{CYC}$ | Clock Cycle Time | 15.5 | | | 20 | | | ns |
| 13 | $t_W$ | Clock Pulse Width High | 5 | | | 6 | | | ns |
| 14 | $t_W$ | Clock Pulse Width Low | 5 | | | 6 | | | ns |
| | | **High Color/XGA Mode1:** | | | | | | | |
| 19 | $t_S$ | Pixel Setup Time, LSB | -1.0 | | | -1.0 | | | ns |
| 20 | $t_H$ | Pixel Hold Time, LSB | 7.0 | | | 7.0 | | | ns |
| 21 | $t_S$ | Pixel Setup Time, MSB | -1.0 | | | -1.0 | | | ns |
| 22 | $t_H$ | Pixel Hold Time, MSB | 7.0 | | | 7.0 | | | ns |
| 12 | $t_{CYC}$ | Clock Cycle Time | 25 | | | 28 | | | ns |
| 13 | $t_W$ | Clock Pulse Width High | 9 | | | 9 | | | ns |
| 14 | $t_W$ | Clock Pulse Width Low | 9 | | | 9 | | | ns |
| 15 | $t_P$ | Analog Output Delay | | | 30 | | | 30 | ns |
| 16 | $t_R$, $t_F$ | Analog Output Rise/Fall Time (Note1) | | 3 | | | 3 | | ns |
| 17 | $t_S$ | Analog Output Settling Time (Note1) | | 15 | | | 20 | | ns |
| | | Clock and Data Feedthrough | | -30 | | | -30 | | dB |
| | | Glitch Impulse (Note1) | | 75 | | | 75 | | pV-sec |
| | | DAC to DAC Crosstalk | | -23 | | | -23 | | dB |
| | | Analog Output Skew | | | 2 | | | 2 | ns |
| 18 | | SENSE Output Delay | | 1 | | | 1 | | $\mu s$ |
| | $I_{CC}$ | $V_{CC}$ Supply Current (Note3) | | 180 | 220 | | 180 | 220 | mA |
| | $I_{SB}$ | $V_{CC}$ Sleep Mode Standby Current | | 3 | 5 | | 3 | 5 | mA |
| Pipeline Delay (Pseudo Color & High Color/XGA Mode 1) | | | 4 | 4 | 4 | 4 | 4 | 4 | Clocks |
| Pipeline Delay (High Color/XGA Mode 2) | | | 8 | 8 | 8 | 8 | 8 | 8 | Clocks |

***Test Conditions:***

***RECOMMENDED OPERATING CONDITIONS*** *unless otherwise specified.*
*External voltage reference. $R_{set}$ = 147Ω, $V_{REF}$ = 1.235V,*
*SELECT = $V_{CC}$. 8/6* = ONE. (28PDIP W82C487: $I_{REF}$ = -8.39mA)*
*TTL Input Level: 0 to 3V with $t_R$, $t_F$ (10-90%) <= 3ns.*
*Analog Output Load <= 10pF, $D_0$-$D_7$ Output Load <= 50pF.*

***Notes:***

1. *Clock and Data Feedthrough are not included.*
2. *Included Clock and data Feedthrough, -3dB bandwidth = 2x Clock Frequency.*
3. *Measured at max. $t_{clk}$: $I_{CC}$(max): $V_{CC}$ = 5.25V, $T_A$ = 0°C. $I_{CC}$(typ): $V_{CC}$ = 5.00V, $T_A$ = +25°C.*

## AC WAVEFORMS

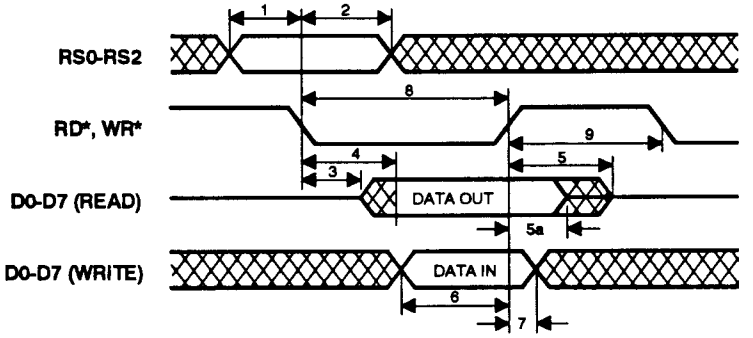
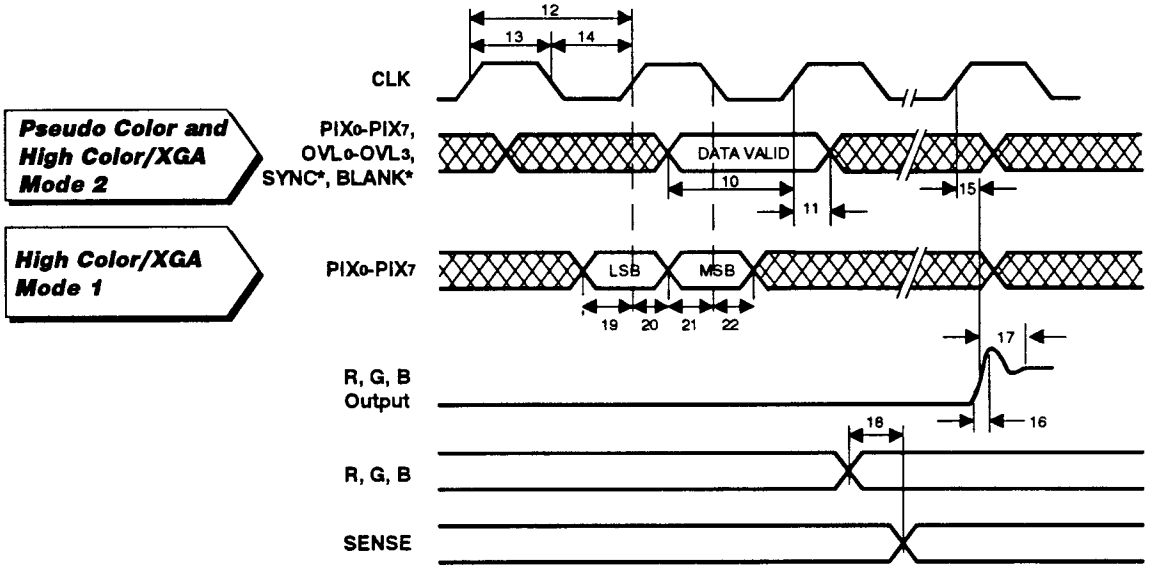
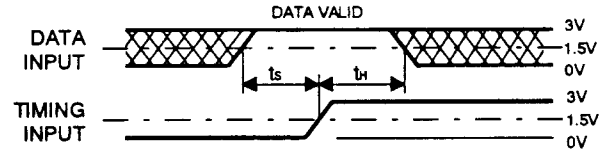



**FIGURE 4. MPU READ/WRITE TIMING**




*Notes: Output delay is measured from the 50% point of the rising edge of CLK, to the 50% point of the measured signals' full scale transition. Settling time is measured from the 50% point of the output full-scale transition, to the point where output remains within ±1 LSB(W82C489), ±1/2 LSB (W82C487), or ±1/2 LSB (W82C485). Output rise/fall time is measured between the 10% and 90% points of the full-scale transition.*

**FIGURE 5. VIDEO INPUT/OUTPUT TIMING**




*Notes: Diagram is shown for HIGH data value only. Output transition may be opposite sense. Cross-hatched areas are "Don't Care" conditions.*

**FIGURE 6. SWITCHING TEST WAVEFORM**

## AC WAVEFORMS (CONT'D)

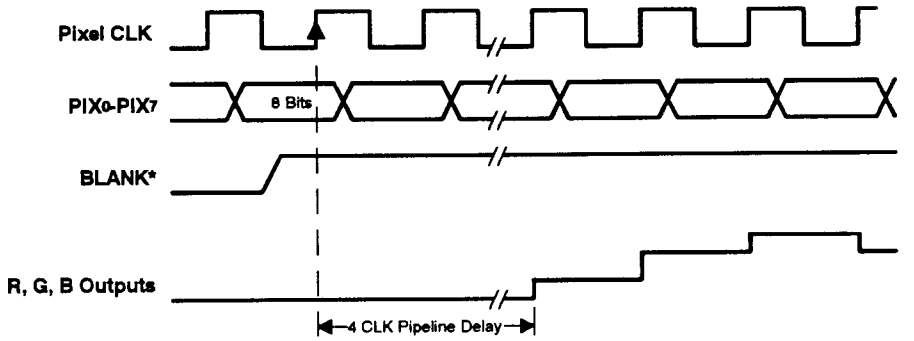



FIGURE 7A. PSEUDO-COLOR (256-COLOR) MODE TIMING

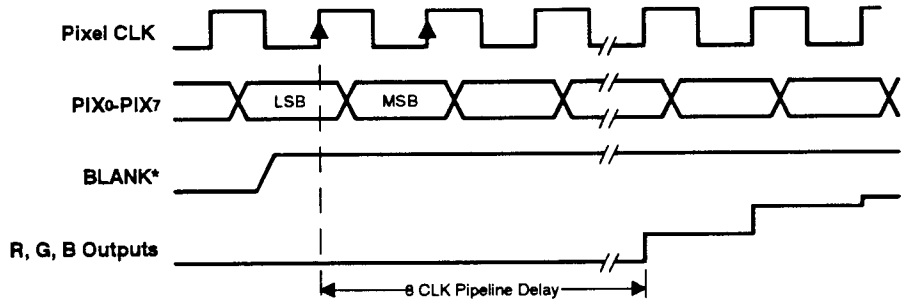



FIGURE 7B. HIGH COLOR/XGA MODE 1 TIMING

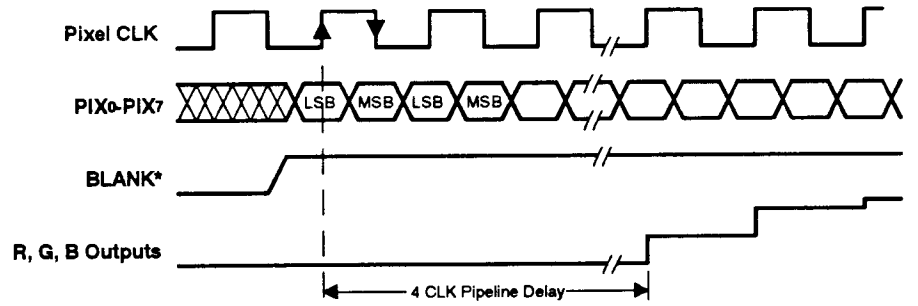



FIGURE 7C. HIGH COLOR/XGA MODE 2 TIMING

## ORDERING INFORMATION

| DEVICE PART NUMBER | SPEED | | | COLOR PALETTE SIZE | OVERLAY PALETTE | SYNC SIGNAL GENERATION | PACKAGE |
|---|---|---|---|---|---|---|---|
| | PSEUDO COLOR | HIGH COLOR MODE 1 | HIGH COLOR MODE 2 | | | | |
| W82C485P-50 | 50 MHz | 45 MHz | 90 MHz | 256 x 18 | 15x18 | yes | 44-pin PLCC, J-Lead |
| W82C485P-66 | 66 MHz | 50 MHz | 120MHz | 256 x 18 | 15x18 | yes | 44-pin PLCC, J-Lead |
| W82C485P-80 | 80 MHz | 50 MHz | 120 MHz | 256 x 18 | 15x18 | yes | 44-pin PLCC, J-Lead |
| W82C485P-120 | 120 MHz | TBD | TBD | 256 x 18 | 15x18 | yes | 44-pin PLCC, J-Lead |
| W82C487P-50 | 50 MHz | 45 MHz | 90 MHz | 256 x 18 | none | no | 44-pin PLCC, J-Lead |
| W82C487P-66 | 66 MHz | 50 MHz | 120MHz | 256 x 18 | none | no | 44-pin PLCC, J-Lead |
| W82C487P-80 | 80 MHz | 50 MHz | 120 MHz | 256 x 18 | none | no | 44-pin PLCC, J-Lead |
| W82C487P-120 | 120 MHz | TBD | TBD | 256 x 18 | none | no | 44-pin PLCC, J-Lead |
| W82C487-50 | 50 MHz | 45 MHz | 90 MHz | 256 x 18 | none | no | 28-pin, 600mil PDIP |
| W82C487-66 | 66 MHz | 50 MHz | 120MHz | 256 x 18 | none | no | 28-pin, 600mil PDIP |
| W82C487-80 | 80 MHz | 50 MHz | 120 MHz | 256 x 18 | none | no | 28-pin, 600mil PDIP |
| W82C489P-50 | 50 MHz | 45 MHz | 90 MHz | 256 x 24 | 15x24 | yes | 44-pin PLCC, J-Lead |
| W82C489P-66 | 66 MHz | 50 MHz | 120MHz | 256 x 24 | 15x24 | yes | 44-pin PLCC, J-Lead |
| W82C489P-80 | 80 MHz | 50 MHz | 120 MHz | 256 x 24 | 15x24 | yes | 44-pin PLCC, J-Lead |
| W82C489P-120 | 120 MHz | TBD | TBD | 256 x 24 | 15x24 | yes | 44-pin PLCC, J-Lead |

*Note: ALL DEVICES ABOVE ARE COMMERCIAL AMBIENT TEMPERATURE RANGE, 0°C to +70°C.*

## CIRCUIT CONNECTION RECOMMENDATIONS

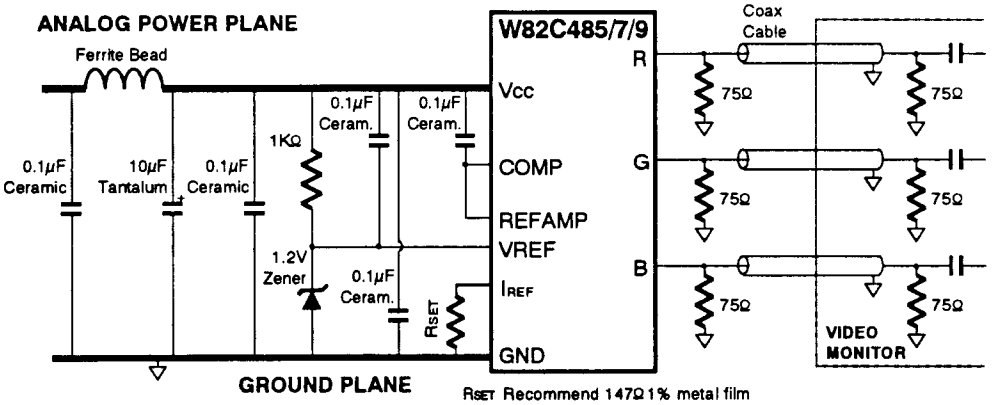



**FIGURE 8. EXAMPLE APPLICATION CIRCUIT, EXTERNAL VOLTAGE REFERENCE MODE W82C485/487/489**

## CIRCUIT CONNECTION RECOMMENDATIONS (CONT'D)

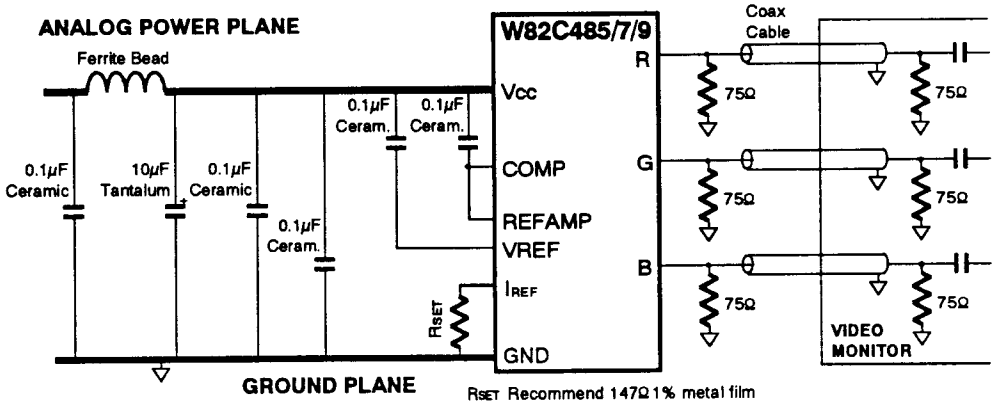



**FIGURE 9. EXAMPLE APPLICATION CIRCUIT, INTERNAL VOLTAGE REFERENCE MODE W82C485/487/489 44 PIN PLCC**

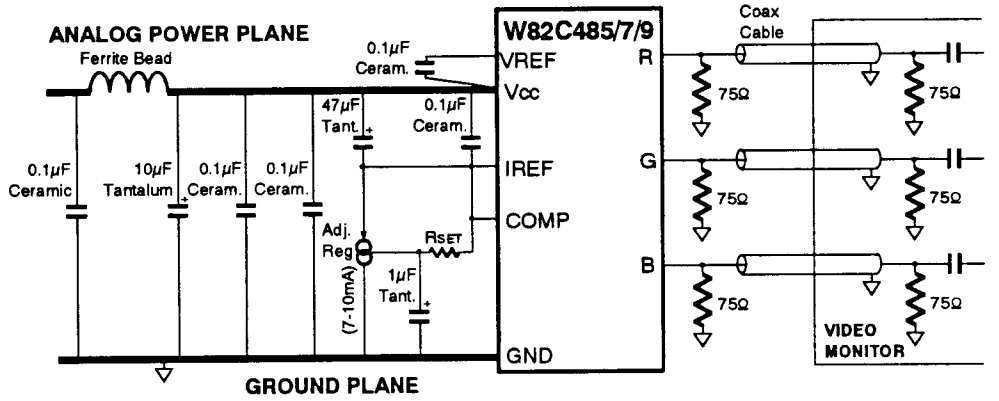



**FIGURE 10. EXAMPLE APPLICATION CIRCUIT, EXTERNAL CURRENT REFERENCE W82C485/487/489, 44 PIN PLCC**

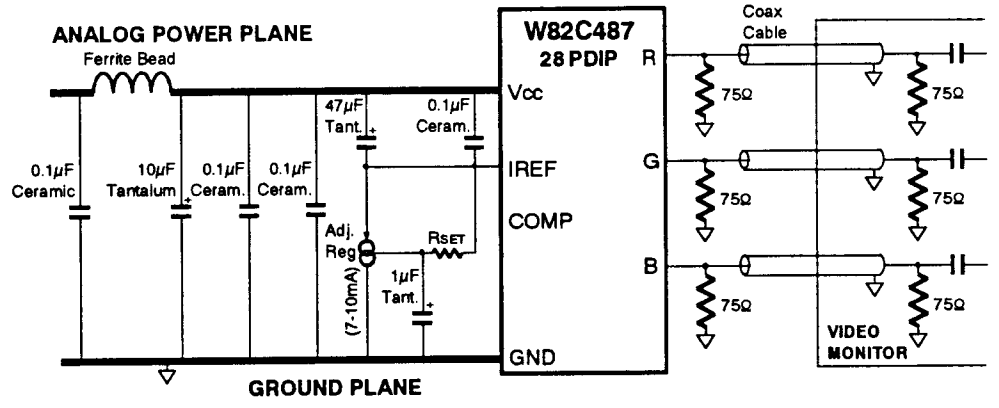



**FIGURE 11. EXAMPLE APPLICATION CIRCUIT, EXTERNAL CURRENT REFERENCE W82C487 28 PDIP ONLY**

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