



2Mx32 SRAM 3.3V MULTI-CHIP PACKAGE ADVANCED*

FEATURES

- Access Times of 12, 15, 17, 20ns
- Packaging
 - 255 PBGA, 25mm x 25mm, 625mm²
- Organized as 2Mx32
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
 - 3.3V ± 10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
 - No clock or refresh required.
- Three State Output.

* Advanced data sheet describes a product that is developmental, non-qualified and is subject to change or cancellation without notice.

PIN CONFIGURATION FOR W82M32V-XBX

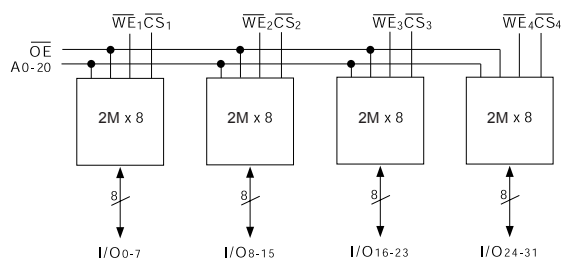
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A		NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
B	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	NC	NC	A ₂	A ₁	A ₀	GND	GND	V _{CC}	V _{CC}	A ₁₈	A ₁₇	A ₁₆	GND	NC	NC
D	NC	NC	$\overline{CS}_2$	A ₃	A ₄	D ₁₄	D ₁₅	NC	$\overline{CS}_4$	D ₂₄	D ₂₅	$\overline{OE}$	A ₁₅	NC	NC	NC
E	NC	NC	D ₉	D ₈	A ₁₉	D ₁₂	D ₁₃	GND	V _{CC}	D ₂₆	D ₂₇	$\overline{WE}_4$	D ₃₁	D ₃₀	NC	NC
F	NC	NC	D ₁₀	D ₁₁	GND	GND	GND	GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	D ₂₈	D ₂₉	NC	NC
G	NC	NC	$\overline{WE}_2$	GND	GND	GND	GND	GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	NC	NC	NC
H	NC	NC	GND	GND	GND	GND	GND	GND	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	NC	NC
J	NC	NC	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	GND	GND	GND	GND	GND	GND	NC	NC
K	NC	NC	$\overline{CS}_1$	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	GND	GND	GND	GND	GND	NC	NC	NC
L	NC	NC	D ₁	D ₀	V _{CC}	V _{CC}	V _{CC}	V _{CC}	GND	GND	GND	GND	D ₂₃	D ₂₂	NC	NC
M	NC	NC	D ₂	D ₃	A ₂₀	D ₇	D ₅	V _{CC}	GND	D ₁₇	D ₁₆	$\overline{CS}_3$	D ₂₀	D ₂₁	NC	NC
N	NC	NC	$\overline{WE}_1$	A ₆	A ₅	D ₆	D ₄	NC	$\overline{WE}_3$	D ₁₉	D ₁₈	A ₁₄	A ₁₃	NC	NC	NC
P	NC	NC	GND	A ₇	A ₈	A ₉	V _{CC}	V _{CC}	GND	GND	A ₁₀	A ₁₁	A ₁₂	V _{CC}	NC	NC
R	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
T	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₂₀	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE
(T_A = +25°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	30	pF
$\overline{WE}$ ₁₋₄ capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	10	pF
$\overline{CS}$ ₁₋₄ capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	10	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	10	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	30	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS
(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current (x 32 Mode)	I _{CC} x 32	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 3.6V		1100	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 3.6V		400	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V.

NOTE: Contact factory for low power option.

**AC CHARACTERISTICS**
(VCC = 3.3V, TA = -55°C to +125°C)

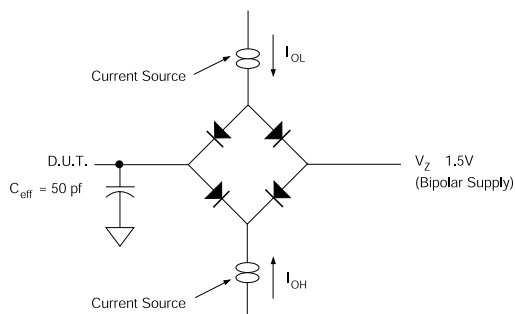
Parameter	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read Cycle Time	t _{RC}	12		15		17		20		ns
Address Access Time	t _{AA}		12		15		17		20	ns
Output Hold from Address Change	t _{OH}	3		3		3		3		ns
Chip Select Access Time	t _{ACS}		12		15		17		20	ns
Output Enable to Output Valid	t _{OE}		7		8		8		10	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	1		1		1		1		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		7		8		8		10	ns
Output Disable to Output in High Z	t _{OHZ} ¹		7		8		8		10	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(VCC = 3.3V, TA = -55°C to +125°C)

Parameter	Symbol	-12		-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle										
Write Cycle Time	t _{WC}	12		15		17		20		ns
Chip Select to End of Write	t _{CW}	10		12		12		14		ns
Address Valid to End of Write	t _{AW}	10		12		12		14		ns
Data Valid to End of Write	t _{DW}	8		9		9		10		ns
Write Pulse Width	t _{WP}	10		12		14		14		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	2		2		3		3		ns
Write Enable to Output in High Z	t _{WHZ} ¹		7		8		8		9	ns
Data Hold Time	t _{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

V_Z is programmable from -2V to +7V.

I_{OL} & I_{OH} programmable from 0 to 16mA.

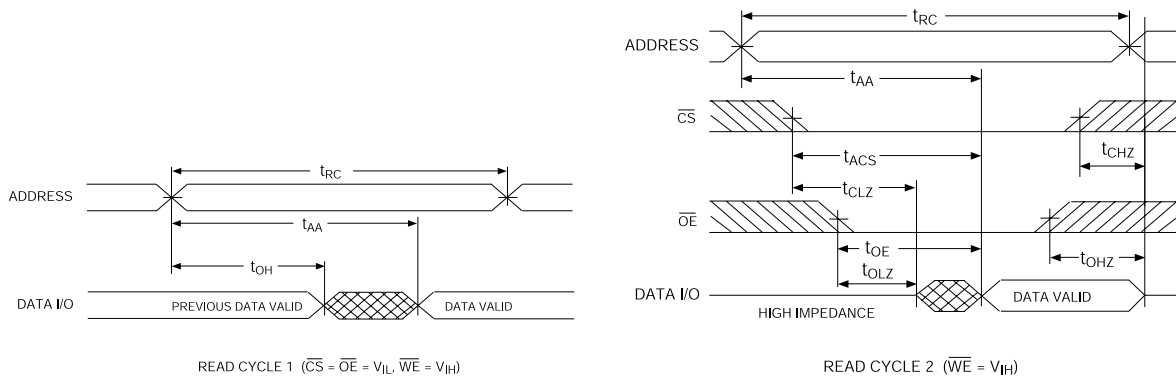
Tester Impedance Z₀ = 75 W.

V_Z is typically the midpoint of V_{OH} and V_{OL}.

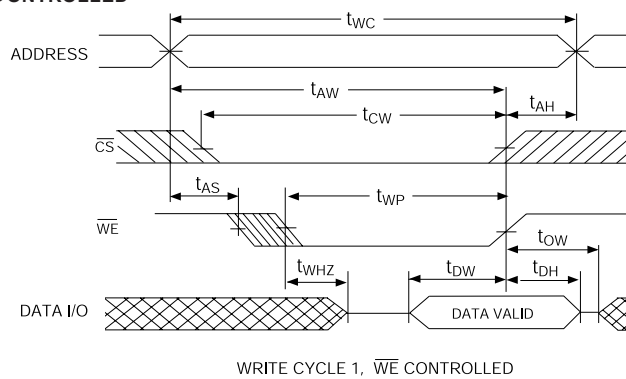
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit. ATE tester includes jig capacitance.



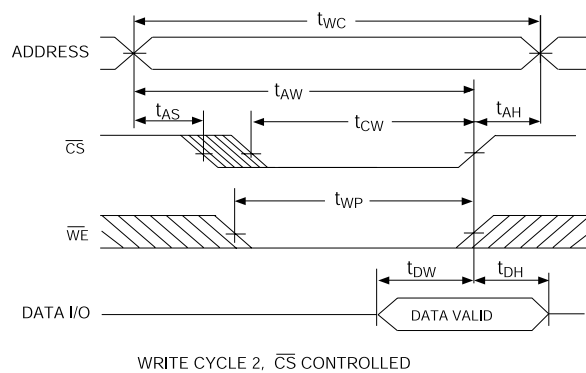
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - $\overline{WE}$ CONTROLLED



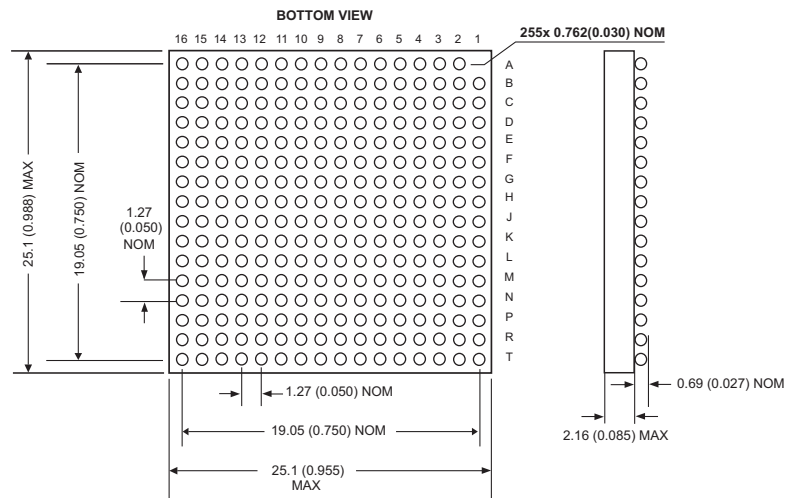
WRITE CYCLE - $\overline{CS}$ CONTROLLED





PACKAGE 781: 255 BALL GRID ARRAY

ADVANCED*



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**Note: Advanced Product. This product is developmental, is not qualified, and is subject to change or cancellation without notice.*



ORDERING INFORMATION

W 8 2M 32 V - XX X X

DEVICE GRADE:

M = Military -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:

B = 25mm x 25mm, 255 PBGA

ACCESS TIME (ns)

Low Voltage Supply 3.3V ± 10%

ORGANIZATION, 2Mx32

User configurable as 4Mx16 or 8Mx8

SRAM

WHITE ELECTRONIC DESIGNS CORP.

**Document Title**

2M x 32 Asynchronous SRAM

Revision History

<u>Rev #</u>	<u>History</u>	<u>Release Date</u>	<u>Status</u>
Rev 0	Initial Release	July 2002	Advanced
Rev 1	Changes 1.1 Add AC/DC Electricals & Timing Diagrams (Pg. 1-7) 1.2 Change Pinout to full 255 (16x16) array 1.3 Change Package Dimension to full 255 (16x16) array	October 2002	Advanced
Rev 2	Changes (Pg.1,5,6,7) 1.1 Change package dimension from 27mm square to 25mm square 1.2 Change package height from 2.20mm to 2.70mm Max	May 2002	Advanced
Rev 3	Changes (Pg.1,5,7) 1.1 Change package mechanical drawing to new format.	November 2003	Advanced