Winbond Electronics Corp.

DDR/SDRAM BUFFER

W83196R-718

Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a	02/July	1.0	1.0	Change version and version on web site to 1.0
3					
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

1.0 GENERAL DESCRIPTION

The W83196R-718 is a 2.5V/3.3V Clock buffer. W83196R_718 can support 4 D.D.R. DRAM DIMMs or 3 standard SDRAM and 2 D.D.R. DRAM DIMMs.

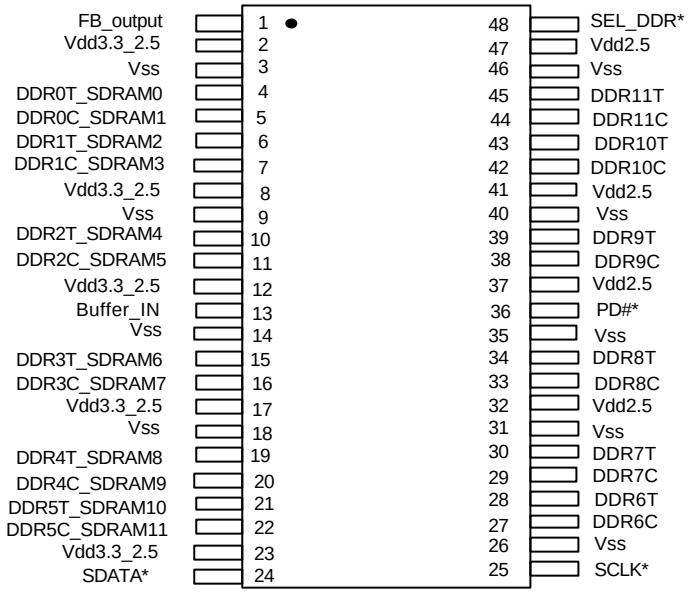
W83196R-718 can be incorporated with W83194BR-P4X or W83194BR-325.

The W83196R_718 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs. The W83196R_718 accepts a reference clock as its input and runs on a 3.3V or 2.5V supply.

2.0 PRODUCT FEATURES

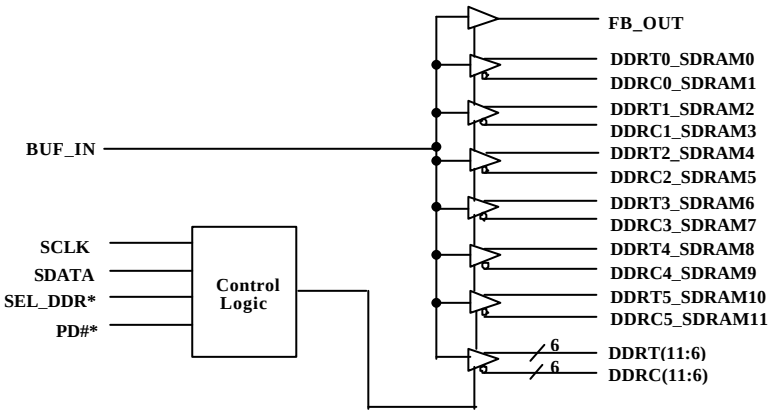
- One input to 24 outputs buffer
- Supports up to 4 D.D.R. DIMMs or 3 SDRAM DIMMs and 2 D.D.R. DIMMs
- One additional output for feedback
- Low Skew outputs (< 100ps)
- Supports up to 200MHz D.D.R. SDRAM
- I^2C 2-Wire serial interface and supports Byte or Block Date RW
- Power management pin for power down control
- 48-pin SSOP package

3.0 PIN CONFIGURATION



*: Internal pull-up resistor 120K to Vdd3.3_2.5
#: Active low

Block Diagran



4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

*- Internal 120kΩ pull-up

4.1 Pin Description

SYMBOL	PIN	I/O	FUNCTION
SEL_DDR	48	IN	1= DDR only mode 0=Standard SDRAM mode When SEL_DDR is pulled high. Pin 4,5,6,7,10,11,15, 16,19,20,21,22,27,28,29,30,33,34,38,39,42,43,44 and 45 will be D.D.R. outputs. Vdd3.3_2.5 should be connected to 2.5V for DDR power supply. When SEL_DDR is pulled low. Pin 4,5,6,7,10,11,15,16,19, 20,21 and 22 will be standard SDRAM outputs. Pin 27,28,29,30,33,34,38,39,42,43,44 and 45 will be DDR outputs, Vdd3.3_2.5 should be connected to 3.3V for SDRAM.
SDATA*	24	I/O	Serial data of I^2C 2-wire control interface Internal pull-up resistor 120K to Vdd3.3_2.5
SCLK*	25	IN	Serial clock of I^2C 2-wire control interface Internal pull-up resistor 120K to Vdd3.3_2.5
Buffer_IN	13	IN	Reference input from chipset. 2.5V input for DDR only mode. 3.3V for standard SDRAM mode.
FB_output	1	OUT	Feedback clock for chipset. Output voltage depends on Vdd3.3_2.5
PD#*	36	IN	Active LOW input to enable Power Down mode and all outputs will be Three-Stated Internal pull-up resistor 120K to Vdd3.3_2.5
DDR[6:11]T	28,30,34,39,43, 45	OUT	Clock outputs. Copies of Buffer_IN.
DDR[6:11]C	27,29,33,38,42, 44	OUT	Complementary copies of Buffer_IN
DDR[0:5]T_SDRAM [0,2,4,6,8,10]	4,6,10,15,19, 21	OUT	Clock outputs. SEL_DDR=1, these pins are copies of Buffer_IN. SEL_DDR=0, these pins are copies of Buffer_IN. Voltage dpends on the Vdd3.3_2.5

DDR[0:5]C_SDRAM [1,3,5,7,9,11]	5,7,11,16,20 22	OUT	Clock outputs. SEL_DDR=1, these pins are complementary copies of Buffer_IN. SEL_DDR=0, these pins are copies of Buffer_IN. Voltage dpends on the Vdd3.3_2.5

4.5 Power Pins

SYMBOL	PIN	FUNCTION
Vdd3.3_2.5	2,8,12,17,23	Connected to 2.5V when SEL_DDR=1 and 3.3V when SEL_DDR=0
Vdd2.5	32,37,41,47	Power supply 2.5V.
Vss	3,9,14,18,26,31,35, 40,46	Ground

5.1 Register 6 : Control Register (default = 1)

Bit	@PowerUp	Pin	Description
7	1	48	SEL_DDR (Read back only)
6:5	11	-	Reserved for winbond internal use, do not change them
4	1	-	When the pin is low –level, Pin 27,28,29,30,32,33,34,,38,39,42,43 ,44,45 will be Three-Stated in the SDRAM Mode.
3	1	45,44	DDR11T,DDR11C(Active / Inactive)
2	1	43,42	DDR10T,DDR10C(Active / Inactive)
1	1	39,38	DDR9T,DDR9C(Active / Inactive)
0	1	34,33	DDR8T,DDR8C(Active / Inactive)

5.2 Register 7: Control Register (1 = enable, 0 = Stopped)

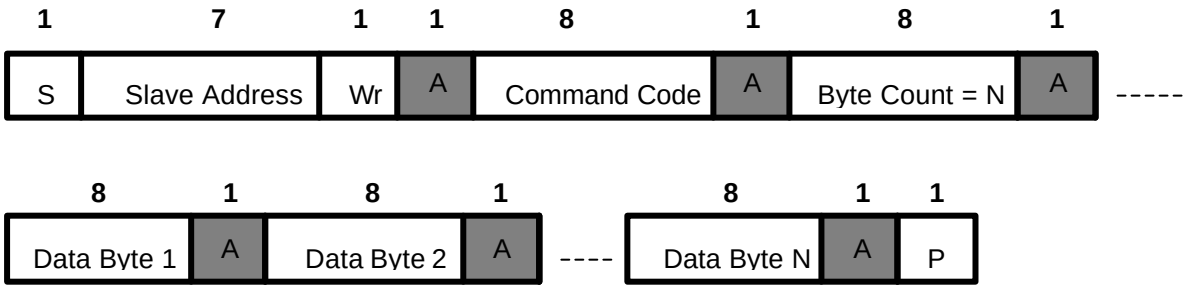
Bit	@PowerUp	Pin	Description
7	1	30,39	DDR7T,DDR7C(Active / Inactive)
6	1	28,27	DDR6T,DDR6C(Active / Inactive)
5	1	21,22	DDR5T_SDRAM10, DDR5C_SDRAM11(Active / Inactive)
4	1	19,20	DDR4T_SDRAM8, DDR4C_SDRAM9 (Active / Inactive)
3	1	15,16	DDR3T_SDRAM6, DDR3C_SDRAM7 (Active / Inactive)
2	1	10,11	DDR2T_SDRAM4,

			DDR2C_SDRAM5 (Active / Inactive)
1	1	6,7	DDR1T_SDRAM2, DDR1C_SDRAM3 (Active / Inactive)
0	1	4,5	DDR0T_SDRAM0, DDR0C_SDRAM1(Active / Inactive)

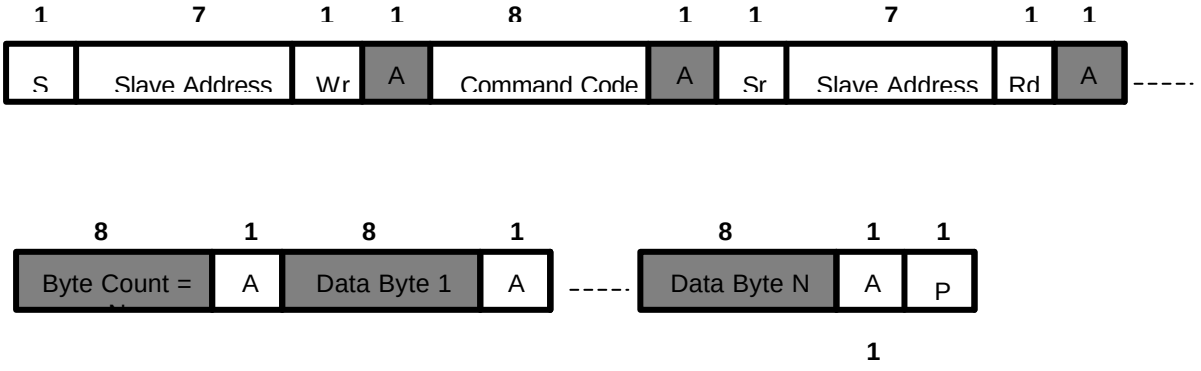
6. ACCESS INTERFACE

The W83196R-718 provides I²C Serial Bus for microprocessor to read/write internal registers. In the W83196R-718 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I²C address is defined at 0xD2.

6.1 Block Write protocol

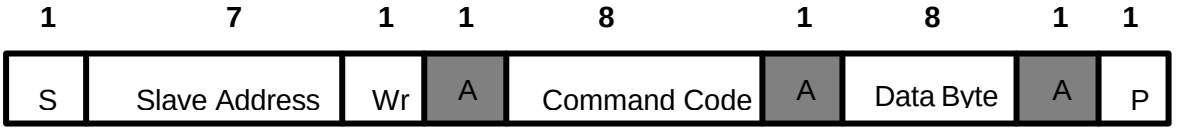


6.2 Block Read protocol

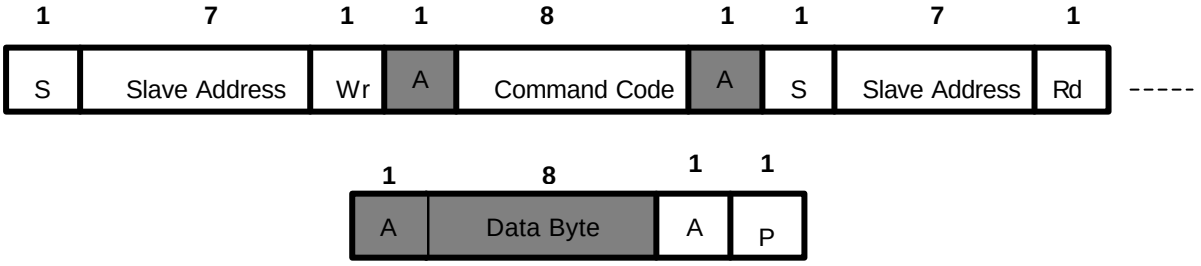


In block mode, the command code must filled 8' h00

6.3 Byte Write protocol



6.4 Byte Read protocol



6.5 The serial bus access timing

(a) Serial bus writes to internal address register followed by the data byte.

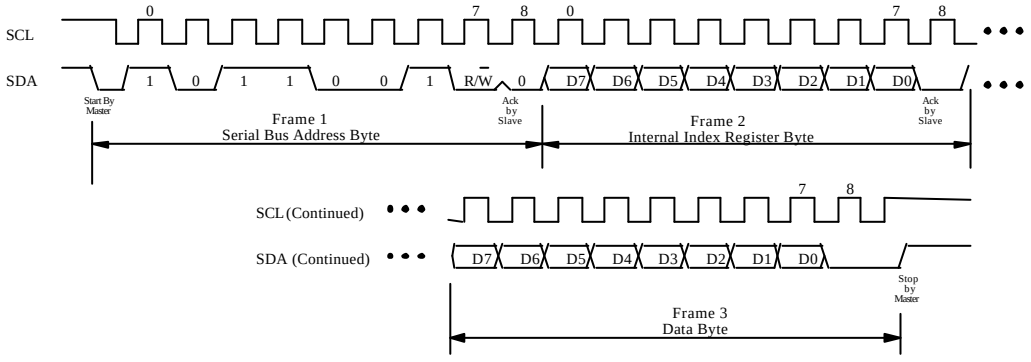


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus writes to internal address register only

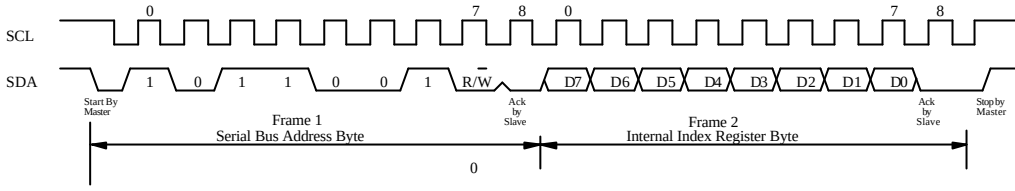


Figure 2. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location.

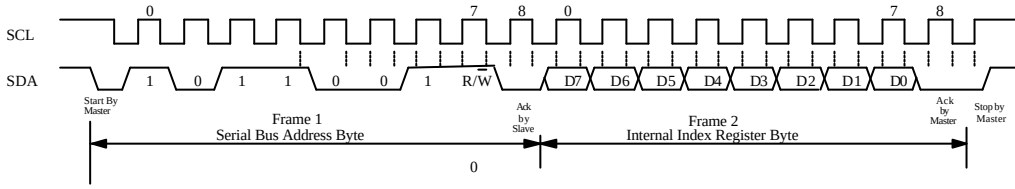


Figure 3. Serial Bus Read from Internal Address Register

(d) Serial bus read from a register with writing to internal address register.

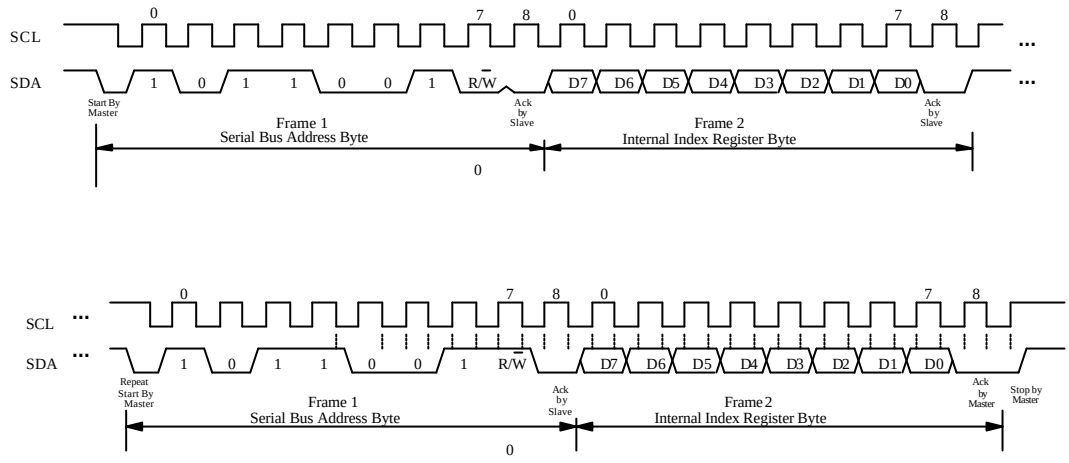
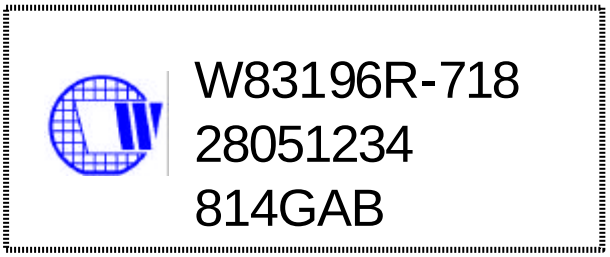


Figure 4. Serial Bus Read from Writing Internal Address Register

7.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83196R_718	48 PIN SSOP	Commercial, 0°C to +70°C

8.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83196R-196

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

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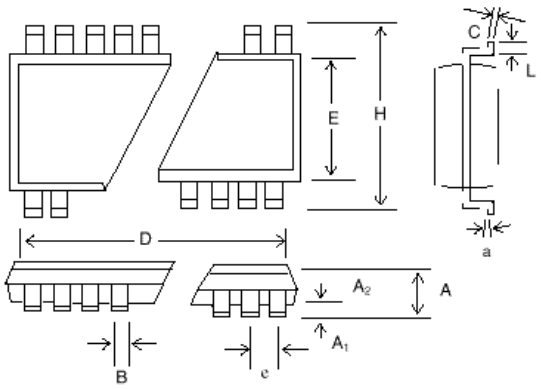
9.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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