SBE D

CMOS Peripheral Circuits

CDP1800-Series and CDP6805-Series Peripherals (Continued)

Input Levels: CMOS for All Types

| Туре | Description and Function | Features | Operating Voltage Range Volts | Operating Temp Range (T _A)† | Fanout (TTL Loads) | No. of Pins* Package |
|---------------------|--|---|--|---|--------------------------|----------------------------|
| | | | | | | |
| CDP6818 | Real-Time Clock with RAM (MOTEL Bus)** | Low-power, high-speed CMOS Internal time base and oscillator Counts seconds, minutes and hours of the day Counts days of the week, date, month and year | 3 to 6 | 0 to +70 | 1 | 24 D E |
| CDP6818A | | Time base input options: ▶ 1.048576MHz ▶ 32.768kHz Time base oscillator for parallel resonant crystals 40 to 200µW typical operating power at low frequency time base 4.0 to 20mW typical operating power at high frequency time base Binary or BCD representation of time, calendar and alarm 12 or 24 hour clock with AM and PM in 12 hour mode Daylight savings time option Automatic end of month recognition Automatic leap year compensation Microprocessor bus compatible Selectable between Motorola and competitor bus timing Multiplexed bus for pin efficiency Interfaced with software as 64 RAM locations 14 bytes of clock and control registers 50 bytes of general purpose RAM Status bit indicates data integrity Bus compatible interrupt signals (IRQ) Three interrupts are separately software maskable and testable Time-of-day alarm, Once-per-second to Once-per-day Periodic rates from 30.5µs to 500ms End-of-clock update cycle Programmable square-wave output signal Clock output may be used as microprocessor clock input at time base frequency ÷ 1 or ÷ 4 | | | | 24 D E 28 Q |
| INTERRUPT | CONTROLLER | at time sees inequality | <u> </u> | | | |
| CDP1877 CDP1877C | Programmable Interrupt Controller (PIC) | Compatible with CDP1800-series Programmable long branch vector address and vector interval Blevels of interrupt per chip Easily expandable Latched interrupt requests Hard wired interrupt priorities Memory mapped Multiple chip select inputs to minimize address space requirements | 4 to 10.5 4 to 6.5 | -40 to +85 | 1 | 28 D E |

[†] TA indicates operating temperature range over which the published electrical data are specified * See interpretation guide and packaging section

^{**} MOTEL Bus not included in 'A' version