CDP1800-Series and CDP6805-Series Peripherals

Family Features

- CMOS Static Operation
- Compatible With Many Industry-Standard Microprocessors and Microcomputers, CMOS & NMOS
- Wide Variety of I/O Functions
- 36 I/O Configurations
- Programmable I/Os
- Byte-Wide Latches
- Decoders
- UARTs and ACIAs
- Multiply-Divide Units (MDUs)
- Buffers
- Counters
- Clocks
- Video Interface
- Interrupt Controllers
- Serial Peripheral Interface (SPI) Circuits

Input Levels: CMOS for All Types

Type	Description and Function	Features	Operating Voltage Range Volts	Operating Temp Range (T_A) † °C	Fanout (TTL Loads)	No. of Pins* Package
I/O PORTS						
CDP1851 CDP1851C	Programmable I/O Interface	• 20 Programmable I/O lines • Programmable for operation in four modes: ▶ Input ▶ Bidirectional ▶ Output ▶ Bit-Programmable • Operates in either I/O or memory space	4 to 10.5 4 to 6.5	-40 to +85	1	40 D E
CDP1852 CDP1852C	Byte-Wide Input/Output Port	• Static silicon-gate CMOS circuitry • Parallel 8-bit data register and buffer • Handshaking via service request flip-flop • Low quiescent and operating power • Interfaces directly with CDP1800-series µPs • Single voltage supply • Full military temperature range: (-55°C to +125°C)	4 to 10.5 4 to 6.5	-40 to +85	1	24 D E
CDP1872 CDP1872C CDP1874C	High-Speed 8-Bit Input Port	• Parallel 8-bit I/O register with buffered outputs • High-speed data-in to data-out: ▶ 85ns (max) at V_{DD} = 5V • Flexible applications in µP systems as buffers & latches • High order address-latch capability in CDP1800 series µP systems • Output sink current = 5mA (min) at V_{DD} = 5V • Three-state output	4 to 6.5	-40 to+85	3	22 D E
CDP1875C	High-Speed 8-Bit Output Port	• Parallel 8-bit input/output register with buffered outputs • High-speed data-in to data-out: ▶ 85ns (max) at V_{DD} = 5V • Flexible applications in µP systems as buffers & latches • High order address-latch capability in CDP1800 series µP systems • Output sink current = 5mA (min) at V_{DD} = 5V	4 to 6.5	-40 to +85	3	22 D E
CDP6823	Parallel Interface (MOTEL Bus)	• 24 individual programmed I/O pins • MOTEL circuit for bus compatibility with many µPs • Multiplexed bus compatible with: ▶ CDP6805E2 and competitive µPs • Data direction registers for ports A, B and C • Reset input to clear interrupts and init. internal reg's • Four port C I/O pins may be used as control lines for: ▶ Four interrupt inputs ▶ Output pulse ▶ Input byte latch ▶ Handshake activity • 15 registers addressed as memory locations • Handshake control logic for input & output periph. oper. • Interrupt output pin • 3V to 5.5V operating V_{DD}	4.5 to 5.5	0 to +70	1	40 D E 44 Q

† T_A indicates operating temperature range over which the published electrical data are specified
* See interpretation guide and packaging section