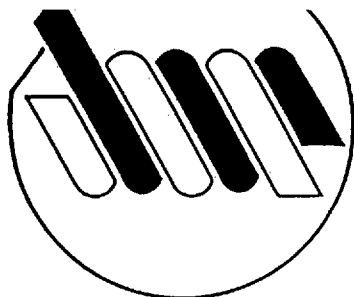


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**Walmsley Microsystems Limited****DATA SHEET**

T-77-17

WA1005

64 ELEMENT LINEAR MULTIPLEXER

The WA1005 is a 64 element linear multiplexer intended for use in Infra Red imaging applications. Designed using CMOS technology with the elements on a $80\mu\text{m}$ pitch, inputs to the device are by way of wire bonds to alternately offset pads down one side of the chip. Charge is transferred to the device from external photodetectors eg. InSb, using a direct injection scheme incorporating a buffer amplifier. The storage capacity is switchable to reduce kTC noise at low integration currents. Readout is accomplished using a MOSFET multiplexer with a rolling reset. A block diagram of the device is shown in figure 1 overleaf.

FEATURES

No. of elements	64
Spacing of elements	$80\mu\text{m}$
Attachment	Direct wire bonding to pads on-chip
Input structure	Direct injection using transimpedance amplifier
Storage capacity	(a) 4×10^7 (approx. 65nV/charge) (b) 5×10^6 (approx. 500nV/charge)
Minimum integration time	$32.5\mu\text{s}$ (2MHz shift register clock)
Maximum integration time	Application dependent
Maximum integration current	80nA (with $75\mu\text{s}$ integration time)
Technology	$3\mu\text{m}$ CMOS

Table 1 overleaf gives details of the chip performance at 77K.

APPLICATIONS

High resolution thermal imagers for use in surveillance and detection, medical and industrial process control applications.

For test and evaluation purposes an evaluation kit consisting of a test board and a packaged device plus a detailed report on chip operation and architecture is available. For prices and availability please contact the address overleaf.

Figure 1 Block Diagram

T-77-17

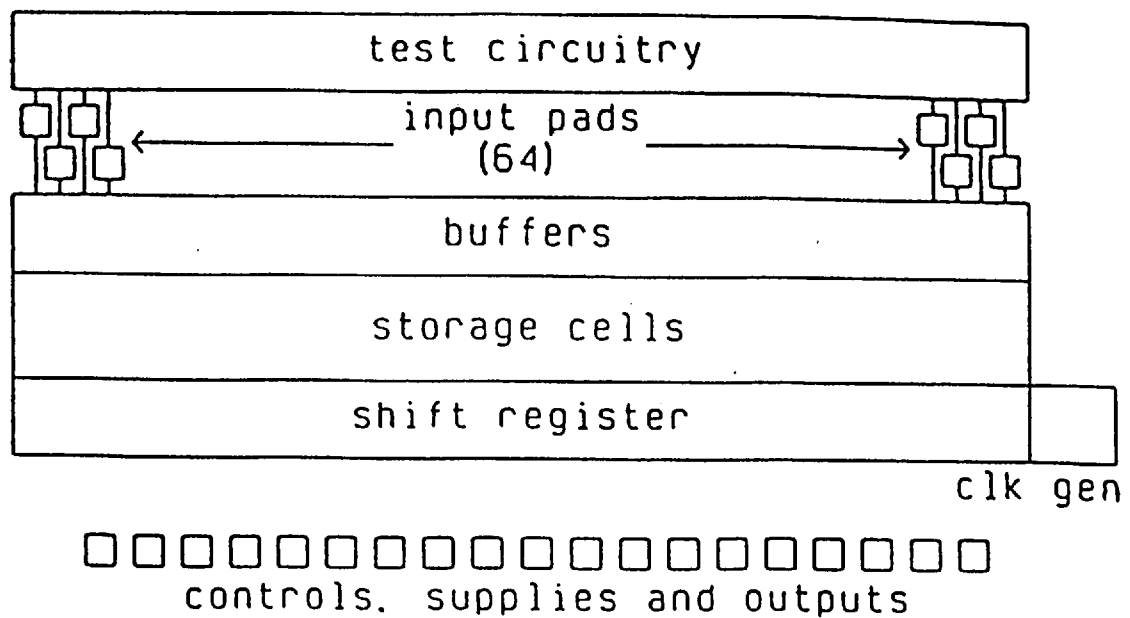
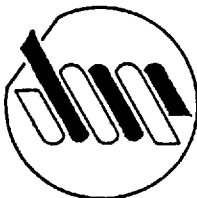


Table 1

Chip Performance at 77K

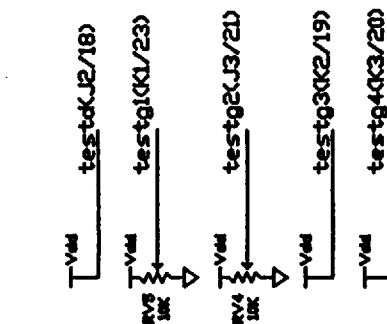
Parameter	Units	Min	Typ.	Max
f clock	MHz		0.5	2.0
I supply	mA		1.3	
RMS noise	μV		1.50	
Output signal	V			2.6
Dynamic range	dB		85	
Fixed pattern noise	mV		± 40	
Detectivity	$\text{cm}\sqrt{\text{Hz}}/\text{W}$		3×10^{11}	
Crosstalk	dB			-80

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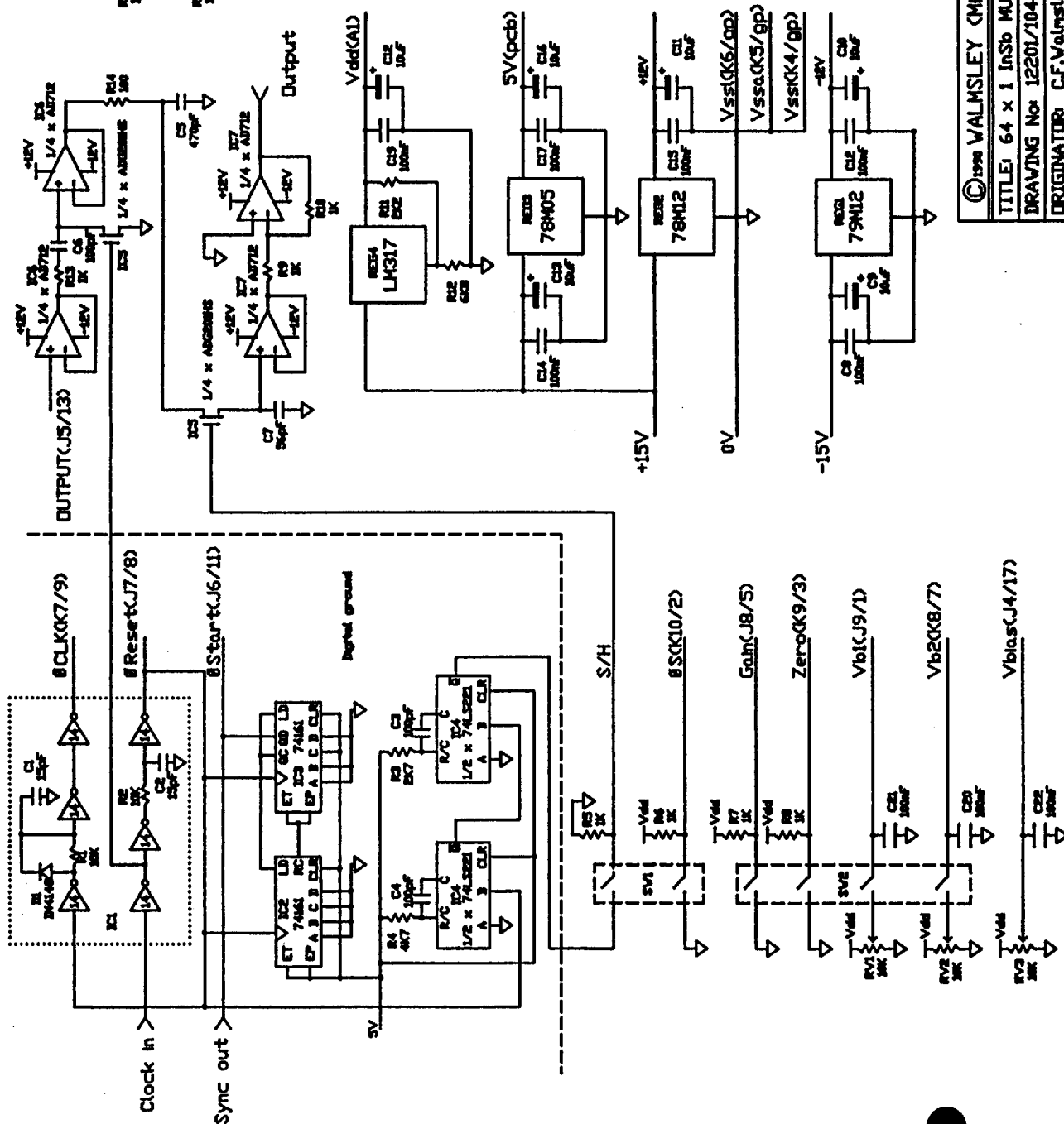
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 Birmingham B7 4BJ Telex: 334535 Fax No: 021 359 0433

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NOTES

- 1/ Chip output needs to be as short as possible, as do all tracks in analogue section.
- 2/ Test point to be added to chip output.
- 3/ ADG201HS requires 0/-12V
- 4/ Reset and clock outputs are now removed.
- 5/ Analogue/digital grounds to be separate and configured at source in star formation.
- 6/ Chip decoupling capacitors to be 100nF.
- 7/ R2 may be shorted with C2 open circuit.
- 8/ SV1 should be omitted in this version.
- 9/ Supplies are not filtered here and therefore will not provide optimum noise performance



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TITLE: 64 x 1 InSb MUX evaluation board	
DRAWING No: 12201/1044 Issue 6 DATE: 31/10/90	
ORIGINATOR: C.F. Walmsley	SCALE: n/a