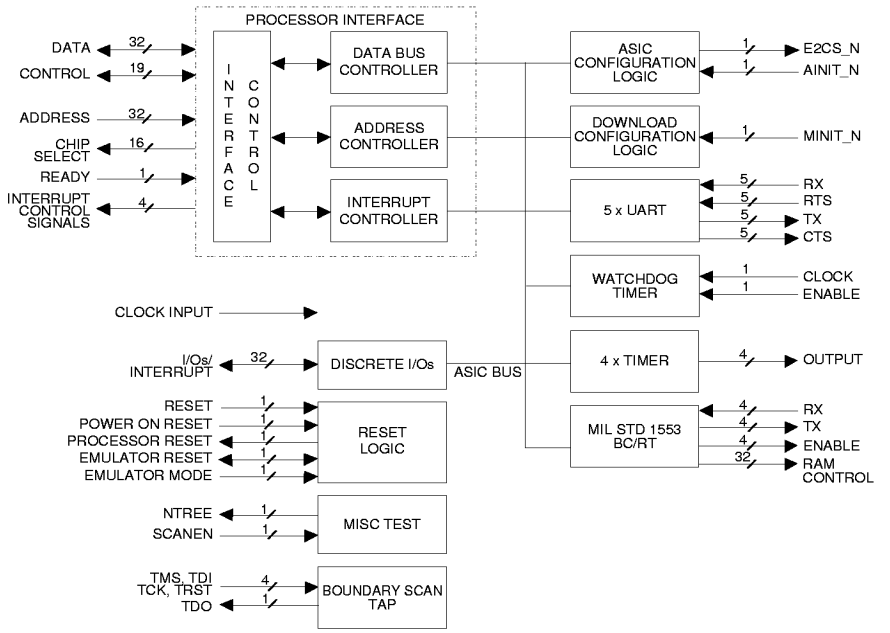
ATLAS TMS320C40 PERIPHERAL PROCESSOR *ADVANCED**

FEATURES

- TMS320C40 DSP Interface
- Clock Frequencies: 33, 40 MHz
- Packaging:
  - 447-pin Ceramic PGA
  - 484-ball Ceramic BGA
  - 484-ball Plastic BGA
- 5 General UARTs
- 4 Programmable Timers 48-bits
- Watchdog Timer
- 32 Discrete Input/Outputs
- 1553B Remote Terminal/Bus Controller Interface
- 16 Programmable Chip Selects
- Download and Device Configuration Logics
- Reset Logic
- Commercial, Industrial, and Military Temperature Ranges
- Boundary Scan Test Capability
- 5V ± 10% Power Supply
- Low Power CMOS

** This data sheet describes a product that may or may not be under development, and is subject to change or cancellation without notice.*

LOGIC FUNCTION BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	-65	+150	°C
Junction Temperature	T_J		+150	°C
Supply Voltage	V_{CC}	-0.5	+7.0	V
Input Signal Voltage Range	V_I	-0.5	+5.5	V
Voltage applied to any output in the high state	V_O	-0.5	V_{CC}	V
Voltage applied to any output in Z or power off state	V_{OZ}	-0.5	+7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Operating Temp (Military)	T_{AMB}	-55	+125	°C
(Industrial)		-40	+85	°C
(Commercial)		0	+70	°C
Supply Voltage Range	V_{CC}	+4.5	+5.5	V
Input High Signal Voltage	V_{IH}	+3.0	V_{CC} + 0.3	V
Input Low Signal Voltage	V_{IL}	-0.3	+1.5	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Max	Unit
Input	I_X	10	pF
Input/Output	IO_X	10	pF
Output	O_X	TBD	pF

OUTPUT DC CHARACTERISTICS

(V_{CC}= 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol	Test Condition	Min	Max	Units
Output High Voltage	V_{OH}	V_{CC} = 4.5V; I_{OH} = 4.0mA	2.0		V
Output Low Voltage	V_{OL}	V_{CC} = 5.5V; I_{OL} = 4.0mA		0.5	V
Output Leakage Current	I_{OZ}	Output = Tristate; $V_{OH/L}$ = min/max; V_{CC} = 5.5V		+10	µA
V_{OH} Output Current	I_{OH}	TBD		4	mA
V_{OL} Output Current	I_{OL}	TBD		4	mA

INPUT DC CHARACTERISTICS

(V_{CC}= 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol	Test Condition	Min	Max	Units
Input High Voltage	V_{IH}	Min. condition: V_{CC} = 4.5V	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	Max. condition: V_{CC} = 5.5V	GND	0.8	V
Output Leakage Current	I_{LIN}	V_{CC} = 5.5V; $V_{IH/L}$ = min/max	–	+10	µA
Input Clamp Voltage	V_{CL}*	TBD			

* The input clamp function is intended for ESD-protection of the inputs in unbiased conditions (component or board handling, assembly, test, and service). Their use for limitation of signal surge or overshoot is not recommended and may impair the function or the useful lifetime of the product.

ATLAS Data Sheet

Table of Contents

1 Functional Description

Reset Logic

The Power on Reset is supplied into the ATLAS using the device reset input MRES_N. The signal is active low. Based on this signal, the device generates the Power on Reset (PRST_N) for the processor and external devices. All reset inputs are filtered. The reset logic controls two reset output pins and the emulator reset.

Download Configuration Logic

The ATLAS Configuration Logic loads the data of the configuration memory (i.e., EEPROM) to set up the device. The content of the configuration memory modifies the device default parameters. The device external memory map, access rights and port sizes may be modified by the data content of the configuration memory. During normal operation the control registers are locked to prevent damage caused by non-functioning code.

If the Configuration Logic detects no valid configuration memory, it will cause the device to boot with its default configuration. The configuration memory can be loaded by setting the AINIT_N signal active during a Reset.

ATLAS Configuration Logic

The Device Configuration Logic serves any standard PC serial interface running its protocol using the device's main UART with RS232 drivers interface.

The MINIT_N input signal has to be set active during Reset to enter the device configuration mode. The logic will listen to the connected PC COM port waiting for download data. The data will be loaded into the specified Configuration Memory address range.

To load the Configuration memory and the Program memory in one step, both signals (AINIT_N & MINIT_N) must be active during Reset.

Processor Interface

Device PC(2:0) pins input define the clock speed. All ATLAS functions which use the input clocks as a time base need to be set up accordingly to provide a proper time base. The main UART coupled with a RS232 driver interface will configure itself automatically to interface after power up with 9600 Baud. This baud rate may be changed at any time afterwards.

Data Bus Controller

The data bus controller performs the routing of data from and to the processor.

Address Controller

The address controller selects internal ATLAS blocks or external functions like program or data, depending on the information stored in the Configuration memory or based on the default values. Read and write signals are also controlled by the address controller.

MODULAR ADDRESS MAP

Start Address	End Address	Valid data bits	Selected Block
#8000 0000h	#83FF FFFFh	D(31:0)	Data Memory
#8400 0000h	#87FF FFFFh	D(15:0)	ATLAS Blocks
#8800 0000h	#BFFF FFFFh	D(31:0)	Chip Select
#C000 0000h	#FFFF FFFFh	D(31:0)	Program Memory

There are 16 free programmable Chip Select Areas. The following settings may be performed for all areas:

- Start Address
- Offset Address
- Wait States: 0-7 or External
- Select or Deselect Area
- Select whether Data or Program
- Select whether Program Memory is read only
- Select whether data memory is read only or read and write

According to the described settings error messages will appear if:

- Read or Write access to undefined / unused area
- Program access to data area
- Write access to write protected area
- Illegal Function Code
- Time Out

All settings will be loaded from the configuration memory or defaults will be used. Default size for Chip Selects (memory area) is 64Mbyte.

ATLAS INTERNAL ADDRESS MAP

Start Address	End Address	Valid data bits	Selected Block
#840F 0000h	#840F FFFFh	D(15:0)	Reserved
#8400 0000h	#8400 FFFFh	D(15:0)	MIL-STD-1553
#8400 0000h	#8400 FFFFh	D(15:0)	Timer 3
#8400 0000h	#8400 FFFFh	D(15:0)	Timer 2
#8400 0000h	#8400 FFFFh	D(15:0)	Timer 1
#8400 0000h	#8400 FFFFh	D(15:0)	Timer 0
#8400 0000h	#8400 FFFFh	D(7:0)	UART 4
#8400 0000h	#8400 FFFFh	D(7:0)	UART 3
#8400 0000h	#8400 FFFFh	D(7:0)	UART 2
#8400 0000h	#8400 FFFFh	D(7:0)	UART 1
#8400 0000h	#8400 FFFFh	D(7:0)	UART 0
#8400 0000h	#8400 FFFFh	D(15:0)	Watch Dog Timer
#8400 0000h	#8400 FFFFh	D(15:0)	Discrete I/O
#8400 0000h	#8400 FFFFh	D(7:0)	ATLAS BOOT EEPROM
#8400 0000h	#8400 FFFFh	D(15:0)	Interrupt Controller
#8400 0000h	#8400 FFFFh	D(15:0)	Address Controller

Address Map Address Controller

The internal address control registers are read only during normal operation. The contents is either default or overwritten by configuration memory data.

The address controller registers define start addresses, size and features of the relevant CS area.

Start Address/Size Registers

- The smallest programmable memory area is 64K.
- The start address may be incremented in steps of 64K.
- Overlapping within the defined address space will cause a Bus Error.

Control Register for External CS(x)

With physical memory location bit set, the ATLAS is capable of driving data buffers.

Error Register

The error codes will be set as soon as a bus error occurs. It will show the status of the last bus error until a new error occurs.

Error Address Register

The error address register will hold the address which was valid during occurrence of the bus error.

DMA Controller

A Direct Memory Access from the outside is possible on the Global Bus. the external device must request the bus by driving BUSREQ_N signal to a low level. As soon as the BUS_DIS signal goes high, the external device is the master of the global bus. For a read or write access, the External Master must simulate the DSP read or write cycle. At the end of the DMA, the BUSREQ_N signal will go high to enable the Global Bus for the C40.

Interrupt Controller

The interrupt controller provides the required signals. Interrupt functionality is provided for all internal ATLAS blocks. The Interrupt priority level is fully programmable.

Features:

- Maskable Interrupt-Events
- Programmable interrupt level for every event
- Interrupt reset by writing to specific address
- Automatic interrupt reset utilizing interrupt acknowledge cycle
- Uses all four C40 Interrupt Inputs.
- Every ATLAS block can generate interrupt events
- The pending interrupts are visible by reading the interrupt register
- 32 discrete I/Os are combined to 4 interrupt events

Address Map Interrupt Controller

The port size of the interrupt controller is 16 bits. Within the address space the Interrupt Register, 15 Interrupt Control Registers and 15 Pending Interrupt registers will be found. The 15 Interrupt Control Registers are used to define the processor interrupt priority and the hardware interrupt priority. The same level of processor interrupt priority may be assigned more than once, the device interrupt priority is allowed only once. Each block in the device has to have one unique interrupt priority.

The Interrupt Control Registers also allow masking of every interrupt independent of its priority.

A read access to the Interrupt Status Register will give the processor an overview of all pending interrupts which are waiting at the input of the priority decoder to be selected based on their importance.

UARTs

The ATLAS device includes 5 UARTs. One main UART (for download purposes with RS232 transceivers) and 4 other UARTs. All UARTs have the same features. The main UART should be connected to RS 232 drivers to allow easy connection to a PC serial port.

Features:

- A baud rate generator, programmable between 76 Baud and 5 Mbaud
- 5 - 8 Data bits
- 1 - 2 Stop bits
- Programmable Parity
- Receive and Transmit FIFO (32x8 bit)
- One interrupt assigned for each UART
- Interrupts are caused by Receive, Transmit, Frame and Parity Error, FIFO Overflow and Receiver Write Fail
- Handshake Signals RTS/CTS
- Hello Message following each reset

The default UART settings are: 8 Data bits, 1 Stop bit, no Parity, no Handshake, 9600 Baud.

Address Map UART

Starting from the Base Address given in the address controller section the address space of the UART will be 75 Bytes.

Example:

Baud Rate settings running the device with 25 MHz:

UTRH	UTRL	Baud Rate
02_{Hex}	08_{Hex}	9600
01_{Hex}	03_{Hex}	19K2
00_{Hex}	81_{Hex}	38K4
00_{Hex}	$2A_{Hex}$	115K2
00_{Hex}	00_{Hex}	5M
FF_{Hex}	FF_{Hex}	76

Discrete I/Os

There are 32 Bi-directional I/O Signals. Each can be programmed as Discrete Input, Discrete Output or Interrupt Input. When programmed as Discrete Input/Output, the level of each individual pin can be set/observed via a write/read access to internal registers. When programmed as Interrupt Input, each Interrupt Input can be programmed to be level or edge sensitive. The maximum of 32 Interrupt Inputs are routed as 4 individual Interrupt Signals to the Interrupt Controller. All inputs feature glitch suppression.

Watch Dog Timer

The Watch Dog Timer has its own clock input to be fully independent of the rest of the device. The Watch Dog has two functioning modes: Overflow and Window Mode. If programmed in Overflow Mode, the Watch Dog will cause a Watch Dog trigger if the Watch Dog is not triggered during a given time period (max. 167 ms). In Window Mode the Watch Dog must be triggered during the last 1.6 ms of the given Time Period, otherwise a Watch Dog trigger will occur. The Time Period is programmable between 1.6 ms and 167 ms (at 25 MHz).

Features:

- The Watch Dog is a timer which counts down to zero
- The Watch Dog will cause a Watch Dog trigger once it reaches zero
- It is programmable whether it's possible to set the timer to zero at any time (Overflow Mode) or just during a given window before reaching zero (Window Mode)

Setting the WDDIS_N signal to a zero ('0') level disables the Watch-Dog circuitry .

After every reset, the Watch Dog Counter will be reloaded with its time base, which is 64 times the value stored inside the Overflow Register (OPR). Every time the counter reaches zero, the Watch Dog Error Counter will be incremented by one until the Watch Dog Error Counter reaches 15. *Only an external or a power on reset can reset the Watch Dog Error Counter.*

Timers

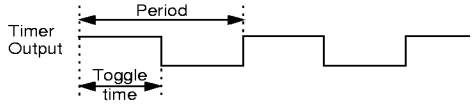
The device includes 4 identical Timers of 16 bits with 32 bits prescaler.

Features:

- Programmable time base
- The timers count back to zero from their set values.
- Time base reload is possible at any time.
- Interrupt event when reaching zero
- Programmable whether the timer generates a one time interrupt or continues interrupts
- Programmable whether the timer works as frequency divider or in pulse mode.
- Timer clock is device output

Programming Modes:

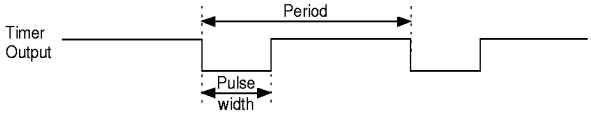
A. Timer in Frequency Divider Mode



Minimum Toggle Time: 2/Frequency
Maximum Toggle Time: $(2^{16}+1) \times (2^{32}+1)$/Frequency

In frequency divider mode the duty cycle is 50/50. Every edge (falling and rising) will cause an interrupt.

B. Timer in Pulse Mode

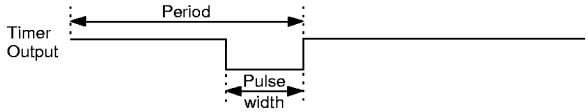


Minimum Pulse Width: 1/Frequency
Maximum Pulse Width: $(2^{16}+1)$/Frequency
Minimum Time Period: 2/Frequency
Maximum Time Period: $(2^{16}+1) \times (2^{32}+1)$/Frequency

The interrupt will occur immediately after the Pulse becomes active.

C. Timer in Trigger Mode

In trigger mode the timer will run one period, generate one interrupt and stop afterwards.



Minimum Pulse Width: 1/Frequency
Maximum Pulse Width: $(2^{16}+1)$/Frequency
Minimum Time Period: 2/Frequency
Maximum Time Period: $(2^{16}+1) \times (2^{32}+1)$/Frequency

The pulse gap may only be programmed as a multiple of the pulse width. The interrupt will be set as soon as the pulse width becomes active.

MIL-STD-1553

The device features a MIL-STD-1553B remote terminal and bus controller.

General

MIL-STD-1553B defines a time-multiplexed serial data bus. Using a half-duplex protocol commands and responds are sent over the bus. Up to 32 subsystems and a bus monitor may be connected onto the same bus. One of these subsystems, the Bus Controller (BC), controls as a Master the bus communication. All other 31 subsystems have Slave status and are connected to the bus as Remote Terminals (RT).

For bus communication, the BC sends Command Words (CW) over the bus addressing RTs to either transfer 16-bit wide Data Words (DW) to RT's or request data from them. A Command Word (CW) contains the address of the desired RT and the command to be executed.

The addressed RT responds under normal conditions with a Status Word (SW). This Status Word contains, beneath its own address, information about the current status of the RT. Dependent on the command sent by the BC, one or more Data Words may follow the RT's Status Word.

In addition to the data communication the BC is capable of controlling or debugging an RT by sending so-called Mode-Code Command Words.

All transferred data consists of 20 bits. The first 3 bits are used for synchronization, 16 bits contain real information and the last bit is used for parity. The Mil.-Bus parity is defined to be "odd". The Mil.-Bus data rate is 1 Mbit (1 MHz). The Mil.-Bus uses bipolar Manchester II Code for data transmission.

MIL-STD-1553B may be used as redundant Bus System. In case of a one time redundant bus system (2 Busses) one bus has to be active, the other one needs to be standby.

Bus Protocol

This chapter gives a brief introduction about the MIL-STD-1553B Bus protocol.

Message Types

The 1553 Bus knows 10 different types of information/ message transfers.

6 Dedicated Information Transfers

- BC - to - RT
- RT - to - BC
- RT - to - RT
- BC - to - RT (Mode Command)
- BC - to - RT (Mode Command with Data return)
- BC - to - RT (Mode Command with Data)

4 Global Information Transfers (Broadcast Messages)

- BC - to - RT
- RT - to - RT
- BC - to - RT (Mode Command without Data Words)
- BC - to - RT (Mode Command with Data Word)

Word Formats

The complete 1553 Bus communication uses only three (3) word formats. All words are 20 bits long, comprised of 3 Synchronization bits, 16 Information bits and a final Parity bit.

The Synchronization bits violate the Manchester II Code which is used for the rest of the transmission. Manchester II changes its level in the middle of the transferred bit. The Synchronization bits may be seen as three bits where only the middle one acts like it is required by Manchester II. This means during the 3 bit time frame of the Synchronization bits, the Bus will start active low by changing after 1.5 bits to active high for Data Words and start active high by changing to active low after 1.5 bits to active low for Command Words and Status Words.

Command Word: The CW is sent only by the BC.

Data Word: The Data Word contains only 16 Data bits.

Status Word: Status Words are not sent in a Broadcast Cycle.

Mode Code - Commands

The Bus Controller uses Mode Code - Commands to control the RT. By setting the subaddress in a Command Word to either '00000' or '11111' the BC indicates a Mode Code in the following five (5) bits. In addition to the Mode Code the RT has to look at the R/T-bit as well.

ATLAS Typical Application

Functional Description

The Block Diagram shows the processor connected to program and data memories on both, local and global buses, to allow optimum processing performance. All functions which are necessary to boot and run the processor, interface to the memories, are implemented in the device. Additional functions like timers, counters, etc. are also part of the device functionality. The ATLAS also includes the digital functions of the MIL-STD-1553B Remote Terminal/Bus Controller. The transceiver chips, which are necessary to drive the Mil-Bus transformers, need to be connected externally to the device as well as the transformers.

Connected to the ATLAS is its configuration memory. This memory holds the data which tells the device how to configure itself, the module and its environment. Without the configuration memory or without data in it, the device boots with its default configuration.

In the default configuration, the device is capable of communicating with a standard PC serial port or any other compatible interface using its main UART with RS232 transceivers. This function must be used to load the configuration memory as well as the program memory.

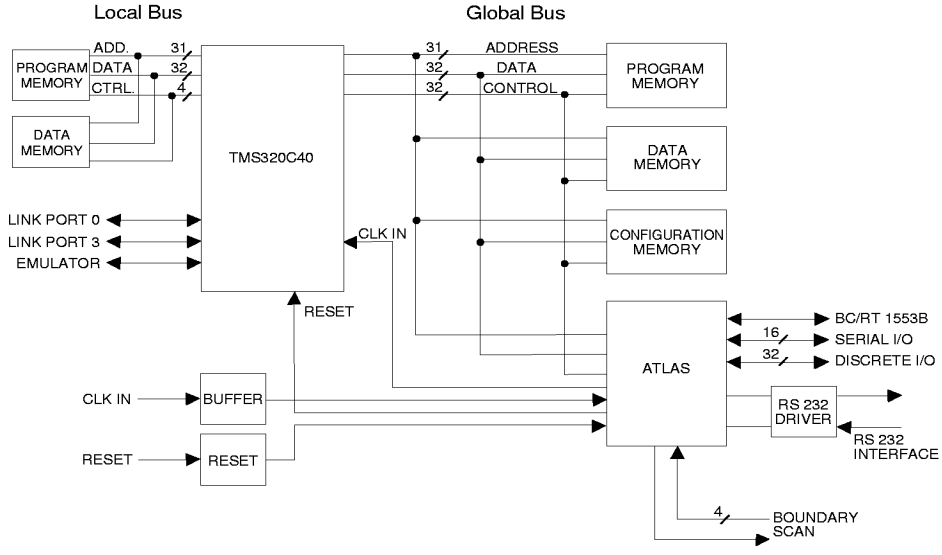
The configuration memory and the program memory may also be loaded using the ATLAS BSCAN capability.

ATLAS Programming Mode

The ATLAS will boot after reset with the default values if the first bytes of the configuration memory are not loaded with a special sequence . If the ATLAS finds this sequence, it assumes valid data in the configuration memory and will use them.

To program the device, the user needs to set two external pins (AINIT_N & MINIT_N) telling the ATLAS whether configuration memory, program memory or both shall be loaded. Then the ATLAS RS232 interface must be connected to a PC serial port. Following any Power On Reset the ATLAS will check AINIT_N and MINIT_N first before releasing the processor. If one or both of the signals are set, the ATLAS keeps control and waits for download data. The PC needs to run software which supports the protocol.

More detail about ATLAS initialization and ATLAS addressing will be found in the device user's manual.



2 Initialization of Processor Modules

Boot Up Sequence

After receiving an external reset (RSTIN_N), the ATLAS will recover from reset first and will hold all other devices connected to its RESOUT signal in reset.

The ATLAS will first check the CLKTYPE Pins to configure its Time-Base registers. Then the AINIT_N and MINIT_N signal will be checked. If one or both of them are set the configuration memory and/or program memory download will be initiated. As soon as the download and/or configuration process is finished the ATLAS will load the configuration data, send an 'OK' message to the PC and release the reset after 100,000 clock cycles.

If AINIT_N and/or MINIT_N are not set, the ATLAS will release the processor to boot from memory.

The RSTIN_N -input may be driven by another processor device, a switch or any peripheral circuitry.

Depending on the presence of the configuration memory, the ATLAS is reset to its default values or loads its configuration out of the configuration memory.

Configuration Memory Download

Having set the AINIT_N input to zero after reset, the device is in Configuration Memory Download mode. It listens to the main UART interface waiting for data from the host PC. The PC has to send data to the device using a specific protocol.

Program Memory Download

If the AINIT_N input is not set after reset but the MINIT_N is set to zero, the device will be in the Program Download Mode. The device will listen to the main UART interface and wait for data. The data has to be sent using a specific protocol.

3 IEEE Standard 1149.1-1990 Implementation

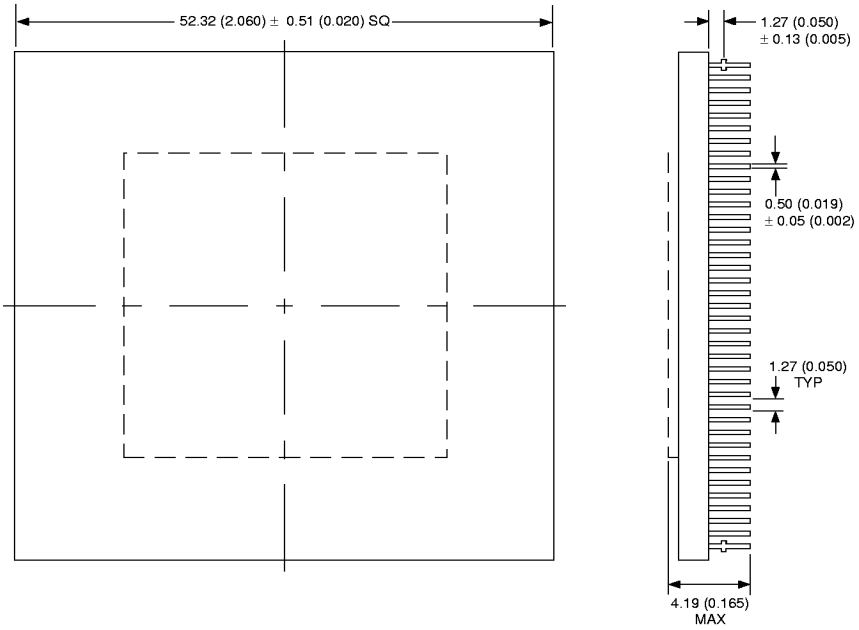
Test Architecture

Serial test information is conveyed with a 4-wire test bus, or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK, and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

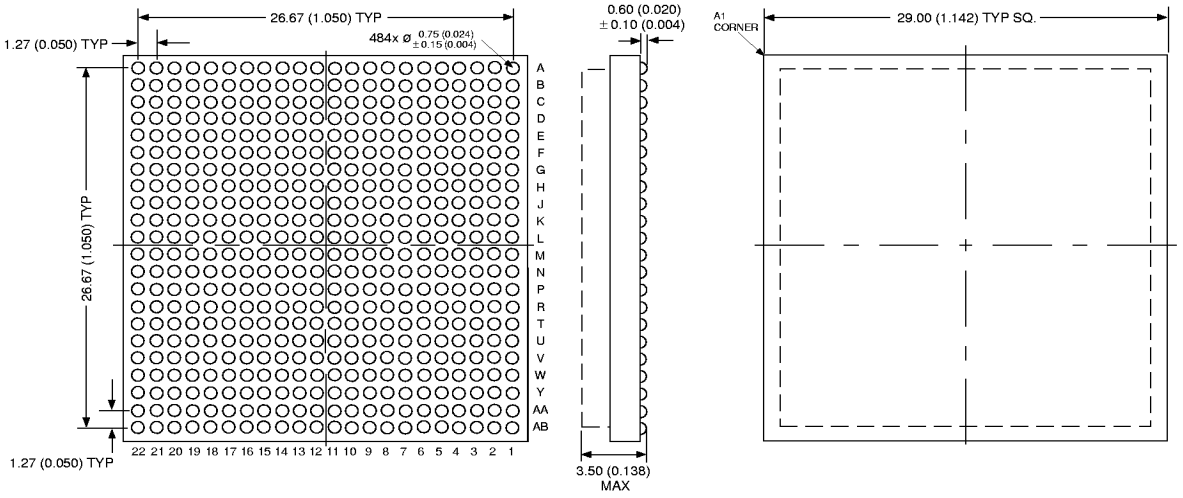
The device features a 32 bit ID code register and an 8 bit Data Register.

PACKAGE DIMENSION: 447 CERAMIC PGA (STAGGERED PINS)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION: 484 PLASTIC/CERAMIC BGA



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

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