HEWLETT® PACKARD

# 155 Mb/s Single Mode Fiber Transceiver with Integrated Clock and Data Recovery for ATM, SONET OC-3/SDH STM-1

## Technical Data

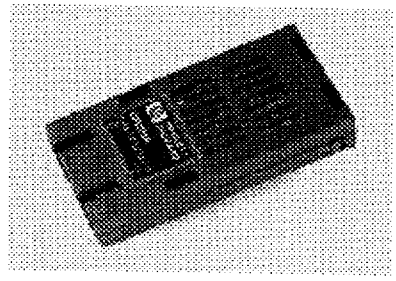
**CDX2155**

### Features

- **1300 nm Single Mode Transceiver for Links up to 15 Km**
- **Compliant with ATM Forum 155.52 Mb/s Physical Layer Specification AF-PHY-0046.000**
- **Compliant with Specifications Proposed to ANSI T1E1.2 Committee for Inclusion in T1.646-1995 Broadband ISDN and T1E1.2/96-002 SONET Network to Customer Installation Interface Standards**
- **Compliant with ANSI T1.105.06 SONET Physical Layer Specifications Standard**
- **Multisourced 2 x 9 Pin-out Package Style**
- **Integral Duplex SC Connector Receptacle Compliant with TIA/EIA and IEC Standards**
- **Single +5 V Power Supply Operation and PECL Logic Interfaces**
- **Incorporates Hewlett-Packard's Eyesafe Laser Subassembly**
- **Integral Digital PLL Provides Regenerated Differential Clock Output**
- **Integral Decision Circuit Provides Retimed Differential Data Output**
- **Laser Bias Monitor, Reference Clock, Transmitter Disable and Laser Power Monitor Functions**
- **Two Temperature Ranges: 0°C to +70°C - CDX2155B/D -40°C to +85°C - CDX2155A/C**
- **Wave Solder and Aqueous Wash Process Compatible**
- **Manufactured in an ISO 9001 Certified Facility**

### Applications

- **ATM 155 Mb/s Links**
- **SONET OC-3/SDH STM-1 Interconnections**



### Description

#### General

The CDX2155 is a 1300 nm laser-based duplex SC receptacle 2 x 9 transceiver with integral clock and data recovery circuits. It provides a cost-effective solution to medium haul 155 Mb/s data link requirements.

This compact transceiver requires a single +5 V source and contains the following data, clock and monitoring features as depicted in Figure 1: differential data input, differential retimed data output, recovered clock output, signal detect, laser bias monitor, transmitter disable, and

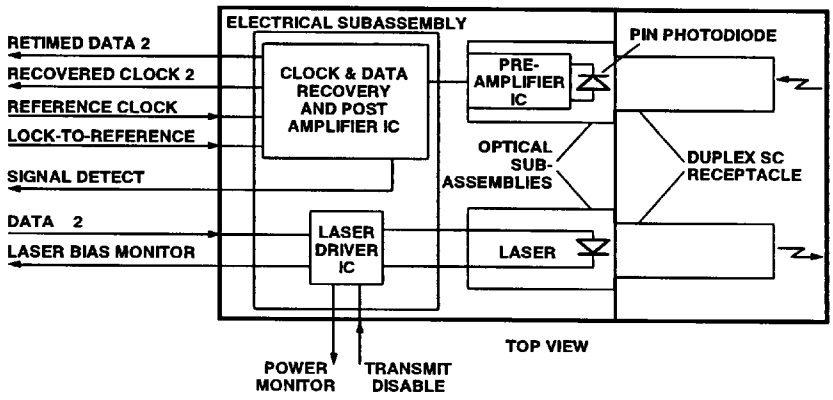



**Figure 1. Block Diagram.**

an option to generate a local timing signal from an external, low-frequency reference clock. The external timing signal acts as the reference clock when incoming optical signals become undetectable.

### Transmitter Section

The transmitter section of the CDX2155 is similar to other Hewlett-Packard 1300 nm single mode transceivers in use at the 155 Mb/s data rate. It consists of a 1300 nm InGaAsP laser in an eye-safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a custom, silicon bipolar IC which converts differential input PECL logic signal into an analog laser drive current.

### Receiver Section

The receiver section of the transceiver provides a full set of features including an integral clock and data recovery (CDR) circuit together with an optional, selectable receiver local clock source.

The receiver utilizes an InGaAs PIN photodiode mounted together with a transimpedance preamplifier IC in an OSA. This OSA is connected to a custom, silicon bipolar circuit providing post-amplification and quantization, CDR function, and optical signal detection.

### CDR Function

In normal operation, the CDR data loop is able to acquire and maintain bit lock without the use of the optional, external reference clock. This loop consists of a patented phase/frequency detector with false-lock protection. The recovered clock is used to retime the quantizer data output, which completes the full CDR function.

The relative timing relationship between the output retimed data and the recovered clock signals is shown graphically in Figure 2.

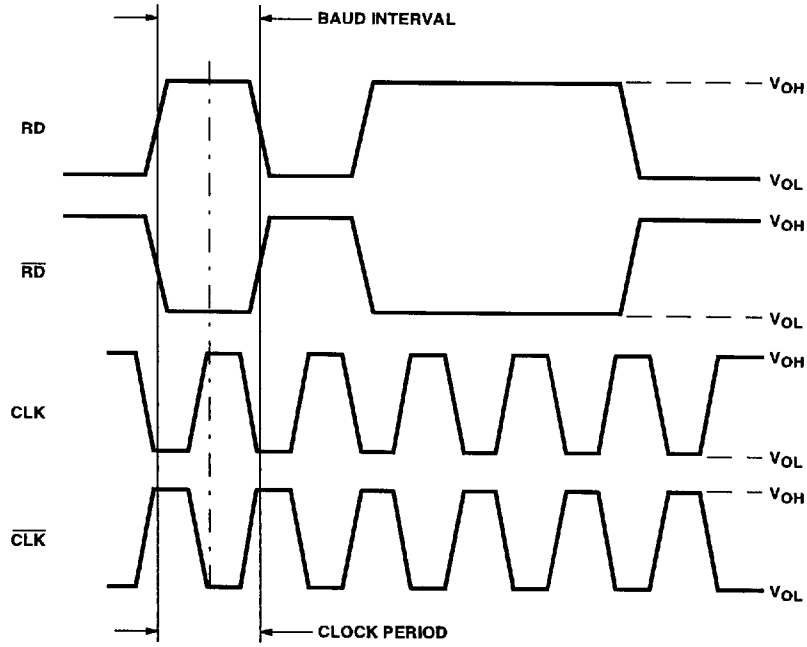



**Figure 2. Relative Timing Relationship between Output Retimed Data and Recovered Clock Signals.**

For input optical power greater than the specified receiver sensitivity of -28 dBm, the bit-error-ratio will be better than $1 \times 10^{-10}$. As the input power is decreased by several dB, the bit-error-ratio degrades. Within 1 dB below the $1 \times 10^{-2}$ BER input optical power level, the CDR will begin to lose lock and the clock frequency will drift from 155.52 MHz. Once the CDR loses lock, the clock frequency will sweep through the entire VCO range, about 140 to 200 MHz. The rate of the sweep is inversely proportional to the input optical power and will reach its maximum at a point of 2 dB below the lock point. Since data is retimed to the clock, a loss of lock will produce an output data stream consisting of randomly switching data bits, i.e., noise.

### Receiver Signal Detect

As the input optical power is decreased, Signal Detect will switch from high to low (de-assert point) at a point between 3 dB below minimum guaranteed sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 0.5 dB higher than the de-assert level. This single-ended low-power PECL output is designed to drive a standard PECL input using a 10 kΩ load instead of the normal 50 Ω PECL load.

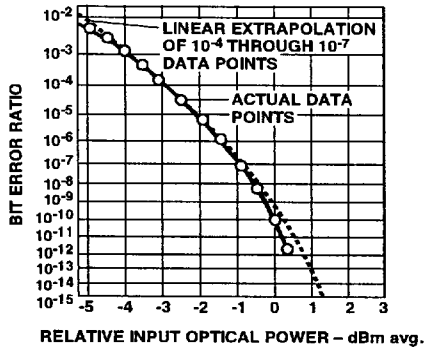



**Figure 3. Relative Input Optical Power–dBm Avg.**

### Reference Clock

In applications where the receiver recovered clock frequency is not allowed to drift upon loss of input optical signal, the CDX2155 has the ability to generate a local clock output by multiplying an optional, external 19.44 MHz reference clock up to the OC-3/STM1 155.52 MHz rate. This feature is possible because the clock recovery system consists of two loops: a data loop which locks onto the incoming optical data stream, and a second reference loop which locks onto the optional external reference clock.

This optional feature is initiated by applying a Lock-to-Reference logic signal to pin 2 (Lck Ref-) which switches the loop to the external reference clock and disables the received data outputs. Pin 2 (Lck Ref-) can be driven from the Signal Detect pin 15 (SD) output or from other logic further upstream in the ATM interface which may be monitoring the quality of the received data stream.

### Transceiver Specified for Wide Temperature Range Operation

The CDX2155 is specified for operation over normal commercial temperature range of 0° to +70°C (CDX2155B/D) or the extended temperature range of -40°C to +85°C (CDX2155A/C).

## Other Members of HP 155 Mb/s Product Family

- SDX1155, 1300 nm laser-based 1 x 9 SC receptacle transceiver for 15 km links with SMF cables (without CDR)
- HFBR-5208 1300 nm LED based 1 x 9 SC receptacle transceiver for 500 m links with MMF cables (drop in replacement for SDX1155)
- XMT5360-155 1300 nm laser-based transmitter in pigtailed package for 15 km links with SMF cables
- XMT5160-155 1300 nm laser-based transmitter in pigtailed package for 40 km links with SMF cables
- RCV1201D-155 receiver in pigtailed package for 15 km and 40 km links with SMF cables
- RGR1155 receiver with integral clock and data recovery in pigtailed packages for 15 km

## Applications Information

### Typical BER Performance of Receiver versus Input Optical Power Level

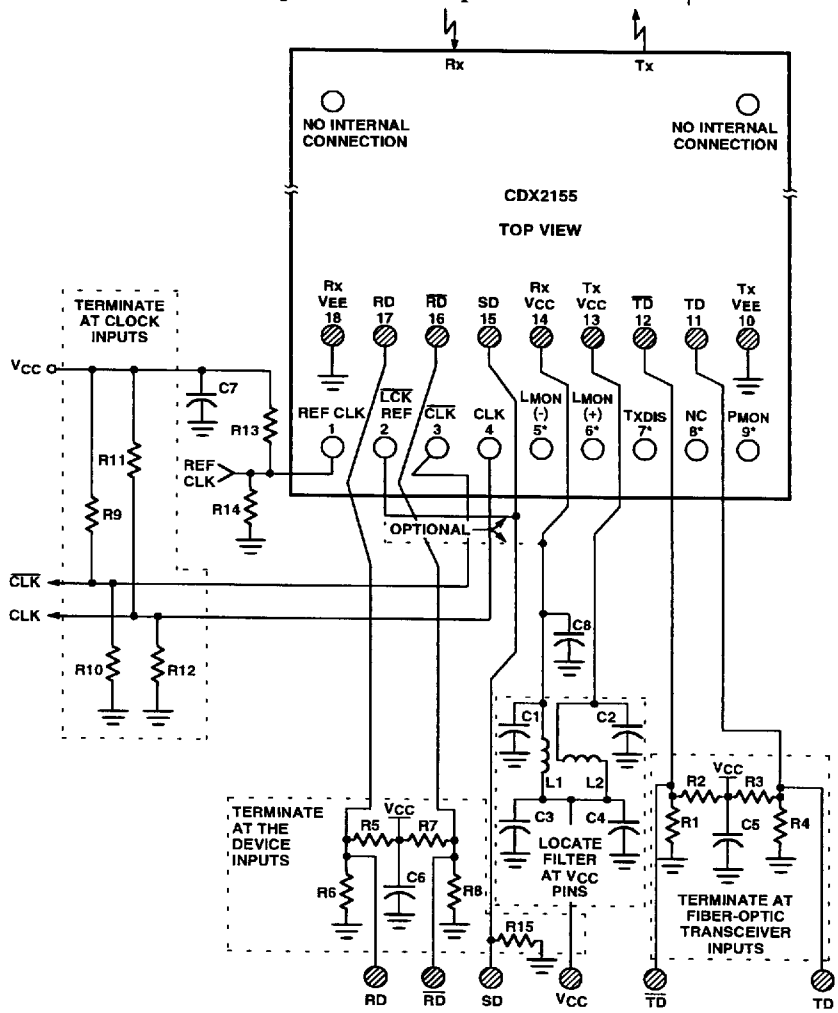
The CDX2155 transceiver can be operated at Bit-Error-Rate conditions other than the required BER = $1 \times 10^{-10}$ of the ATM Forum 155.52 Mb/s Physical Layer Standard. The typical tradeoff of BER versus Relative Input Optical Power is shown in Figure 3. The Relative Input Optical Power in dB is referenced to the Input Optical Power parameter value in the Receiver Optical Characteristics table. For

better BER condition than $1 \times 10^{-10}$, more input signal is needed (+dB).

**Recommended Circuit Schematic**

In order to insure proper functionality of the CDX2155 a recommended circuit is provided in Figure 4. When designing the circuit interface, there are a few fundamental guidelines to follow. For example, in the Recommended Circuit Schematic figure the differential data lines should be treated as 50 ohm Microstrip or stripline transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Proper termination of the differential data and clock signals will prevent reflections and ringing which would compromise the signal fidelity and generate unwanted electrical noise. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length to prevent pulse-width distortion and data-to-clock timing skew from occurring. For the high speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents from flowing which will cause distortion in the signal.

Maintain a solid, low inductance ground plane for returning signal currents to the power supply. Multilayer plane printed circuit board is best for distribution of $V_{CC}$, returning ground currents, forming transmission lines and shielding. Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver and the clock recovery circuits. Proper power supply filtering of $V_{CC}$ for this transceiver is accomplished by using the recommended, separate filter circuits shown in Figure 4, the Recommended Circuit Schematic diagram, for the transmitter and receiver sections. These filter circuits suppress $V_{CC}$ noise of 50 mV peak-to-peak or less over a broad frequency range. This prevents receiver sensitivity degradation as well as false-lock or loss-of-lock in the clock recovery circuitry due to $V_{CC}$ noise. It is recommended that surface-mount components be used. Use tantalum capacitors for the 10 µF capacitors and monolithic, ceramic bypass capacitors for the 0.1 µF




NOTES:
THE SPLIT-LOAD TERMINATIONS FOR PECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE PECL SIGNALS.
R1 = R4 = R6 = R8 = R10 = R12 = R14 = 130 Ω.
R2 = R3 = R5 = R7 = R9 = R11 = R13 = 82 Ω.
C1 = C2 = C3 = C5 = C6 = C7 = 0.1 µF.
C4 = C8 = 10 µF.
L1 = L2 = 1 µH COIL.
R15 = 10 kΩ.
FOR THE SINGLE MODE CDX2155 TRANSCEIVER, PINS 5 - 9 ARE USED FOR LASER DIODE BIAS AND OPTICAL POWER MONITORING AS WELL AS TO PROVIDE A TRANSMITTER DISABLE FUNCTION. *FOR THE MULTIMODE HFBR-5207 TRANSCEIVER, PINS 5 - 9 ARE NOT USED.

**Figure 4. Recommended Circuit Schematic.**

capacitors. Also, it is recommended that a surface-mount coil inductor of 1 µH be used. Ferrite beads can be used to replace the coil inductors when using quieter $V_{CC}$ supplies, but a coil inductor is recommended over a ferrite bead. Coils with a low, series dc resistance (<0.7 ohms) and high, Self-resonating frequency are recommended. All power supply components need to be placed physically next to the $V_{CC}$ pins of the receiver and transmitter. Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

In addition to these recommendations, Hewlett-Packard's Application Engineering staff is available for consulting on best layout practices with various vendors mux/demux, clock generator and clock recovery circuits. HP has participated in several reference design studies and is prepared to share the findings of these studies with interested customers. Contact your local HP sales representative to arrange for this service.

### Evaluation Circuit Boards

Evaluation circuit boards implementing this recommended circuit design are available from Hewlett-Packard's Application Engineering staff. Contact your local HP sales representative to arrange for access to one if needed.

### Operation in -5.2 V Designs

For applications that require -5.2 V dc power supply level for true ECL logic circuits, the CDX2155 transceiver can be operated with a $V_{CC}$ = 0 V dc and a $V_{EE}$ = -5.2 V dc. This transceiver is not specified with an operating, negative power supply voltage. The potential compromises that can occur with use of -5.2 V dc power are that the absolute voltage states for $V_{OH}$ and $V_{OL}$ will be changed slightly due to the 0.2 V difference in supply levels. Also, noise immunity may be compromised for the CDX2155 transceiver because the ground plane is now the $V_{CC}$ supply point. The suggested power supply filter circuit shown in Figure 4 Recommended Circuit Schematic should be located in the $V_{EE}$ paths at the transceiver supply pins. Direct coupling of the differential data and clock signals can be done between the CDX2155 transceiver and the standard ECL circuits. For guaranteed -5.2 V dc operation, contact your local Hewlett-Packard Field Sales Engineer for assistance.

## Recommended Solder and Wash Process

The CDX2155 is compatible with industry standard wave or hand solder processes.

### CDX2155 Process Plug

The CDX2155 transceiver is supplied with a process plug for protection of the optical ports with the Duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping, or storage. It is made of high-temperature, molded, sealing material that will withstand +80°C and a rinse pressure of 50 lb/in$^2$.

### Recommended Solder Fluxes and Cleaning/Degreasing Chemicals

Solder fluxes used with the CDX2155 fiber-optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha- metals of Jersey City, N.J.

Recommended cleaning and degreasing chemicals for the CDX2155 are alcohols (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane), and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1.1.1. trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone.

## Regulatory Compliance

The CDX2155 is intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table 1 for details. Additional information is available from your Hewlett-Packard sales representative.

### Electrostatic Discharge (ESD)

Normal ESD handling precautions for ESD sensitive devices should be followed while using the CDX2155. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

Additionally, static discharges to the exterior of the equipment chassis containing the transceiver parts must also be considered. If the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

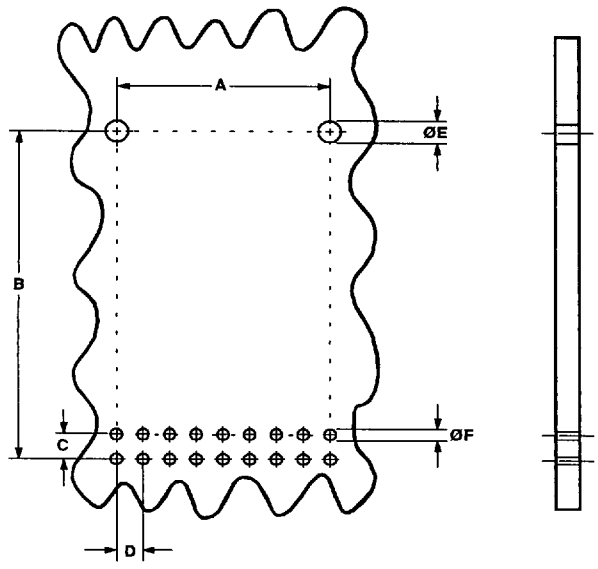
**Electromagnetic Interference (EMI)**

Most equipment designs utilizing these high-speed transceivers from Hewlett-Packard will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe, and VCCI in Japan.

The CDX2155 has been characterized without a chassis enclosure to demonstrate the robustness of the parts integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

**Immunity**

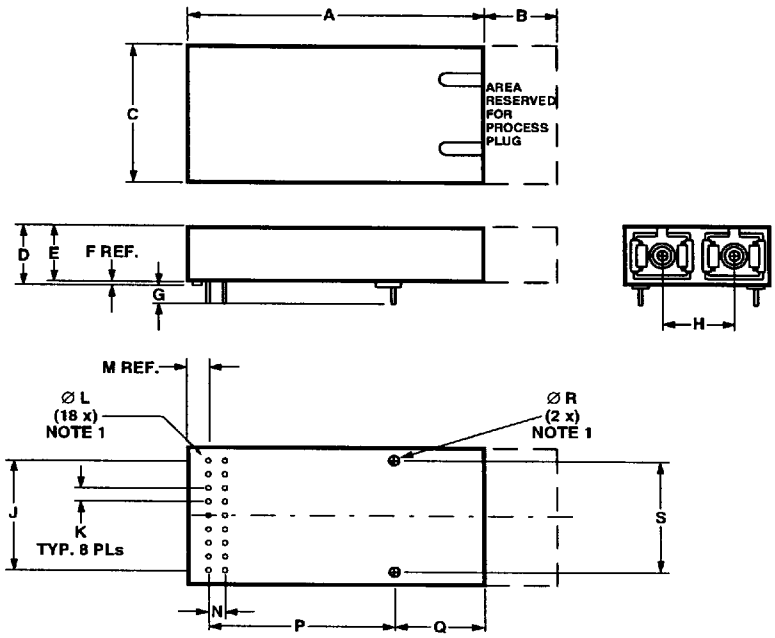
Equipment utilizing these CDX2155 transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well-designed chassis is expected to be better than the results of these tests without a chassis enclosure.



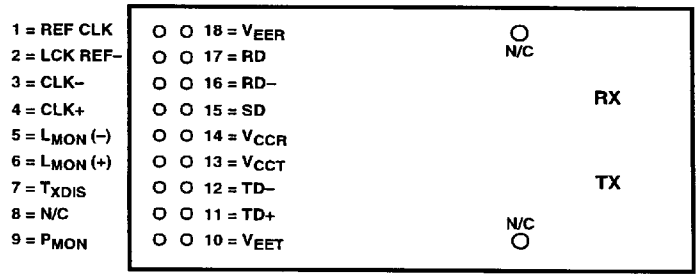

TOP VIEW

| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | 20.32 | | | 0.8 | |
| B | | 33.02 | | | 1.3 | |
| C | | 2.54 | | | 0.1 | |
| D | | 2.54 | | | 0.1 | |
| E | 1.8 | | 2.0 | 0.071 | | 0.079 |
| F | 0.7 | | 0.9 | 0.027 | | 0.035 |

**Figure 5. Recommended Board Layout Hole Pattern.**




NOTE 1: SOLDER POSTS AND ELECTRICAL PINS ARE TIN/LEAD PLATED.




TOP VIEW

| DIM. | MILLIMETERS | | | INCHES | | | DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 52.02 | | | 2.048 | K | | 2.54 | | | 0.100 | |
| B | | 12.70 | | | 0.500 | | ØL | 0.46 | | 0.53 | 0.018 | | 0.021 |
| C | | | 25.40 | | | 1.000 | M | | 3.12 | | | 0.123 | |
| D | | | 11.1 | | | 0.437 | N | | 2.54 | | | 0.100 | |
| E | | | 10.35 | | | 0.407 | P | | 33.02 | | | 1.300 | |
| F | | 0.75 | | | 0.030 | | Q | | 15.88 | | | 0.625 | |
| G | | 3.30 | | | 0.130 | | ØR | 1.27 | | 1.32 | 0.050 | | 0.052 |
| H | | 12.70 | | | 0.500 | | S | | 20.32 | | | 0.800 | |
| J | | 20.32 | | | 0.800 | | | | | | | | |

**Figure 6. Package Outline Drawing and Pinout.**

**Table 1. Regulatory Compliance–Typical Performance**

| Feature | Test Method | Performance |
|---|---|---|
| Electrostatic Discharge (ESD to the Electrical Pins) | MIL-STD-883C Method 3015.4 | Class 1 (>1000 V) |
| Electrostatic Discharge (ESD) to the Duplex SC Receptacle | Variation of IEC 801-2 | Products of this design typically withstand at least 25 kV without damage when the Duplex SC Connector Receptacle is contacted by a Human Body Model probe. |
| Electromagnetic Interference (EMI) | FCC Class B CENELEC EN55022 Class B (CISPR 22B) VCCI Class 2 | Typically provide TBD dB margin to FCC Class B and a TBD dB margin to the other noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. Margins above 1 GHz are dependent on customer board and chassis designs. |
| Immunity | Variation of IEC 801-3 | Typically show 1.3 dB penalty from a 3 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure. |
| Eye Safety | IEC 825/CDRH Class 1 | CDX2155 License pending. |

## Performance Specifications
## Absolute Maximum Ratings

| Parameter | Symbol | Minimum | Maximum | Units |
|---|---|---|---|---|
| Storage Temperature | $T_S$ | -40 | +85 | °C |
| Operating Temperature - CDX2155A/C | - | -40 | +85 | °C |
| Operating Temperature - CDX2155B/D | - | 0 | +70 | °C |
| Lead Soldering Temperature/Time | - | - | +240/10 | °C/s |
| Output Current (Other Outputs) | I out | 0 | 30 | mA |
| Input Voltage | - | GND | $V_{CC}$ | V |
| Power Supply Voltage | - | 0 | +6 | V |

## Operating Environment

| Parameter | Symbol | Minimum | Maximum | Units |
|---|---|---|---|---|
| Power Supply Voltage ECL Operation | $V_{CC}$ | -4.95 | -5.45 | V |
| Power Supply Voltage PECL Operation | $V_{CC}$ | +4.75 | +5.25 | V |
| Ambient Operating Temperature - CDX2155A/C | T op | -40 | +85 | °C |
| Ambient Operating Temperature - CDX2155B/D | T op | 0 | +70 | °C |

## Transmitter Section

(Ambient Operating Temperature, $V_{CC}$ = 4.75 V to 5.25 V)

| Parameter | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Output Center Wavelength | λce | 1261 | 1360 | nm | - |
| Output Spectral Width (RMS) | Δλ | - | 7.7 | nm | - |
| Average Optical Output Power | Po | -15 | -8.0 | dBm | 1 |
| Extinction Ratio | Er | 8.2 | - | dB | - |
| Power Supply Current | $I_{CC}$ | - | 140 | mA | 2 |
| Output Eye | Compliant with Bellcore TR-NWT-000253 and ITU recommendation | | | | |

## Receiver Section

(Ambient Operating Temperature, $V_{CC}$ = 4.75 V to 5.25 V)

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| Receiver Sensitivity | - | -28 | - | - | dBm | 3 |
| Maximum Input Power | - | -7.0 | - | - | dBm | - |
| Alarm ON | - | -42 | - | -31 | dBm | - |
| Hysteresis | - | 0.5 | - | 4.0 | dB | - |
| Power Supply Current | $I_{CC}$ | - | 180 | 290 | mA | 4 |
| Data Outputs | ECL/PECL | | | | | |
| Alarm Output | ECL/PECL | | | | | |
| Clock Outputs | ECL/PECL | | | | | |
| Jitter Tolerance | ITU G.958 Compliant | | | | | |

**Notes:**

1. Output power is power coupled into a single mode fiber.
2. The power supply current varies with temperature. Maximum current is specified at $V_{CC}$ = Maximum at maximum temperature (not including terminations) and end of life.
3. Minimum sensitivity and saturation levels for a $2^{23}$-1 PRBS with 72 ones and 72 zeros inserted. (ITU recommendation G.958).
4. The current excludes the output load current.

**Table 2. Pin Out Table**

| Pin | Symbol | Functional Description |
|---|---|---|
| Mounting Studs | | The mounting studs are provided for transceiver mechanical attachment to the circuit board. They are embedded in the nonconductive plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board. |
| 1 | Ref Clk | Reference Clock - Optional Feature<br>Reference Clock can be used as an optional, internally generated local receiver clock when the Input Optical Signal is disrupted. See Pin 2 Lck Ref- description. This input is not required for the normal operation of the Clock recovery circuit. This is a single-ended PECL input.<br><br>If this Reference Clock input is used, provide a 19.44 MHz external reference clock signal and terminate at this input pin with standard PECL techniques.<br><br>If this Reference Clock input is not used, leave the input open-circuited. With the input open-circuited, an internal pull-down resistor will bias this input to a low-state condition. |
| 2 | Lck Ref- | Lock-to-Reference Clock Bar - Optional Feature<br>Lock-to-Reference Clock Bar can be used to help manage the performance of the receiver when the Input Optical Signal is disrupted. When used, it places the received data outputs in static states and it triggers an internally generated local receiver clock to be output on Clk/Clk- in substitution of recovered clock. This is a single-ended PECL input.<br><br>For normal operation of the transceiver, connect this Lock-to-Reference-bar input to $V_{CC}$ or a PECL high-state ($V_{IH}$) which causes the internal CDR circuit to output recovered differential clock on Clk/Clk- and re-timed differential data on RD/RD-.<br><br>For optional use to make static the received data outputs and to output the internally generated local receiver clock, connect Lck Ref- input to a PECL low-state ($V_{IL}$), or leave this input open-circuited. When this is done it will cause: 1) the Received Data outputs to change to static PECL logic levels (RD = $V_{OL}$ and RD- = $V_{OH}$), 2) the internal CDR circuit to switch over to using the external reference clock, if provided, as the timing source to generate a 155.52 Mb/s clock output on Clk/Clk-. If the feature is used, one way to implement it is to connect this pin to Signal Detect directly with a single pull-down resistor of 10 kΩ to ground.<br><br>If this Lock-to-Reference feature is not used, this pin must be connected directly to $V_{CC}$ or a PECL high-state to disable it. |
| 3 | Clk- | Received Recovered Clock Out Bar<br>See pins 1 & 2 for optional, local generated clock output.<br><br>The rising edge occurs coincident with the edges of the Received Data output.<br>The falling edge occurs in the middle of the Received Data baud period.<br><br>Terminate this high-speed, differential clock output with standard PECL techniques at the clock input point of the follow-on device. |

**Table 2. Pin Out Table (continued)**

| Pin | Symbol | Functional Description |
|---|---|---|
| 4 | Clk+ | Received Recovered Clock Out<br>See pins 1 and 2 for optional, local generated clock output.<br><br>The falling edge occurs coincident with the edges of the Received Data output.<br>The rising edge occurs in the middle of the Received Data baud period.<br><br>Terminate this high-speed, differential clock output with standard PECL techniques at the clock input point of the follow-on device. |
| 5 | $L_{MON}(-)$ | Laser Bias Monitor (-)<br>This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver. |
| 6 | $L_{MON}(+)$ | Laser Bias Monitor (+)<br>This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver. |
| 7 | Txdis | Transmitter Disable<br>Transmitter Output Disabled: $V_{CCT} - 1.5\ V \le V_7 \le V_{CCT}$.<br>Transmitter Output Uncertain: $V_{CCT} - 4.2\ V \le V_7 \le V_{CCT} - 1.5\ V$.<br>Transmitter Output Enabled: $V_{EET} \le V_7 \le V_{CCT} - 4.2\ V$ or open circuit. |
| 8 | N/C | |
| 9 | $P_{MON}$ | Power Monitor<br>The analog voltage measured at this high impedance output provides an indication of whether the optical power output of the Laser Diode is operating within the normal specified power output range per the following relationships:<br>High Light Indication: $V_9 \le V_{EET} + 1.7\ V$.<br>Normal Operation: $V_9 \cong V_{EET} + 1.2\ V$.<br>Low Light Indication: $V_9 \le V_{EET} + 0.7\ V$. |
| 10 | $V_{EET}$ | Transmitter Signal Ground<br>Directly connect this pin to the transmitter signal ground plane. |
| 11 | TD+ | Transmitter Data In<br>Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin. |
| 12 | TD- | Transmitter Data In Bar<br>Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin. |
| 13 | $V_{CCT}$ | Transmitter Power Supply<br>Provide +5 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the $V_{CCT}$ pin. |
| 14 | $V_{CCR}$ | Receiver Power Supply<br>Provide + 5 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the $V_{CCR}$ pin. |

**Table 2. Pin Out Table (continued)**

| Pin | Symbol | Functional Description |
|---|---|---|
| 15 | SD | Signal Detect<br>Normal input optical levels to the receiver result in a logic "1" output.<br>Low input optical levels to the receiver result in a fault indication shown by a logic "0" output.<br><br>Signal Detect is a single-ended, low-power, PECL output. Since SD is a low-power PECL output, complete the interconnection of SD output with other PECL inputs using a 10 kΩ pull-down resistor to $V_{EE}$ to allow biasing of the interconnection. Do not load this SD output with standard PECL, 50 Ω to $V_{CC}$ - 2 V, termination. If Signal Detect output is not used, leave it open-circuited.<br><br>This signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input, Loss of Signal-bar input, or to optionally drive the Lock-to-Reference-bar input (pin 2) of this transceiver. |
| 16 | RD- | Retimed Receiver Data Out Bar<br>Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin. |
| 17 | RD+ | Retimed Receiver Data Out<br>Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin. |
| 18 | $V_{EER}$ | Receiver Signal Ground<br>Directly connect this pin to receiver signal ground plane. |

## Ordering Information

**CDX2155 X**

- A = -40/+85°C black
- B = 0/+70°C black
- C = -40/+85°C blue
- D = 0/+70°C blue

**Class 1 Laser Product:** This product conforms to the applicable requirements of 21 CFR 1040 at the date of manufacture

Date of Manufacture: _____

Hewlett-Packard Ltd., Whitehouse Road, Ipswich, England

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

**Americas/Canada:** 1-800-235-0312 or 408-654-8675

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