PDH ATM UNI Processor Product Overview

FEATURES

- Operates at rates up to 140 Mbps.
- Complies with the ATM Forum UNI specification 3.0, ITU specification G.804, ITU specification G.832, and Bellcore specification TR-TSV-000773.
- Provides integrated framers for DS3 (44.736 Mbps), E3 G.804 (34.368 Mbps), and E4 G.804 (139.264 Mbps).
- Provides ATM cells for DS1 (1.544 Mbps) or E1 (2.048 Mbps).
- Transfers ATM data through an 8-bit UTOPIA interface.
- Transfers DS3- and E3-formatted data through a synchronous, serial, Non-Return to Zero (NRZ) interface, and E3/E4-formatted data through a synchronous 8-bit interface.
- Provides access to the full DS3 PLCP, E3, and E4 data stream via a synchronous 8-bit interface.
- Provides built-in performance and alarm monitoring.
- Inserts and monitors Generic Flow Control (GFC) bits.
- Provides built-in error generation and loopback.
- Compatible with CMOS and TTL signals.
- Provides boundary scan capability and tristatable outputs for ATE testing.
- Available in 144-pin QFP.

DESCRIPTION

The WAC-034-B PDH ATM UNI Processor maps 53-byte ATM cells into a synchronous DS3, E3, or E4 payload. It is ideally suited for equipment in the wide area network, such as ATM switches, hubs, bridges, routers, workstations, and test equipment. This device can also be used with external circuitry in any application requiring a DS1 or E1 interface. Figure 1 shows a simple data flow diagram for DS3 applications.

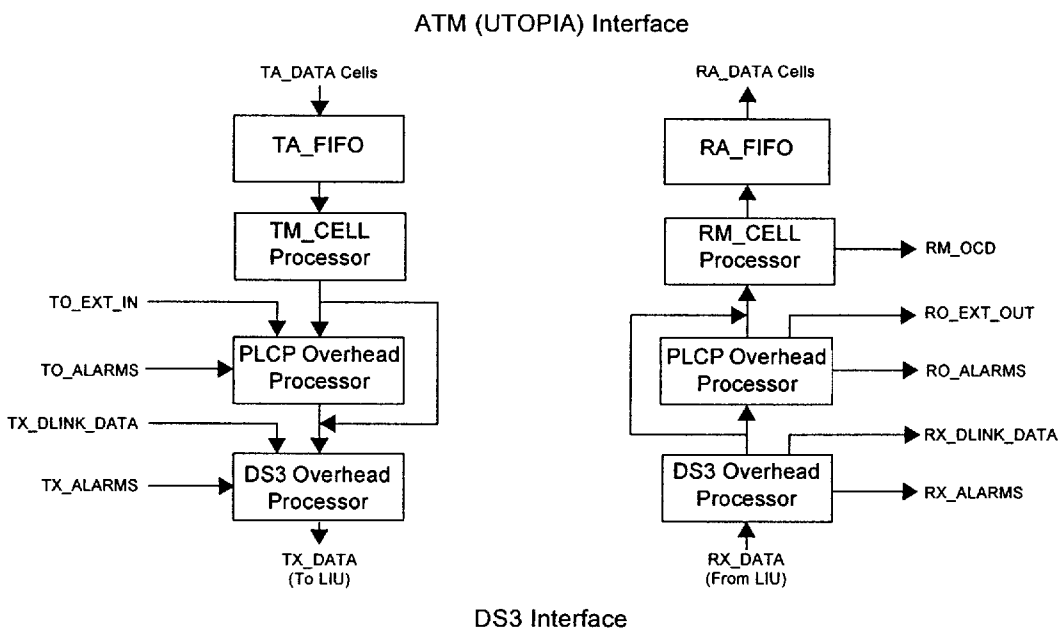

Figure 1. Simple Data Flow Diagram of the WAC-034-B for DS3 Applications

Figure 2 shows a simple data flow diagram for E3/E4 applications.

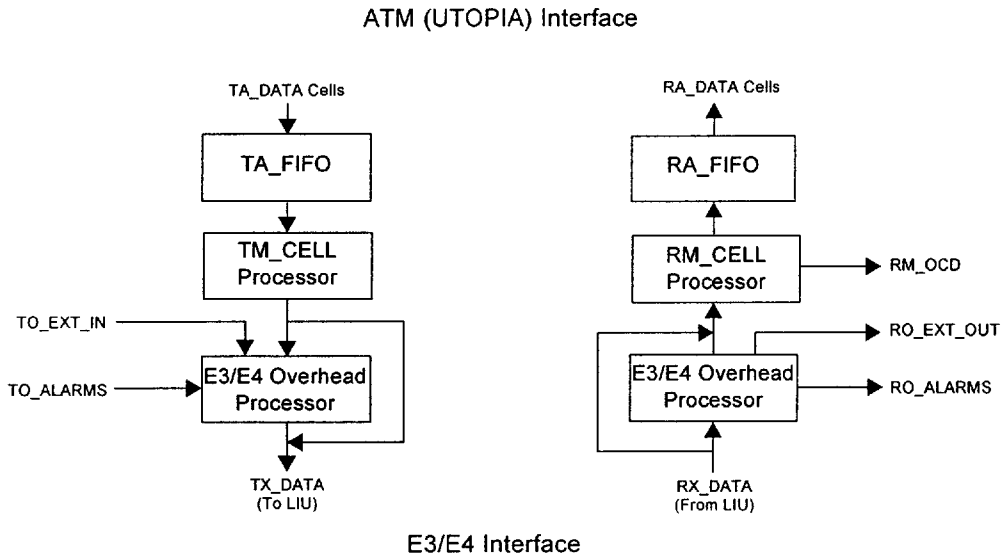

Figure 2. Simple Data Flow Diagram of the WAC-034-B for E3/E4 Applications

Figure 3 shows connection to a generic physical medium dependent layer.

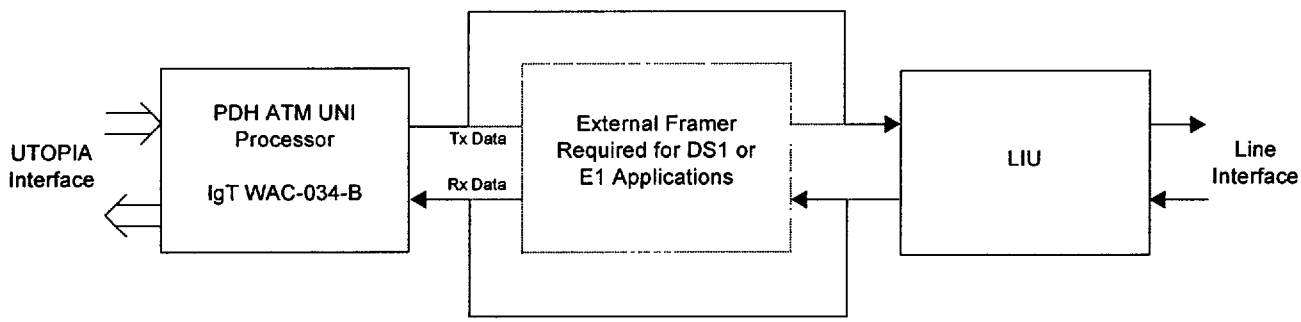

Figure 3. Generic Physical Medium Connection

DS3 APPLICATION

1. SYSTEM FEATURES

1. 1. Rates

- DS3 (44.736 Mbps).

1. 2. Setup

- Transmitter and receiver can be set up and accessed independently.

1. 3. Loopback

- Local: TX_SER_DATA and TX_SER_CLK is fed back to RX_SER_DATA and RX_SER_CLK.

1. 4. Testability

- All outputs are tristatable.
- Boundary scan (JTAG) on all pins except the serial data and clock signals.

1. 5. Framing Format

1. 5. 1. DS3 Format

The DS3 frame is composed of seven subframes. Table 1 and Table 2 show the overhead bits for the M13 and C-bit parity modes. Each subframe consists of eight blocks containing 85 bits each. The first bit in each block is a DS3 overhead bit.

Table 1. M13 DS3 Overhead Bits

X	[84]	F_1	[84]	C_{11}	[84]	F_0	[84]	C_{12}	[84]	F_0	[84]	C_{13}	[84]	F_1	[84]
X	[84]	F_1	[84]	C_{21}	[84]	F_0	[84]	C_{22}	[84]	F_0	[84]	C_{23}	[84]	F_1	[84]
P	[84]	F_1	[84]	C_{31}	[84]	F_0	[84]	C_{32}	[84]	F_0	[84]	C_{33}	[84]	F_1	[84]
P	[84]	F_1	[84]	C_{41}	[84]	F_0	[84]	C_{42}	[84]	F_0	[84]	C_{43}	[84]	F_1	[84]
M_0	[84]	F_1	[84]	C_{51}	[84]	F_0	[84]	C_{52}	[84]	F_0	[84]	C_{53}	[84]	F_1	[84]
M_1	[84]	F_1	[84]	C_{61}	[84]	F_0	[84]	C_{62}	[84]	F_0	[84]	C_{63}	[84]	F_1	[84]
M_0	[84]	F_1	[84]	C_{71}	[84]	F_0	[84]	C_{72}	[84]	F_0	[84]	C_{73}	[84]	F_1	[84]

NOTES:

- Each row represents a subframe.
- $F_1F_0F_0F_1$ is the frame alignment signal. $F_0 = 0$ and $F_1 = 1$.
- $M_0M_1M_0$ is the multiframe alignment signal. $M_0 = 0$ and $M_1 = 1$.
- P is the parity information calculated over all information bits in the preceding DS3 frame. Both P-bits equal 1 if the digital sum of all information bits is 1. Both P-bits equal 0 if the sum is 0.
- The X-bits may be used to transmit in-service messages. In any one DS3 frame the two X-bits must be identical and may not change more than once per second.
- $C_{11}C_{12}C_{13}$ = stuffing indicators for DS2 input 1.
  $C_{21}C_{22}C_{23}$ = stuffing indicators for DS2 input 2.
  $C_{31}C_{32}C_{33}$ = stuffing indicators for DS2 input 3.
  $C_{41}C_{42}C_{43}$ = stuffing indicators for DS2 input 4.
  $C_{51}C_{52}C_{53}$ = stuffing indicators for DS2 input 5.
  $C_{61}C_{62}C_{63}$ = stuffing indicators for DS2 input 6.
  $C_{71}C_{72}C_{73}$ = stuffing indicators for DS2 input 7.
- [84] represents 84 information bits between every DS3 overhead bit.

Table 2. C-bit Parity DS3 Overhead Bits

X	[84]	F_1	[84]	AIC	[84]	F_0	[84]	N_a	[84]	F_0	[84]	FEAC	[84]	F_1	[84]
X	[84]	F_1	[84]	User DL	[84]	F_0	[84]	User DL	[84]	F_0	[84]	User DL	[84]	F_1	[84]
P	[84]	F_1	[84]	CP	[84]	F_0	[84]	CP	[84]	F_0	[84]	CP	[84]	F_1	[84]
P	[84]	F_1	[84]	FEBE	[84]	F_0	[84]	FEBE	[84]	F_0	[84]	FEBE	[84]	F_1	[84]
M_0	[84]	F_1	[84]	DL	[84]	F_0	[84]	DL	[84]	F_0	[84]	DL	[84]	F_1	[84]
M_1	[84]	F_1	[84]	User DL	[84]	F_0	[84]	User DL	[84]	F_0	[84]	User DL	[84]	F_1	[84]
M_0	[84]	F_1	[84]	User DL	[84]	F_0	[84]	User DL	[84]	F_0	[84]	User DL	[84]	F_1	[84]

NOTES:

- Each row represents a subframe.
- $F_1F_0F_0F_1$ is the frame alignment signal. $F_0 = 0$ and $F_1 = 1$.
- $M_0M_1M_0$ is the multiframe alignment signal. $M_0 = 0$ and $M_1 = 1$.
- P is the parity information calculated over all information bits in the preceding DS3 frame. Both P-bits equal 1 if the digital sum of all information bits is 1. Both P-bits equal 0 if the sum is 0.
- The X-bits are used to transmit a Yellow Alarm. In any one DS3 frame the two X-bits must be identical and may not change more than once per second.
- C-bit definitions:
  AIC = Application Identification Channel = 1.
  N_a = Reserved Network Application Bit = 1.
  FEAC = Far-End Alarm and Control Channel.
  DL = Data Link.
  User DL = User Defined Data Link = 1.
  CP = C-bit Parity.
  FEBE = Far-End Block Error.
- [84] represents 84 information bits between every DS3 overhead bit.

1. 5. 2. PLCP Format

The Physical Layer Convergence Protocol (PLCP) for DS3 is shown in Figure 4. *Inactive* overhead bytes (bytes not processed by the WAC-034-B) are shown in the shaded squares. These bytes are transmitted as 00_h and are ignored by the receiver. *Active* overhead bytes (bytes processed by the WAC-034-B) are summarized in Table 3. The trailer may be 13 or 14 nibbles in length and is used to frequency justify the 125 µs PLCP frame. The contents of each trailer nibble is 1100. Descriptions of the processing performed on each one of the active bytes is given in section "2. Transmitter Features" on page 10 and in section "3. Receiver Features" on page 12. .

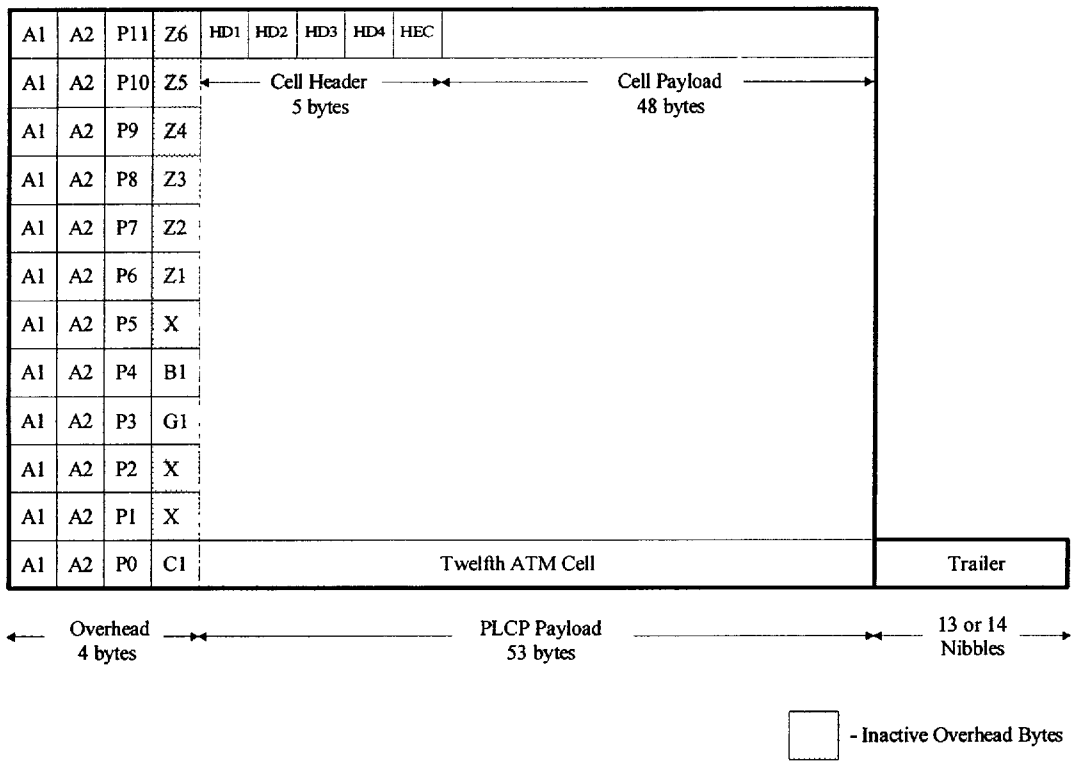

Figure 4. DS3 PLCP Format

Table 3 describes the values used for coding the DS3 overhead bytes. Bits are shown in parentheses; bit 7 is the most significant bit and is the first bit to be transmitted in the data stream, and bit 0 is the least significant bit and is the last bit to be transmitted in the data stream. For example, the first four bits of the G1 byte are indicated as G1(7:4). This numbering scheme maintains consistency between the pin descriptions and the microprocessor port register descriptions. Default values used by the transmitter are indicated by (def).

Table 3. Values for the DS3 Overhead Bytes

Overhead Byte Location	Function	Value
A1	Frame alignment	$F6_h$
A2	Frame alignment	28_h
P11	Path Overhead Identifier	$2C_h$
P10	Path Overhead Identifier	29_h
P9	Path Overhead Identifier	25_h
P8	Path Overhead Identifier	20_h
P7	Path Overhead Identifier	$1C_h$
P6	Path Overhead Identifier	19_h
P5	Path Overhead Identifier	15_h
P4	Path Overhead Identifier	10_h
P3	Path Overhead Identifier	$0D_h$
P2	Path Overhead Identifier	08_h
P1	Path Overhead Identifier	04_h
P0	Path Overhead Identifier	01_h
B1	Error monitoring	BIP-8
G1(7:4)	FEBE	B1 error count
G1(3)	No alarm Failure condition	0 (def) 1
G1(2:0)	Inactive bits	000
C1	Identify first frame phase Identify second frame phase Identify third frame phase, no stuffing Identify third frame phase, stuff	FF_h 00_h 66_h 99_h

2. TRANSMITTER FEATURES

2. 1. General

2. 1. 1. Data Insertion

- The default values for all PLCP data, including the overhead, can be overwritten with a synchronous 8-bit interface.

2. 1. 2. Error Insertion

- Single and continuous error insertion capabilities are valid for all bytes specified as having a general error insertion feature.

2. 1. 3. Automatic Alarm Generation

- Dedicated internal circuitry or an external signal will generate the appropriate alarm signal upon detection of an alarm condition (for example, a Far-End Block Error - FEBE).
- Software can force alarm signal generation.

2. 2. ATM

- Provides a three cell deep, cell-by-cell FIFO to decouple system and line side clocks.
- Generates null cells with programmable headers and programmable one-byte payload patterns.
- Optionally generates Header Error Check (HEC) with error insertion on any bits.
- Optionally generates the HEC without the coset pattern.
- Optionally scrambles the cell payload.
- Counts the number of message cells transmitted.
- Detects transmit FIFO empty and begins sending a null cell immediately.

2. 3. PLCP Overhead Processing

- Optionally disables PLCP overhead processing.
- Generates A1 and A2 with continuous error insertion on the most significant bit (bit 7) of the A1 and A2 bytes.
- Generates B1 (BIP-8) with error insertion on all 8 bits simultaneously.
- Generates Path Overhead Indentifier (POI) coding to index the adjacent Path Overhead (POH) bytes.
- Automatically generates G1 FEBE on reception of B1 byte errors.
- Generates G1 Remote Alarm Indication (RAI) when the G1_RAI signal is asserted.
- Generates C1 code to indicate nibble stuffing cycle.
- Optionally generates external or looped nibble stuffing.
- Generates a frame pulse to indicate start-of-frame (TO_FRAME).
- Synchronizes the frame format to an external frame sync signal (TO_FRAME_IN).

2. 4. DS3 Frame Overhead Processing

- Optionally generates C-bit parity or M13 framing.
- Generates frame bits (F-bits and M-bits) with single error insertion per frame (F-bits only).
- Generates X-bits with microprocessor control.
- Generates parity bits (P-bits) with single error insertion.
- Generates programmable FEAC codes.
- Generates C-bit Parity bits (CP-bits) with single error insertion.
- Automatically generates FEBEs when F-bit, M-bit, or CP-bit errors are received.
- Generates the Alarm Indication Signal (AIS) pattern. An AIS signal is defined as a signal with all of the following conditions:
  - all C-bits are set to 0,
  - both X-bits are set to 1, and
  - the information bits are set to 1010 and synchronized to the framing bits.
- Generates the Idle signal pattern. An Idle signal is defined as a signal with all of the following conditions:
  - all three C-bits in the subframe three are set to 0,
  - both X-bits are set to 1, and
  - the information bits are set to 1100 and synchronized to the framing bits.
- Generates a frame pulse to indicate start-of-frame (TX_FRAME).
- Synchronizes the frame format to an external frame sync signal (TO_FRAME_IN).

2. 5. Line Interface Processing

- Generates Loss Of Signal (LOS), which forces the transmit data stream to 0.
- Generates B3ZS coding.
- Optionally generates single Bipolar Violations (BPVs).

3. RECEIVER FEATURES

3. 1. General

3. 1. 1. Plesiochronous Digital Hierarchy (PDH) Data Monitoring

- Monitors the full descrambled PLCP data stream, including all the overhead bytes, through a synchronous 8-bit interface.

3. 1. 2. Counters

- Counter length is 16 bits.
- Counters are latched synchronously and cleared when latched.

3. 1. 3. Alarms

- One hardware pin is associated with each alarm.
- One interrupt is generated with each alarm. Each interrupt has three microprocessor bits: mask, interrupt, and status.

3. 2. ATM

- Provides a three cell deep, cell-by-cell FIFO to decouple system and line side clocks.
- Performs cell delineation by checking for HEC matches.
- Detects out-of-cell delineation (RM_OCD) in accordance to ITU Recommendation I.432 (refer to "Appendix B. References" on page 123), where delta is 6 and alpha is 7.
- Detects FIFO overflow with RM_FIFO_OVERFLOW_INTR.
- Optionally corrects the first header containing a single apparent bit error (Correction Mode for ATM cell header processing).
- Optionally disables coset function in HEC calculation.
- Optionally passes cells with invalid HECs.
- Optionally passes unassigned cells. (Unassigned cells have the following five header bytes, $X000000XXX_h$, where X is any hexadecimal digit).
- Optionally passes data during receive out-of-cell delineation.
- Optionally descrambles the cell payload.
- Counts complete cells written to the receive FIFO.
- Counts all cells with invalid HECs in Detection Mode for ATM cell header processing, and counts all cells with uncorrectable HECs in Correction Mode.

3. 3. PLCP Overhead Processing

- Optionally disables PLCP overhead processing.
- Detects *Out-Of-Frame* (RO_OOF).

  RO_OOF is set if:

  - An error is detected in both A1 and A2 bytes, or
  - Two consecutive, invalid, and nonsequential POI bytes are detected.

  RO_OOF is reset if two consecutive valid A1 and A2 bytes with two consecutive, valid, and sequential POI bytes are detected.
- Detects *Loss-Of-Frame* (RO_LOF).

  RO_LOF is set if 1 ms of OOF is accumulated with fewer than 1 ms of in-frame between OOFs.
  RO_LOF is reset if 12 consecutive ms of in-frame are detected.
- Counts A1, A2, and POI errors.
- Optionally counts B1 (BIP-8) errors individually or as a block.
- Detects G1 RAI.

  G1_RAI is set if 10 consecutive G1 bytes are set to XXXX1XXX
  G1_RAI is reset if 10 consecutive G1 bytes are set to XXXX0XXX
- Counts G1 FEBEs.

3. 4. DS3 Frame Overhead Processing

- Detects *Out_Of_Frame* (RX_OOF) with optional criteria.
  RX_OOF is set if:

  - Three out of 15 F-bits are in error, or
  - Six out of 15 F-bits are in error, or
  - Two out of three M-bits are in error.

  RX_OOF is reset if two consecutive frames with correct 010 M-bit sequences are detected. Search for the M-bit sequences begins after detection of 15 consecutive error-free F-bits.
- Counts frame (F-bit and M-bit) errors.
- Counts parity (P-bit) errors.
- Counts C-bit parity (CP-bit) errors.
- Counts FEBEs.
- Provides microprocessor access to X-bit status.
- Detects changes in Far-End Alarm and Control (FEAC) code and provides microprocessor access to FEAC code.
- Detects Yellow Alarm when both X-bits are 0.
- Detects the AIS 1010 signal condition. An AIS 1010 signal is defined as a signal with the following conditions:

  - both X-bits are set to 1, and
  - the information bits are set to 1010 and synchronized to the framing bits.
- Detects the AIS Stuck C-bit condition. An AIS Stuck C-bit condition is defined as a signal with the following conditions:

  - all C-bits are set to 0, and
  - both X-bits are set to 1.

- Detects the Idle signal pattern. An Idle signal is defined as a signal with the following conditions:
  - all three C-bits in subframe three are set to 0,
  - both X-bits are set to 1, and
  - the information bits are set to 1100 and synchronized to the framing bits.

3. 5. Line Interface Processing

- Detects *Loss-Of-Signal* (RX_LOS).
  RX_LOS is valid if incoming data is stuck at all 0s or all 1s for a period of 175 ± 75 contiguous bit positions.
  RX_LOS is reset on the detection of an average pulse density of at least 33 percent over a period of 175 ± 75 contiguous bit positions.
- Provides B3ZS decoding.
- Counts BPVs as line code violations.
- Optionally counts excess 0s as line code violations.

4. PIN DESCRIPTIONS

4. 1. Package Diagram

Figure 5 shows the physical dimensions for the 144-pin plastic quad flat pack used for the WAC-034-B.

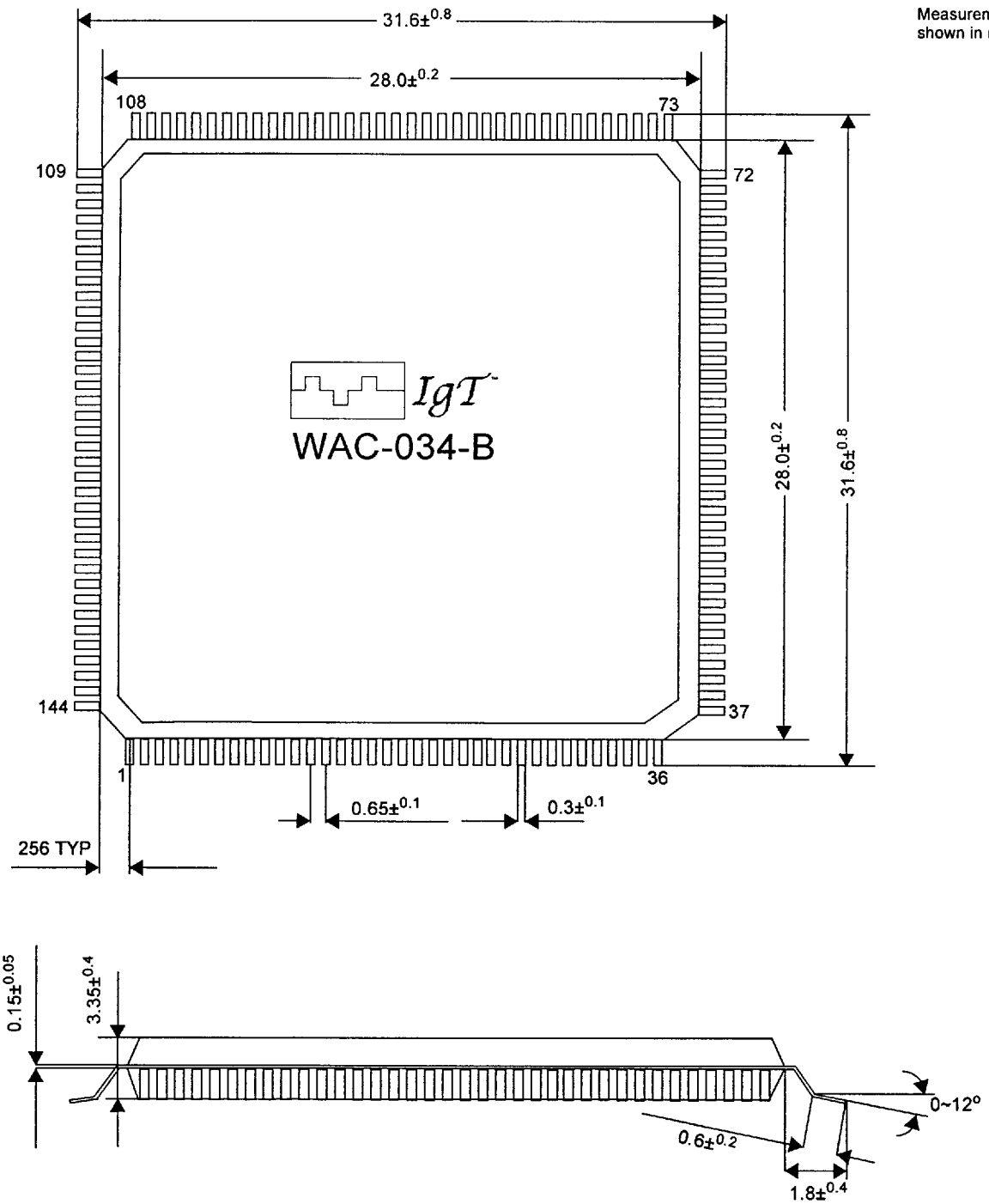

Figure 5. WAC-034-B Package (PQFP-144)

4. 2. Pin Locations

Refer to Table A-1 on page 121 for prefix name explanations.

Table 4. Pin Locations

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	/CS	37	VCC	73	VCC	109	VCC
2	/RD	38	RPHY_SOC	74	SER_IO_EN	110	E3 OUT
3	/WR	39	RPHY_CLAV	75	RX_SER_DATA-	111	E3 OUT
4	A0	40	/RPHY_AEMPTY	76	RX_SER_DATA+	112	TX_PAR_CLK_OUT
5	A1	41	RO_TR_EN	77	GND	113	TO_FRAME
6	A2	42	SCAN_TCK	78	N/C	114	TO_FRAME_IN
7	A3	43	SCAN_TMS	79	RX_SER_CLK	115	TO_INSERT
8	A4	44	SCAN_TDI	80	GND	116	TO_EXT_IN0
9	A5	45	SCAN_TDO	81	N/C	117	TO_EXT_IN1
10	N/C	46	RO_EXT_OUT0	82	E3 IN	118	TO_EXT_IN2
11	N/C	47	RO_EXT_OUT1	83	E3 IN	119	TO_EXT_IN3
12	D0	48	RO_EXT_OUT2	84	E3 IN	120	TO_EXT_IN4
13	D1	49	RO_EXT_OUT3	85	E3 IN	121	TO_EXT_IN5
14	D2	50	RO_EXT_OUT4	86	E3 IN	122	TO_EXT_IN6
15	D3	51	RO_EXT_OUT5	87	E3 IN	123	TO_EXT_IN7
16	D4	52	RO_EXT_OUT6	88	E3 IN	124	TX_DLINK_DATA
17	D5	53	RO_EXT_OUT7	89	E3 IN	125	TX_DLINK_CLK
18	GND	54	GND	90	E3 IN 126	126	GND
19	VCC	55	VCC	91	N/C	127	VCC
20	D6	56	RM_OCD	92	GND	128	TO_RAI
21	D7	57	RX_DLINK_DATA	93	TX_AIS	129	ADDR_LAT_EN
22	INTR	58	/TPHY_AEMPTY	94	TX_SER_CLK	130	TX_FRAME
23	/RESET	59	RX_DLINK_CLK	95	VCC	131	/TPHY_WRITE_EN
24	OUTPUT_EN	60	RX_OOF	96	GND	132	TPHY_SOC
25	RPHY_DATA0	61	RO_EN	97	TX_SER_DATA+	133	TPHY_CLK
26	RPHY_DATA1	62	RX_FRAME	98	TX_SER_DATA-	134	TPHY_DATA0
27	RPHY_DATA2	63	RO_RAI	99	GND	135	TPHY_DATA1
28	RPHY_DATA3	64	RX_AIS	100	VCC	136	TPHY_DATA2
29	GND	65	GND	101	E3 IN	137	TPHY_DATA3
30	RPHY_DATA4	66	RX_LOS	102	E3 OUT	138	TPHY_DATA4
31	RPHY_DATA5	67	RO_OOF	103	E3 OUT	139	TPHY_DATA5
32	RPHY_DATA6	68	RO_LOF	104	E3 OUT	140	TPHY_DATA6
33	RPHY_DATA7	69	RO_FRAME	105	E3 OUT	141	TPHY_DATA7
34	/RPHY_READ_EN	70	RX_PAR_CLK_OUT	106	E3 OUT	142	TO_EXT_STUFF
35	RPHY_CLK	71	/SCAN_TRSTN	107	E3 OUT	143	TPHY_CLAV
36	GND	72	N/C	108	GND	144	GND

Figure 6 displays the pins of the WAC-034-B grouped by logical functions. Arrows heading toward the device are input pins, those heading away from the device are output pins, and those heading both toward and away from the device are bidirectional pins. Larger arrows are buses (multiple pins).

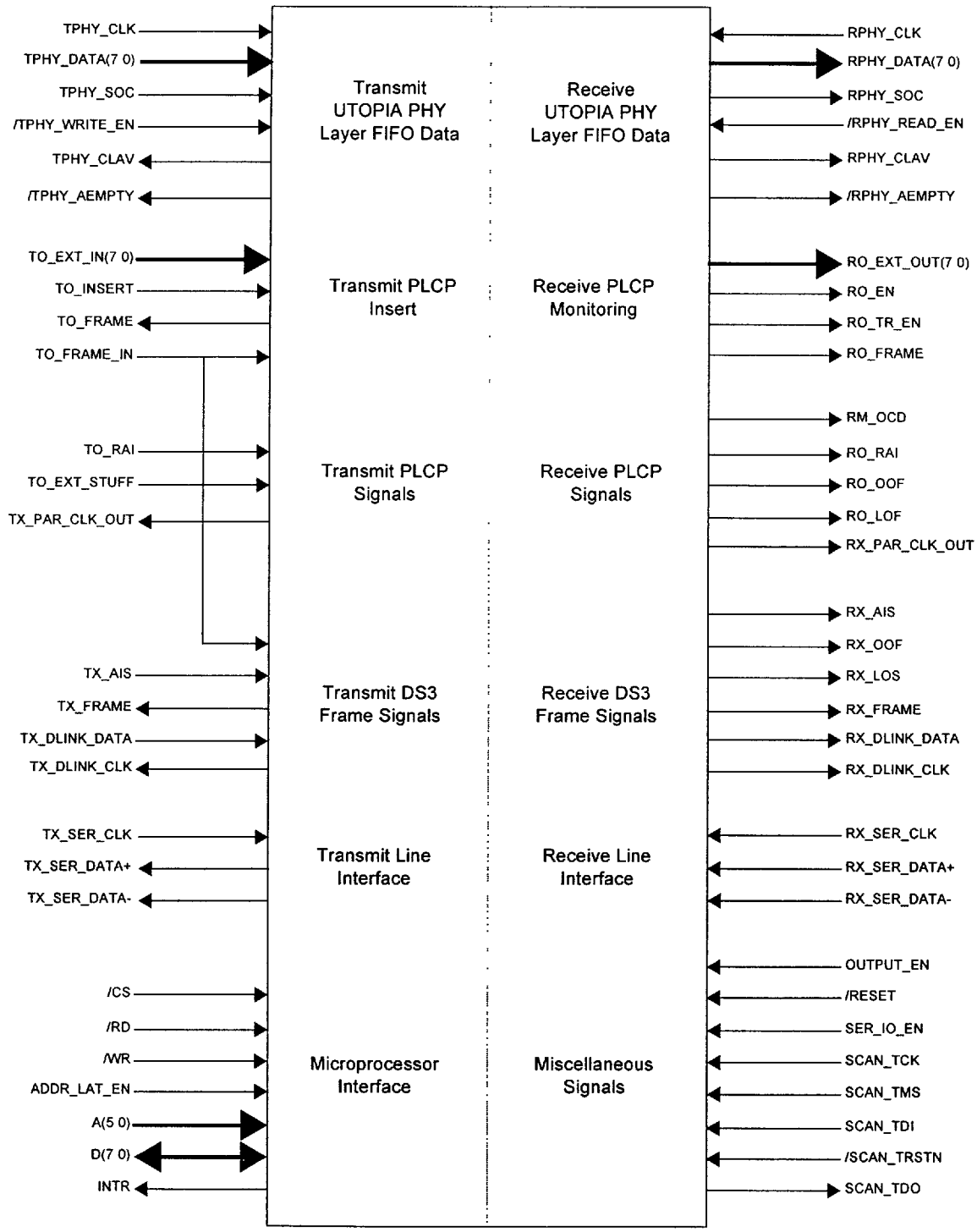

Figure 6. WAC-034-B Logical Pin Diagram for DS3 Applications

4. 3. Pin Descriptions

Refer to Table A-1 on page 121 for pin name prefix explanations.

4. 3. 1. UTOPIA PHY Layer FIFO Data Signals

4. 3. 1. 1. Transmit UTOPIA PHY Layer FIFO Data Signals

Table 5. Transmit UTOPIA PHY Layer FIFO Data Signals

Signal Name	Pin #	Type	Description
TPHY_CLK	133	In	*Transmit UTOPIA PHY Layer Clock* is used to write data from the ATM layer into the transmit ATM FIFO.
TPHY_DATA(7:0)	141 - 134	In	*Transmit UTOPIA PHY Layer Data Bits 7 to 0* are part of the 8-bit ATM data byte being written into the transmit ATM FIFO. Bit 7 is the first bit transmitted once the parallel byte is serialized. Bit 0 is the last bit transmitted once the parallel byte is serialized.
TPHY_SOC	132	In	*Transmit UTOPIA PHY Layer Start-Of-Cell* indicates that the data being written into the transmit ATM FIFO is the first byte of the 53-byte ATM cell.
/TPHY_WRITE_EN	131	In	*Transmit UTOPIA PHY Layer Write Enable* is an active low signal used to enable writing data into the transmit ATM FIFO.
TPHY_CLAV	143	Out	*Transmit UTOPIA PHY Layer Cell Available* is an active high signal used to indicate that the transmit ATM FIFO can accept a complete cell. When this signal is low, the transmit ATM FIFO is able to accept at most four more bytes of data before it becomes full.
/TPHY_AEMPTY	58	Out	*Transmit UTOPIA PHY Layer FIFO Almost Empty* is an active low signal used to indicate that the transmit ATM FIFO has fewer than 51 bytes of data left. Note that this signal is synchronous to TX_PAR_CLK and not to TPHY_CLK.

4. 3. 1. 2. Receive UTOPIA PHY Layer FIFO Data Signals

Table 6. Receive UTOPIA PHY Layer FIFO Data Signals

Signal Name	Pin #	Type	Description
RPHY_CLK	35	In	*Receive UTOPIA PHY Layer Clock* is used by the ATM layer to read data from the receive ATM FIFO.
RPHY_DATA(7:4) RPHY_DATA(3:0)	33 - 30 28 - 25	Out	*Receive UTOPIA PHY Layer Data Bits 7 to 0* are part of the 8-bit ATM data byte being read from the receive ATM FIFO. Bit 7 is the first bit received once the parallel byte is serialized. Bit 0 is the last bit received once the parallel byte is serialized.
RPHY_SOC	38	Out	*Receive UTOPIA PHY Layer Start-of-Cell* indicates that the data being read from the receive ATM FIFO is the first byte of the 53-byte ATM cell.
/RPHY_READ_EN	34	In	*Receive UTOPIA PHY Layer Read Enable* is an active low signal used to indicate that the ATM layer is reading data from the receive ATM FIFO.
RPHY_CLAV	39	Out	*Receive UTOPIA PHY Layer Cell Available* is an active high signal used to indicate that the receive ATM FIFO contains a full cell (53 or more bytes).
/RPHY_AEMPTY	40	Out	*Receive UTOPIA PHY Layer Almost Empty* is an active low signal used to indicate that the receive ATM FIFO contains fewer than 50 bytes.

4. 3. 2. PLCP Signals

4. 3. 2. 1. Transmit PLCP Insert Signals

Table 7. Transmit PLCP Insert Signals

Signal Name	Pin #	Type	Description
TO_EXT_IN7	123	In	*Transmit Overhead External In Bit 7* is bit 7 of the 8-bit parallel data that can overwrite the default PLCP data stream. This pin can also be used to overwrite GFC3 of each cell when GFC_EN ($A=00_h$,D5) is a 1 and GFC_MASK3 ($A=0A_h$, D7) is a 1. This is the first bit transmitted once the parallel byte is serialized.
TO_EXT_IN6	122	In	*Transmit Overhead External In Bit 6* is bit 6 of the 8-bit parallel data that can overwrite the default PLCP data stream. This pin can also be used to overwrite GFC2 of each cell when GFC_EN ($A=00_h$, D5) is a 1 and GFC_MASK2 ($A=0A_h$, D6) is a 1.
TO_EXT_IN5	121	In	*Transmit Overhead External In Bit 5* is bit 5 of the 8-bit parallel data that can overwrite the default PLCP data stream. This pin can also be used to overwrite GFC1 of each cell when GFC_EN ($A=00_h$, D5) is a 1 and GFC_MASK1 ($A=0A_h$, D5) is a 1.
TO_EXT_IN4	120	In	*Transmit Overhead External In Bit 4* is bit 4 of the 8-bit parallel data that can overwrite the default PLCP data stream. This pin can also be used to overwrite GFC0 of each cell when GFC_EN ($A=00_h$, D5) is a 1 and GFC_MASK0 ($A=0A_h$, D4) is a 1.

Table 7. Transmit PLCP Insert Signals (Continued)

Signal Name	Pin #	Type	Description
TO_EXT_IN(3:0)	119 - 116	In	*Transmit Overhead External In Bits 3 to 0* are bits 3 to 0 of the 8-bit parallel data that can overwrite the default PLCP data stream. Bit 0 is the last bit transmitted once the parallel byte is serialized.
TO_INSERT	115	In	*Transmit Overhead Insert* indicates that the current *Transmit Overhead External In* (TO_EXT_IN) byte should overwrite the default PLCP data stream.
TO_FRAME	113	Out	*Transmit Overhead Frame* is an active high signal which indicates that a PLCP frame has been transmitted.
TO_FRAME_IN	114	In	*Transmit Overhead Frame Input* is an active high signal which can be asserted to synchronize the PLCP and DS3 frame generators to an external event.

4. 3. 2. 2. Transmit PLCP Signals

Table 8. Transmit PLCP Signals

Signal Name	Pin #	Type	Description
TO_RAI	128	In	*Transmit Overhead Remote Alarm Indication* inserts RAI into the transmit data stream.
TO_EXT_STUFF	142	In	*Transmit Overhead External Stuff* indicates that stuffing should occur in the third frame of the PLCP when the TO_STUFF_LOOP ($A=0B_h$, D3) is disabled.
TX_PAR_CLK_OUT	112	Out	*Transmit Parallel Clock Out* is equivalent to *Transmit Serial Clock* (TX_SER_CLK) divided by eight.

4. 3. 2. 3. Receive PLCP Monitoring Signals

Table 9. Receive PLCP Monitoring Signals

Signal Name	Pin #	Type	Description
RO_EXT_OUT7	53	Out	*Receive Overhead External Out Bit 7* is bit 7 of the 8-bit PLCP data when GFC_EN (Addr=00_h, D5) is a 0. This pin is used to report GFC3 of each valid cell when GFC_EN is a 1. This bit is the first bit received once the parallel byte is serialized. If GFC_EN is a 0, then the *Receive Overhead External Out* signals, in conjunction with *Receive Overhead Frame* (RO_FRAME), *Receive Overhead Enable* (RO_EN), and *Receive Overhead Trailer Enable* (RO_TR_EN), can be used to monitor the PLCP overhead data.
RO_EXT_OUT6	52	Out	*Receive Overhead External Out Bit 6* is bit 6 of the 8-bit PLCP data when GFC_EN (Addr=00_h, D5) is a 0. This pin is used to report GFC2 of each valid cell when GFC_EN is a 1.
RO_EXT_OUT5	51	Out	*Receive Overhead External Out Bit 5* is bit 5 of the 8-bit PLCP data when GFC_EN (Addr=00_h, D5) is a 0. This pin is used to report GFC1 of each valid cell when GFC_EN is a 1.

Table 9. Receive PLCP Monitoring Signals (Continued)

Signal Name	Pin #	Type	Description
RO_EXT_OUT4	50	Out	*Receive Overhead External Out Bit 4* is bit 4 of the 8-bit PLCP data when GFC_EN (Addr=00_h, D5) is a 0. This pin is used to report GFC0 of each valid cell when GFC_EN is a 1.
RO_EXT_OUT(3:0)	49 - 46	Out	*Receive Overhead External Out Bits 3 to 0* are bits 3 to 0 of the 8-bit PLCP data. Bit 0 is the last bit received once the parallel byte is serialized.
RO_EN	61	Out	*Receive Overhead Enable* indicates that the current *Receive Overhead External Out* (RO_EXT_OUT) is a PLCP overhead byte.
RO_TR_EN	41	Out	*Receive Overhead Trailer Enable* indicates that the current *Receive Overhead External Out* (RO_EXT_OUT) contains the trailer nibbles.
RO_FRAME	69	Out	*Receive Overhead Frame* is an active high signal asserted to indicate that a PLCP framing pattern was detected. This frame pulse is asserted three clock cycles after the frame byte A2 appears at *Receive Overhead External Out* (RO_EXT_OUT).

4. 3. 2. 4. Receive PLCP Signals

Table 10. Receive PLCP Signals

Signal Name	Pin #	Type	Description
RM_OCD	56	Out	*Receive Mapper Out-of-Cell Delineation* indicates that the receiver has lost ATM cell delineation.
RO_RAI	63	Out	*Receive Overhead Remote Alarm Indication* indicates that the receiver is detecting RAI.
RO_OOF	67	Out	*Receive Overhead Out-Of-Frame* indicates that the receiver for the PLCP layer is out-of-frame.
RO_LOF	68	Out	*Receive Overhead Loss-Of-Frame* indicates that the receiver for the PLCP layer has entered the loss-of-frame alarm state.
RX_PAR_CLK_OUT	70	Out	*Receive Parallel Clock Out* is equivalent to *Receive Serial Clock* (RX_SER_CLK) divided by eight.

4. 3. 3. DS3 Frame Signals

4. 3. 3. 1. Transmit DS3 Frame Signals

Table 11. Transmit DS3 Frame Signals

Signal Name	Pin #	Type	Description
TX_AIS	93	In	*Transmit Alarm Indication Signal* inserts the AIS into the transmit data stream.
TX_FRAME	130	Out	*Transmit Frame* is an active high signal which indicates that a DS3 frame has been transmitted.
TX_DLINK_DATA	124	In	*Transmit Data Link Data* is data inserted from an external source for transmission on the DS3 data link (the C-bits in subframe 5).
TX_DLINK_CLK	125	Out	*Transmit Data Link Clock* is a 28.2 kHz clock used by external circuitry to generate LAP-D formatted packets for data link channel communications.

4. 3. 3. 2. Receive DS3 Frame Signals

Table 12. Receive DS3 Frame Signals

Signal Name	Pin #	Type	Description
RX_AIS	64	Out	*Receive Alarm Indication Signal* indicates that the receiver is detecting AIS.
RX_OOF	60	Out	*Receive Out-of-Frame* indicates that the DS3 framer is out-of-frame.
RX_LOS	66	Out	*Receive Loss-of-Signal* indicates that the receiver is detecting loss-of-signal (the incoming data is stuck at 1 or 0).
RX_FRAME	62	Out	*Receive Frame* is an active high signal that marks the location of the first bit of the DS3 frame within the *Receive PHY Layer Serial Data* (RX_SER_DATA).
RX_DLINK_DATA	57	Out	*Receive Data Link Data* is the C-bits which have been extracted from subframe 5 of each incoming DS3 frame.
RX_DLINK_CLK	59	Out	*Receive Data Link Clock* is a 28.2 kHz clock which clocks out the *Receive Data-Link Data* (RX_DLINK_DATA).

4. 3. 4. Line Interface Signals

4. 3. 4. 1. Transmit Line Interface Signals

Table 13. Transmit Line Interface Signals

Signal Name	Pin #	Type	Description
TX_SER_CLK	94	In	*Transmit Serial Clock* is the serial clock used to generate *Transmit Serial Data* (TX_SER_DATA). This clock's frequency is 44.736 MHz for DS3.
TX_SER_DATA+	97	Out	*Transmit Serial Data Plus* is the Non-Return to Zero (NRZ) data when Bipolar is disabled, and represents a positive B3ZS-encoded pulse when Bipolar is enabled.
TX_SER_DATA-	98	Out	*Transmit Serial Data Minus* is the inverted NRZ data when bipolar is disabled, and represents a negative B3ZS-encoded pulse when bipolar is enabled.

4. 3. 4. 2. Receive Line Interface Signals

Table 14. Receive Line Interface Signals

Signal Name	Pin #	Type	Description
RX_SER_CLK	79	In	*Receive Serial Clock* is the serial clock used to write serial data into the receiver. This clock's frequency is 44.736 MHz for DS3.
RX_SER_DATA+	76	In	*Receive Serial Data Plus* is the serial data stream that is written into the receiver. This signal is NRZ data when bipolar is disabled, and represents the positive half of the B3ZS encoded pulse when Bipolar is enabled.
RX_SER_DATA-	75	In	*Receive Serial Data Minus* is the negative half of the B3ZS encoded signal that is written into the receiver when Bipolar is enabled.

4. 3. 5. Microprocessor Interface Signals

Table 15. Microprocessor Interface Signals

Signal Name	Pin #	Type	Description
/CS	1	In	*Chip Select* is an active low signal used to select the device.
/RD	2	In	*Read* is an active low read signal from the external microprocessor.
/WR	3	In	*Write* is an active low write signal from the external microprocessor.
ADDR_LAT_EN	129	In	*Address Latch Enable* is used to latch the value of the bus. A high value enables the internal transparent latches on the address bus. The value on the address bus is latched on the falling edge of address latch enable. If not used, this signal should be tied high.
A(5:0)	9 - 4	In	*Address Bits 5 to 0* are bits 5 to 0 of the 6-bit microprocessor address bus.
D(7:6) D(5:0)	21 - 20 17 - 12	Bi	*Data Bits 7 to 0* are bits 7 to 0 of the 8-bit microprocessor data bus.
INTR	22	Out	*Interrupt* goes high when an alarm condition is detected. Each condition is independently maskable. *Interrupt* goes low after all INTR read ports are read.

4. 3. 6. Miscellaneous Signals

Table 16. Miscellaneous Signals

Signal Name	Pin #	Type	Description
OUTPUT_EN	24	In	*Output Enable* is an active high signal used to enable all output signals. A low on this signal forces all output pins into a high impedance state.
/RESET	23	In	*Reset* is an active low signal used to force all microprocessor write ports to the default setting, and to reset both the transmitter and the receiver.
SER_IO_EN	74	In	*Serial Input/Output Enable* is used to enable the serial PDH section input/output streams. When *Serial Input/Output Enable* is high, the PDH interface is configured to handle serial I/O. When *Serial Input/Output Enable* is low, the PDH interface is configured to handle parallel I/O. For DS3, *Serial Input/Output Enable* **must** be set high.
SCAN_TCK	42	In	*Scan Test Clock* is an independent clock used to drive the internal boundary scan test logic. This signal should be connected to +5 volts through a pull-up resistor.
SCAN_TMS	43	In	*Scan Test Mode Select* controls the operation of the internal boundary scan test logic. This signal should be connected to +5 volts through a pull-up resistor.
SCAN_TDI	44	In	*Scan Test Data Input* is the serial input for boundary scan test data and instruction bits. This signal should be connected to +5 volts through a pull-up resistor.
/SCAN_TRSTN	71	In	*Scan Test Reset* is an active low signal used to reset the internal boundary scan test logic. When not using boundary scan, this signal should be connected to ground through a pull-down resistor.
SCAN_TDO	45	Out	*Scan Test Data Output* is the serial output for boundary scan test data.

Table 16. Miscellaneous Signals (Continued)

Signal Name	Pin #	Type	Description
VCC	19, 37, 55, 73, 95, 100, 109, 127	In	Supply voltage 5 ± 0.25 volts.
GND	18, 29, 36, 54, 65, 77, 80, 92, 96, 99, 108, 126, 144	In	Ground.
N/C	10, 11, 72, 78, 81, 91		No connection. All no-connection pins should be connected to ground through a resistor to maintain compatibility with future hardware revisions.
E3 IN	82, 83, 84, 85, 86, 87, 88, 89, 90, 101	In	E3 inputs are input signals used for different applications. All E3 input pins should be connected to ground through a resistor.
E3 OUT	102, 103, 104, 105, 106, 107, 110, 111	Out	E3 outputs are output signals used for different applications. Leave all E3 outputs unconnected.

5. PHYSICAL CHARACTERISTICS

Table 17. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3	6.5	V
I_{OUT}	DC output current, per pin	All outputs except TX_SER_DATA+/-	-12	12	mA
I_{OUT}	DC output current, per pin	TX_SER_DATA+/-	-25	50	mA
T_{STG}	Storage temperature		-65	150	°C

Table 18. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature		-40	85	°C
t_R	Input rise time			10	ns
t_F	Input fall time			10	ns

Table 19. DC Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ITH}	High-level TTL input voltage	All TTL inputs except clocks	2.0			V
V_{ITL}	Low-level TTL input voltage	All TTL inputs except clocks			0.8	V
V_{ISH}	High-level Schmitt-triggered TTL input voltage	All TTL clock inputs			2.4	V
V_{ISL}	Low-level Schmitt-triggered TTL input voltage	All TTL clock inputs	0.6			V
V_{IHys}	Hysteresis Schmitt-triggered TTL input voltage	All TTL clock inputs	0.1			
V_{OCH1}	CMOS high-level output voltage	I_{OL} = -1 mA DC	V_{CC}=0.4			
V_{OCL1}	CMOS low-level output voltage	I_{OL} = 2 mA DC			0.4	
V_{OCH4}	CMOS high-level output voltage	I_{OH} = -8 mA DC TX_SER_DATA+/-	V_{CC}=0.4			V
V_{OCL4}	CMOS low-level output voltage	I_{OL} = 24 mA DC TX_SER_DATA+/-			0.4	V
I_{TYP}	Typical operating current	139.264 MHz, parallel 44.736 MHz, serial		215 180		mA mA

NOTES: • V_{CC}= 5 V ± 5%, T_A = -40° C to 85° C for industrial use.
• Typical values are T_A = 25° C and V_{CC} = 5 V.

Table 20. Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance			10	pF
C_{OUT}	Output capacitance			6	pF

NOTES: • Capacitance measured at 25° C.
• Sample tested only.

6. TIMING DIAGRAMS

All pin names are described in section "4. 3. Pin Descriptions" starting on page 18. Refer to Table A-1 on page 121 for PDH pin name prefix explanations. Unless otherwise indicated, all output timing delays assume a capacitive loading of 30 pF.

6. 1. Transmitter Timing

6. 1. 1. UTOPIA PHY Layer FIFO Input

The transmit UTOPIA PHY layer FIFO timing signals are compatible with the UTOPIA cell-by-cell specification (refer to "Appendix B. References" on page 123). Table 21 indicates the transmit FIFO signal names and their corresponding UTOPIA designations.

Table 21. Transmit Signal Names and Corresponding UTOPIA Designations

Signal Name	UTOPIA Name
TPHY_DATA	TxData
TPHY_SOC	TxSOC
/TPHY_WRITE_EN	TxEnb*
TPHY_CLAV	TxFull*/TxClav
TPHY_CLK	TxClk
TO_FRAME	TxRef*
/TPHY_AEMPTY	Not Available
Not Available	TxPrty

Figure 7 and Figure 8 display the data input format for the internal transmit UTOPIA PHY layer FIFO. The parameter symbols used in Figure 7 and Figure 8 are defined in the table that follows Figure 8. Table 22 defines the contents of the TPHY_DATA bytes. The transmitter accepts data from the TPHY_DATA pins on the rising edge of TPHY_CLK only when /TPHY_WRITE_EN is asserted (low). The transmit ATM FIFO indicates that it has room to accept a full cell by asserting TPHY_CLAV. TPHY_CLAV will be deasserted (low) when the FIFO has accepted the 43rd payload data byte of the third cell. The clock cycles on which data is accepted are marked by an asterisk.

The start-of-cell marker, TPHY_SOC, is asserted when the first byte of the header is written into the FIFO. Under normal circumstances, the TPHY_SOC should be asserted once for every 53 bytes written into the FIFO. If more than 53 bytes are written into the FIFO before the next TPHY_SOC is asserted, the transmitter will ignore all bytes after the 53rd byte until the next TPHY_SOC. If a cell with fewer than 53 bytes (a runt cell) is written into the FIFO before the next TPHY_SOC is asserted, the transmitter will assume that the next TPHY_SOC is the start of a new cell, and discard the runt cell data.

The HEC fill byte is a dummy byte written into the FIFO and replaced by the transmitter with a HEC calculated for the first four header bytes. TPHY_DATA7 is the first bit transmitted in the serial data stream. TPHY_DATA0 is the last bit transmitted in the serial data stream.

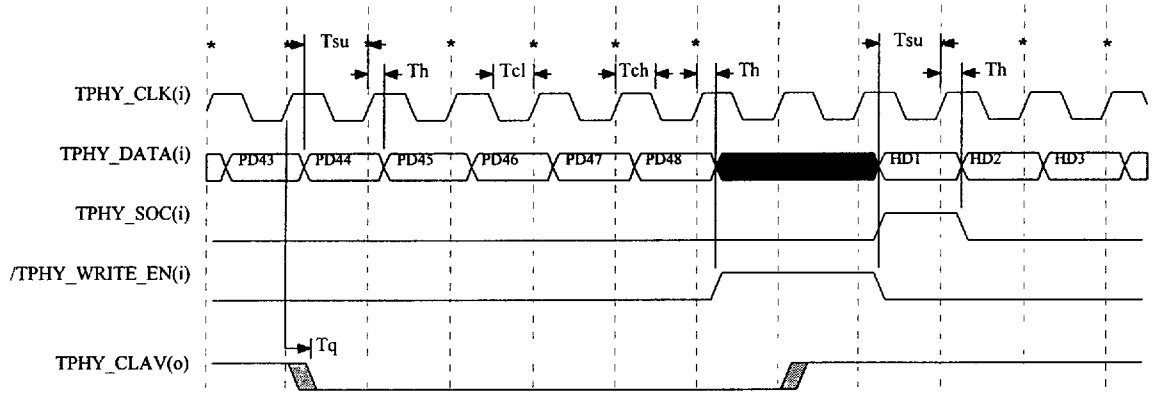

Figure 7. Transmit UTOPIA PHY Layer FIFO Timing

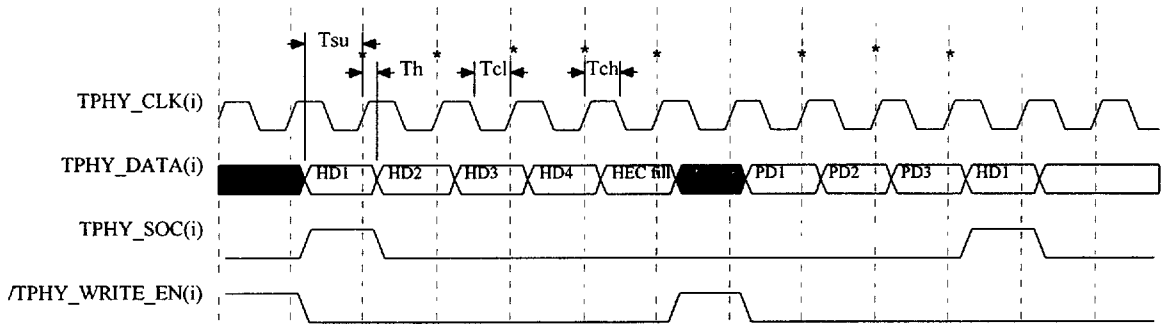

Figure 8. Transmit UTOPIA PHY Layer FIFO Timing with HEC Fill

Symbol	Parameter	Signals	Min	Max	Unit
Fc	TPHY_CLK frequency			25	MHz
Tch	TPHY_CLK high		18		ns
Tcl	TPHY_CLK low		18		ns
Th	TPHY_CLK hold time	TPHY_DATA, /TPHY_WRITE_EN, TPHY_SOC	1		ns
Tsu	TPHY_CLK setup time	TPHY_DATA, /TPHY_WRITE_EN, TPHY_SOC	8		ns
Tq	TPHY_CLK-to-output delay	TPHY_CLAV		19	ns

Table 22. Definitions of TPHY_DATA Byte Contents

Symbol	Definition	Symbol	Definition
HD1	1st header byte	HEC fill	HEC filler byte
HD2	2nd header byte	PD1	1st payload byte
HD3	3rd header byte	PD2	2nd payload byte
HD4	4th header byte	PD48	48th payload byte

6. 1. 2. Transmit Serial Timing

For DS3 operation, the SER_IO_EN signal must be set high. Figure 9 shows the relationship for TX_SER_CLK, TX_SER_DATA, and TX_FRAME. The frame pulse, TX_FRAME, indicates the start of a DS3 frame and occurs once per DS3 frame (once every 4760 clock cycles).

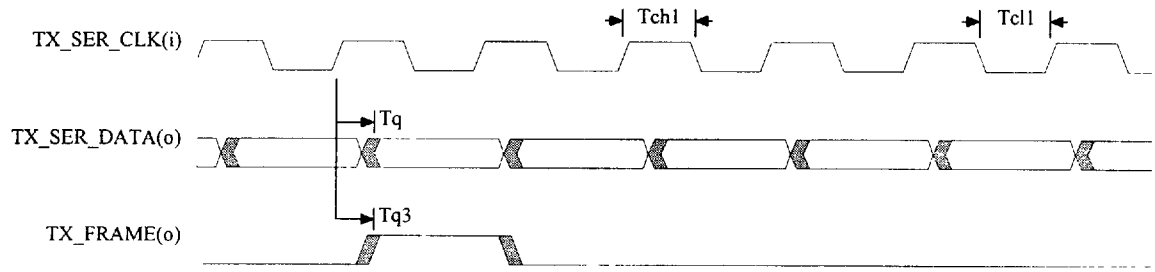

Figure 9. Transmit Serial Timing

Figure 10 reveals that TX_AIS is sampled on the rising edge of TX_SER_CLK. The AIS condition is transmitted while TX_AIS is held high. The example in Figure 10 displays the assertion of TX_AIS for four clock cycles.

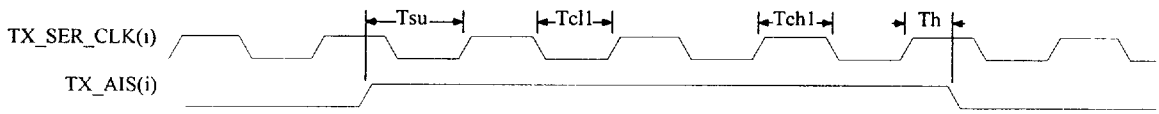

Figure 10. Transmit AIS

Symbol	Parameter	Signals	Min	Max	Unit
Fc	TX_SER_CLK frequency			45	MHz
Tch1	TX_SER_CLK high		9		ns
Tcl1	TX_SER_CLK low		9		ns
Th	TX_SER_CLK hold time	TX_AIS	1		ns
Tsu	TX_SER_CLK setup time	TX_AIS	8		ns
Tq	TX_SER_CLK-to-output delay	TX_SER_DATA+, TX_SER_DATA-		16	ns
Tq3	TX_SER_CLK-to-output delay	TX_FRAME		18	ns

6. 1. 3. Transmit Parallel Timing

The relationship between serial and parallel timing is shown in Figure 11. All parallel inputs and outputs must be associated with the parallel clock output signal, TX_PAR_CLK_OUT.

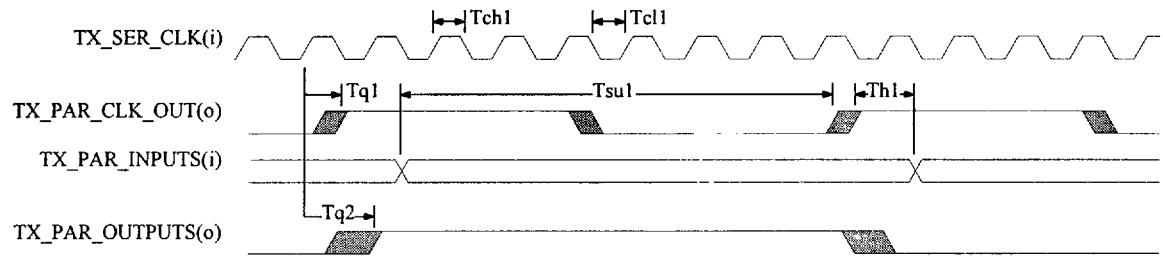

Figure 11. Transmit Parallel Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	TX_SER_CLK frequency			45	MHz
Tch1	TX_SER_CLK high		9		ns
Tcl1	TX_SER_CLK low		9		ns
Th1	TX_PAR_CLK_OUT hold time	TO_RAI, TO_EXT_STUFF, TO_FRAME_IN, TO_INSERT, TO_EXT_IN	0		ns
Tsu1	TX_PAR_CLK_OUT setup time	TO_RAI, TO_EXT_STUFF, TO_FRAME_IN, TO_INSERT, TO_EXT_IN	31		ns
Tq1	TX_SER_CLK-to-output delay	TX_PAR_CLK_OUT		23	ns
Tq2	TX_SER_CLK-to-output delay	TO_FRAME, /TPHY_AEMPTY		30	ns

Figure 12 shows the relationship between TO_FRAME and the insertion data via the TO_EXT_IN and TO_INSERT signals. Bytes in the PLCP data stream are overwritten only when TO_INSERT is asserted. The pulse on TO_INSERT shown in the diagram below, for example, overwrites the HD2 and HD3 bytes following Z6 of the current PLCP with the TO_EXT_IN data (EXT3 and EXT4). The frame pulse, TO_FRAME, occurs once per PLCP frame (once every 688 TX_PAR_CLK_OUT cycles), and can be used to determine when to assert TO_INSERT to overwrite any particular byte of the PLCP data stream. The frame pulse is asserted when the first POH byte (Z6) can be overwritten via the TO_EXT_IN signals.

NOTE: If GFC_EN (A=00h, D5) is a 1, then TO_EXT_IN(7:4) are used to overwrite GFC(3:0) of each cell header, and should not be used to overwrite the PLCP data stream.

The timing parameters for Tsu, Th, and Tq can be derived from the relationships established in Figure 11.

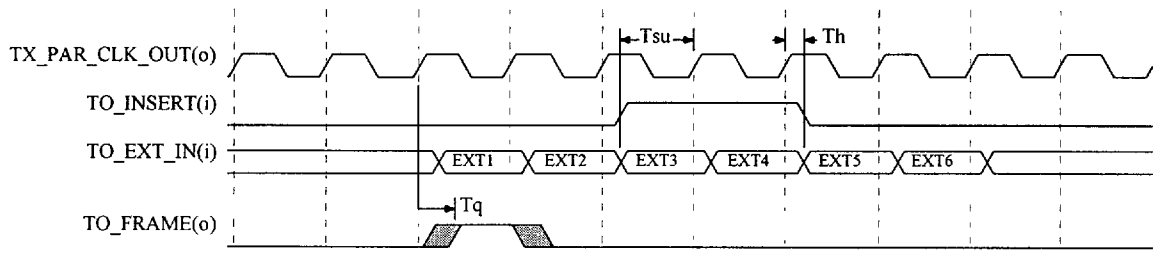

Figure 12. Transmit PLCP Insertion Timing

6. 1. 4. Transmit Data Link Channel Timing

Figure 13 shows the timing associated with inserting data into the data link channel of the DS3 frame. TX_FRAME indicates the beginning of the DS3 frame (occurring once every 4760 clock cycles). The TX_DLINK_CLK is pulsed three times per DS3 frame and should be used to generate the TX_DLINK_DATA.

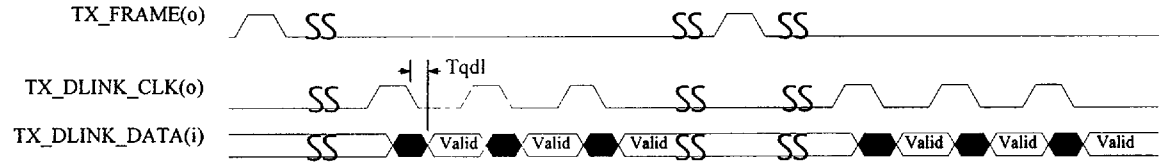

Figure 13. Transmit Data Link Channel Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tqdl	TX_DLINK_CLK-to-output delay	TX_DLINK_DATA		200	ns

6. 2. Receiver Timing

6. 2. 1. UTOPIA PHY Layer FIFO Output

The receive UTOPIA PHY Layer FIFO timing signals are compatible with the UTOPIA cell-by-cell specification (refer to "Appendix B. References" on page 123). Table 23 lists the receive FIFO signal names and their corresponding UTOPIA designations.

Table 23. Receive Signal Names and Corresponding UTOPIA Designations

Signal Name	UTOPIA Name
RPHY_DATA	RxData
RPHY_SOC	RxSOC
/RPHY_READ_EN	RxEnb*
RPHY_CLAV	RxEmpty*/RxClav
RPHY_CLK	RxClk
RO_FRAME	RxRef*
/RPHY_AEMPTY	Not Available
Not Available	RxPrty

Figure 14 shows the output format of the internal receive UTOPIA PHY layer FIFO data. The symbols used in Figure 14 are defined in the table that follows the diagram. Table 24 defines the contents of the RPHY_DATA byte. The receiver presents new data on the rising edge of RPHY_CLK one clock cycle after /RPHY_READ_EN is asserted (low) and the receive FIFO has at least one cell. The deassertion of /RPHY_READ_EN will cause RPHY_DATA and RPHY_SOC to go into tristate. The RPHY_CLAV flag is deasserted (low) one clock cycle after the last data byte is presented at RPHY_DATA. The /RPHY_AEMPTY flag is asserted whenever fewer than 50 bytes are left in the FIFO. The start-of-cell marker, RPHY_SOC, is asserted when the first byte of the header is available on the RPHY_DATA pins. Under normal circumstances, the RPHY_SOC is asserted once for every 53 bytes read from the FIFO. RPHY_DATA7 is the first of the eight bits received in the serial data stream. RPHY_DATA0 is the last of the eight bits received in the serial data stream.

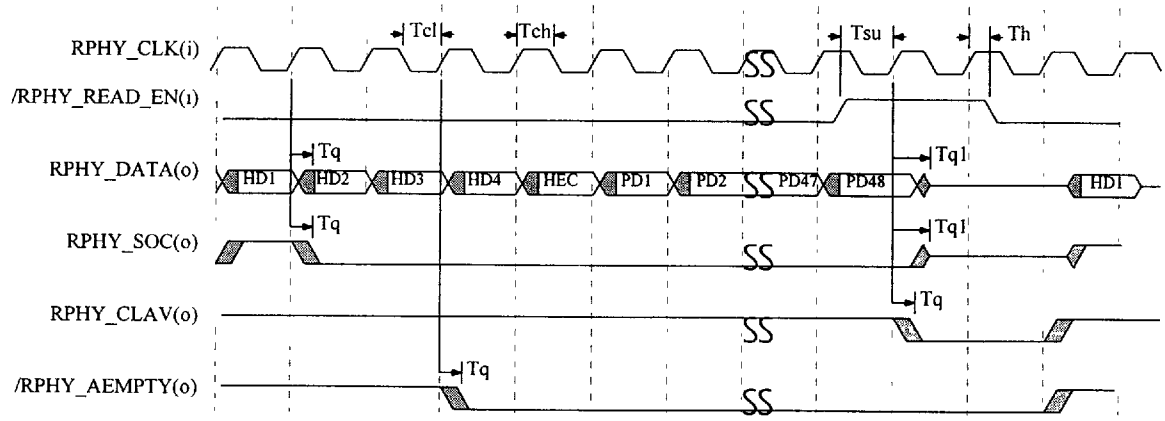

Figure 14. Receive UTOPIA PHY Layer FIFO Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	RPHY_CLK frequency			25	MHz
Tch	RPHY_CLK high		18		ns
Tcl	RPHY_CLK low		18		ns
Th	RPHY_CLK hold time	/RPHY_READ_EN	1		ns
Tsu	RPHY_CLK setup time	/RPHY_READ_EN	8		ns
Tq	RPHY_CLK-to-output delay	RPHY_DATA, RPHY_SOC, /RPHY_AEMPTY, RPHY_CLAV		19	ns
Tq1	RPHY_CLK-to-output enable delay	RPHY_DATA, RPHY_SOC		24	ns

Table 24. Definitions of RPHY_DATA Byte Contents

Symbol	Definition	Symbol	Definition
HD1	1st header byte	HEC	Corrected HEC byte
HD2	2nd header byte	PD1	1st payload byte
HD3	3rd header byte	PD2	2nd payload byte
HD4	4th header byte	PD48	48th payload byte

6. 2. 2. Receive Serial Timing

For DS3 operation, the SER_IO_EN signal must be set high. Figure 15 shows the relationship for RX_SER_CLK, RX_SER_DATA, and RX_FRAME. The frame pulse, RX_FRAME, indicates the start of a DS3 frame and occurs once per DS3 frame (once every 4760 clock cycles).

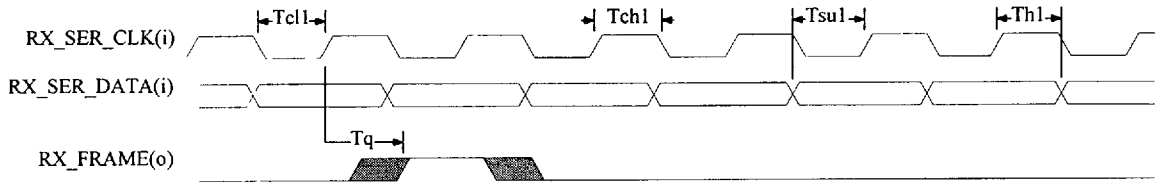

Figure 15. Receive Serial Timing

The timing for the DS3 serial alarms is shown in Figure 16. All alarms are active high and remain high for the duration of the event. The DS3 serial alarms detected by the receiver include RX_AIS, RX_OOF, and RX_LOS. The example in Figure 16 shows the detection of an alarm for four clock cycles.

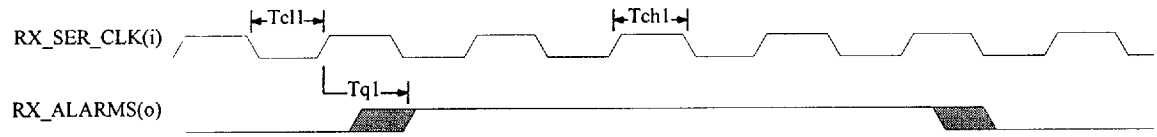

Figure 16. Receive Serial Alarm Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	RX_SER_CLK frequency			45	MHz
Tch1	RX_SER_CLK high		9		ns
Tcl1	RX_SER_CLK low		9		ns
Th1	RX_SER_CLK hold time	RX_SER_DATA	3		ns
Tsu1	RX_SER_CLK setup time	RX_SER_DATA	2		ns
Tq	RX_SER_CLK-to-output delay	RX_FRAME		18	ns
Tq1	RX_SER_CLK-to-output delay	RX_AIS, RX_OOF, RX_LOS		20	ns

6. 2. 3. Receive Parallel Timing

The relationship between serial and parallel timing is shown in Figure 17. All parallel outputs must be associated with the parallel clock output signal, RX_PAR_CLK_OUT.

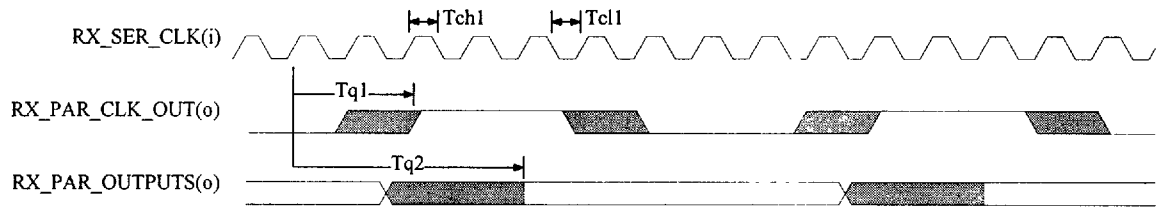

Figure 17. Receive Parallel Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	RX_SER_CLK frequency			45	MHz
Tch1	RX_SER_CLK high		9		ns
Tcl1	RX_SER_CLK low		9		ns
Tq1	RX_SER_CLK-to-output delay	RX_PAR_CLK_OUT		23	ns
Tq2	RX_SER_CLK-to-output delay	RM_OCD, RO_RAI, RO_OOF, RO_LOF, RO_FRAME, RO_EN, RO_TR_EN, RO_EXT_OUT		33	ns

Figure 18 and Figure 19 reveal the relationship for RO_EXT_OUT, RO_FRAME, RO_EN, and RO_TR_EN. These signals can be used to determine the location of the overhead bytes and ATM cells in the PLCP frame. (Refer to Figure 4 on page 8 for details on the DS3 PLCP framing structure.) RO_FRAME is asserted for one clock cycle when valid frame words (A1 and A2) are detected. Typically, the RO_FRAME pulse occurs 12 times per PLCP frame and when RO_EXT_OUT contains the HD1 byte of the ATM cell. RO_EN is an active high signal indicating that an overhead byte is present on RO_EXT_OUT. RO_TR_EN is an active high signal indicating that the trailer nibbles are present on RO_EXT_OUT. Note that in Figure 19, RX_PAR_CLK_OUT is gapped during the reception of the Trailer nibbles. When the trailer length is 13 nibbles, RX_PAR_CLK_OUT is gapped for a period of six nibbles, and when the trailer length is 14 nibbles, RX_PAR_CLK_OUT is gapped for a period of seven nibbles.

NOTE: If GFC_EN (A=00h, D5) is a 1, then RO_EXT_OUT(7:4) are used to present the received GFC(3:0) of each cell header, and should not be used to extract the PLCP data stream.

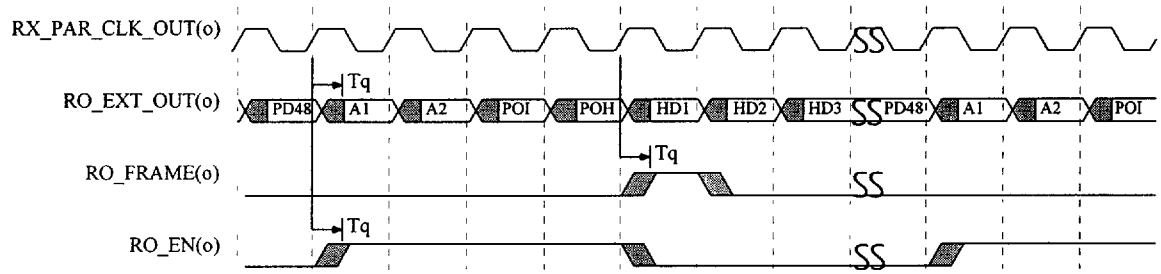

Figure 18. Receive External Timing

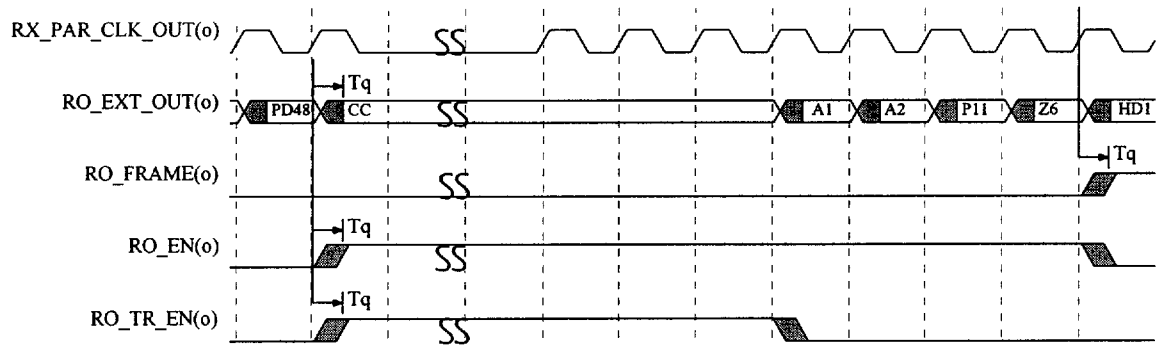

Figure 19. Receive External Timing with RO_TR_EN

6. 2. 4. Receive Data Link Channel Timing

Figure 20 shows the timing associated with accessing data from the data link channel of the DS3 frame. RX_FRAME indicates the beginning of the DS3 frame (occurring once every 4760 clock cycles). The RX_DLINK_CLK is pulsed three times per DS3 frame and is used to indicate that RX_DLINK_DATA is valid. Note that in Figure 20, RX_DLINK_DATA is valid prior to the rising edge of RX_DLINK_CLK and after the falling edge of RX_DLINK_CLK.

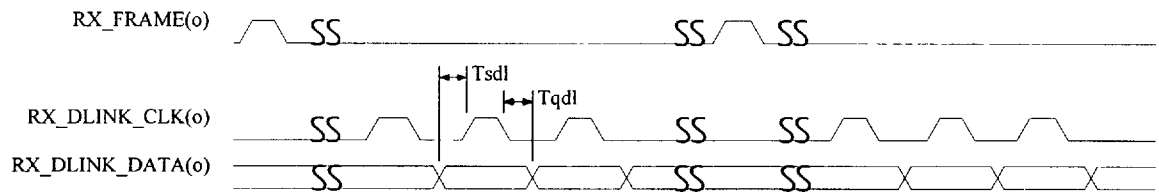

Figure 20. Receive Data Link Channel Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tsdl	RX_DLINK_CLK setup time	RX_DLINK_DATA	1700		ns
Tqdl	RX_DLINK_CLK-to-output delay	RX_DLINK_DATA	1600	1800	ns

6. 3. Microprocessor Timing

Figure 21 displays the timing for typical microprocessor read/write cycles without the use of ADDR_LAT_EN. In the example below, the read cycle precedes the write cycle. The setup, hold, and delay times are given with respect to several signals (/CS, /RD, and /WR). Parameter times are determined by the relationships of the various signals as shown in the table below; for example, the Tdsu parameter definition is "data setup time prior to /CS or /WR, whichever comes first". This definition indicates that the data, D, must be valid *Tdsu* nanoseconds before /CS or /WR, whichever comes first. In the write cycle example below, since /WR is deasserted before /CS, the data must be valid *Tdsu* nanoseconds before the /WR signal, and has no minimum setup time with respect to the /CS signal.

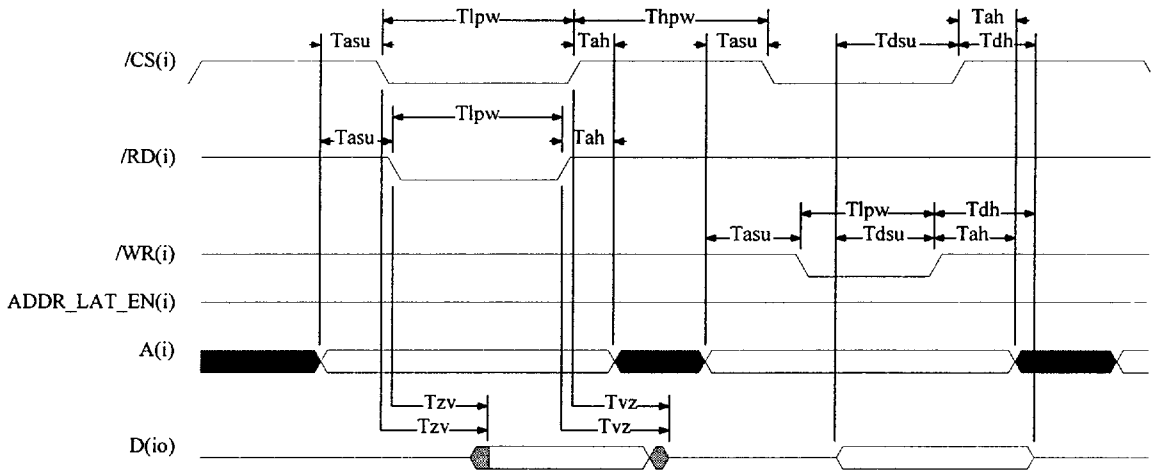

Figure 21. Microprocessor Read and Write Cycle Timing

Figure 22 displays the timing for typical microprocessor read/write cycles with the use of ADDR_LAT_EN. In the example below, the read cycle precedes the write cycle.

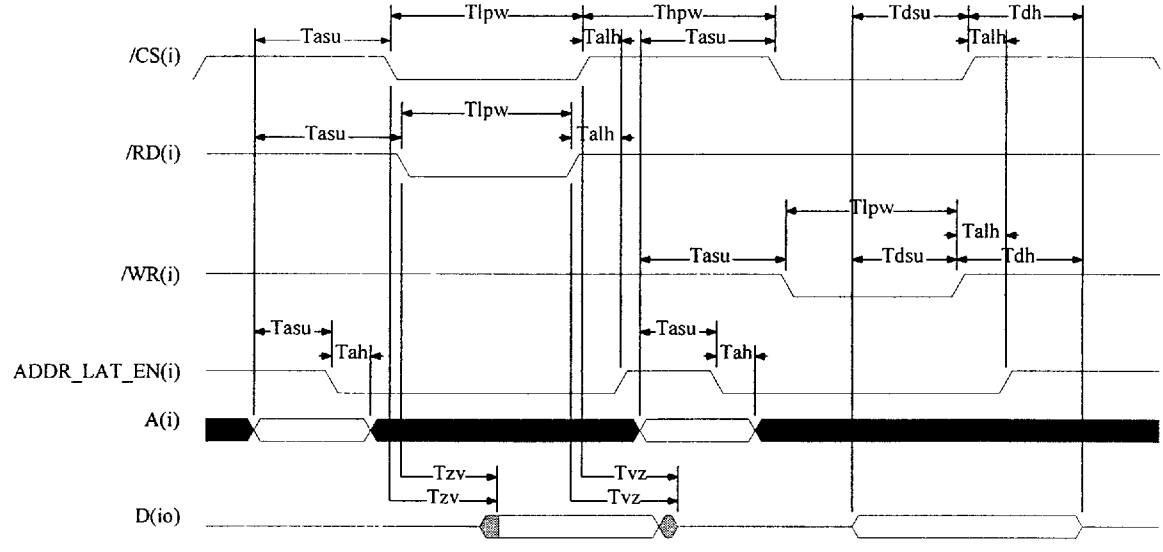

Figure 22. Microprocessor Read and Write Cycle Timing with ADDR_LAT_EN

Symbol	Parameter	Signals	Min	Max	Unit
Tasu	address setup time prior to /CS, /RD, /WR, or ADDR_LAT_EN, whichever comes last	A	12		ns
Tah	address hold time prior to /CS, /RD, /WR, or ADDR_LAT_EN, whichever comes first	A	2		ns
Talh	address latch hold time prior to /CS, /RD, /WR, whichever comes first	ADDR_LAT_EN	0		ns
Tdsu	data setup time prior to /CS or /WR, whichever comes first	D	12		ns
Tdh	data hold time prior to /CS or /WR, whichever comes first	D	0		ns
Tzv	data valid after /CS or /RD, whichever comes last	D		28	ns
Tvz	data tristate after /CS or /RD, whichever comes first	D	2	23	ns
Tlpw	low pulse width	/CS, /RD, /WR	11		
Thpw	high pulse width	/CS, /RD, /WR	23		

Figure 23 displays the interrupt timing constraints. The interrupt is asserted asynchronously with respect to the /RD and /CS signals when a non-masked interrupt occurs. The interrupt is cleared when the interrupt register ($2D_h$ or $2E_h$) containing the active interrupt is read, assuming that no additional interrupts are generated during the read cycle. If interrupts have occurred in both $2D_h$ and $2E_h$, both registers must be read to clear the interrupt line.

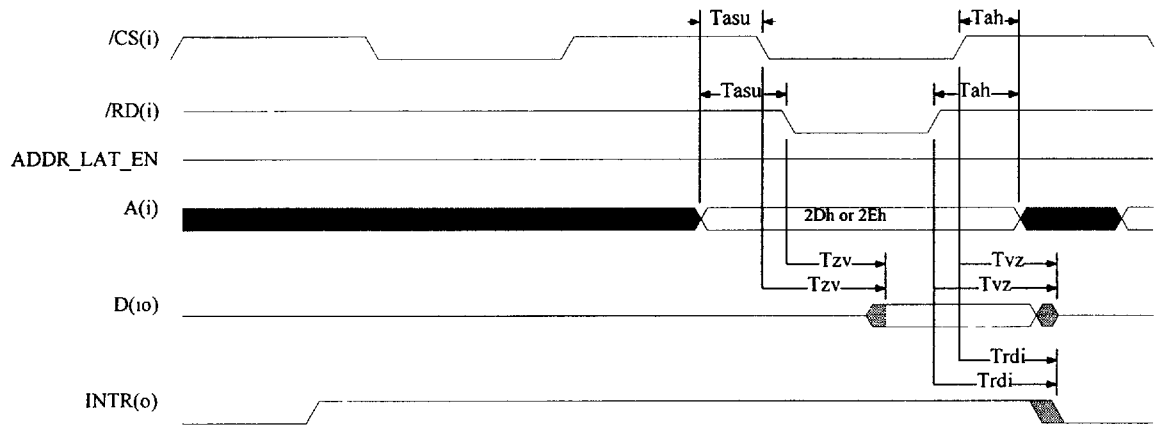

Figure 23. Interrupt Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tasu	address setup to /CS, /RD, or /WR, whichever comes last	A	12		ns
Tah	address hold to /CS, /RD, or /WR, whichever comes first	A	2		ns
Trdi	interrupt cleared after /CS or /RD, whichever comes first	INTR		23	ns
Tzv	data valid after /CS or /RD, whichever comes last	D		28	ns
Tvz	data tristate after /CS or /RD, whichever comes first	D	2	23	ns

6. 4. Miscellaneous Timing

Figure 24 displays the reset pin timing. The /RESET signal must be asserted for a minimum time (Tres) to be registered properly. The WAC-034-B remains in reset while /RESET is asserted and starts performing normally within three to seven transmit parallel/receive parallel clock cycles after the reset is removed.

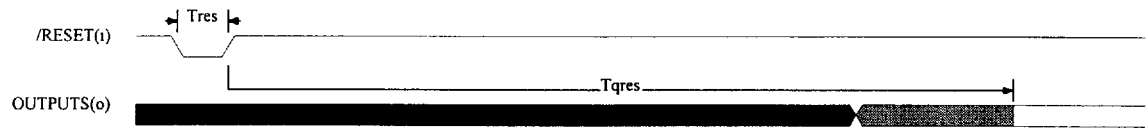

Figure 24. Reset Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tres	minimum reset pulse	/RESET	20		ns
Tqres	reset deasserted to normal operation	all outputs	3	7	clock cycles

All outputs of the chip are tristated when OUTPUT_EN is deasserted. The output enable timing is displayed in Figure 25.

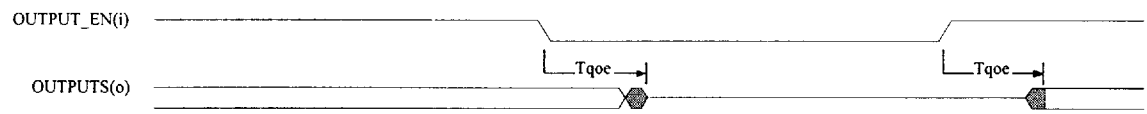

Figure 25. Output Enable Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tqoe	output enable	all outputs		28	ns

The timing for the JTAG port is shown in the Figure 26. The /SCAN_TRSTN signal is asynchronous to SCAN_TCK.

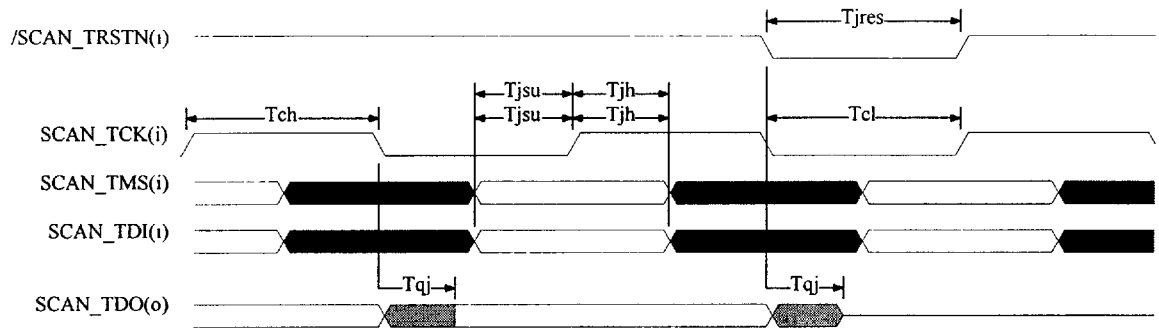

Figure 26. JTAG Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	SCAN_TCK frequency			5	MHz
Tch	SCAN_TCK high		80		ns
Tcl	SCAN_TCK low		80		ns
Tjh	SCAN_TCK hold time	SCAN_TMS, SCAN_TDI	40		ns
Tjres	/SCAN_TRSTN low		80		ns
Tjsu	SCAN_TCK setup time	SCAN_TMS, SCAN_TDI	40		ns
Tqj	SCAN_TCK-to-output delay /SCAN_TRSTN-to-output delay	SCAN_TDO	2	40	ns

7. BOUNDARY SCAN

Table 25 lists the boundary scan instructions and instruction codes supported by the WAC-034-B. Bit 3 is the most significant bit and should be the first bit shifted into SCAN_TMS. Bit 0 is the least significant bit and should be the last bit shifted into SCAN_TMS..

Table 25. Boundary Scan Instruction Codes

Instruction Name	Instruction Code, IR(3:0)
EXTEST	0000
INTEST (not supported)	0001
SAMPLE	0010
SAMPLE	0011
BYPASS	0100
BYPASS	0101
BYPASS	0110
BYPASS	0111
BYPASS	1000
BYPASS	1001
BYPASS	1010
BYPASS	1011
BYPASS	1100
BYPASS	1101
BYPASS	1110
BYPASS	1111

Table 26 shows the boundary scan registers and the order in which they will be shifted out on SCAN_TDO.

Table 26. Boundary Scan Registers

Pin/Enable Name	Bit #	Type
/CS	117	in
/RD	116	in
/WR	115	in
A(0:5)	114:109	in
D0	108	in
D0	107	out
D1	106	in
D1	105	out
D2	104	in
D2	103	out
D3	102	in
D3	101	out
D4	100	in
D4	99	out
D5	98	in
D5	97	out
D6	96	in
D6	95	out
D7	94	in
D7	93	out
/D_OE	92	internal
INTR	91	out
/RESET	90	in
/SCAN_OUTPUT_EN	89	internal
OUTPUT_EN	88	in
RPHY_DATA(0:7)	87:80	out
/RPHY_READ_EN	79	in
RPHY_CLK	78	in
RPHY_SOC	77	out
RPHY_CLAV	76	out
/RPHY_AEMPTY	75	out
RO_TR_EN	74	out
RO_EXT_OUT(0:7)	73:66	out
/RO_EXT_OUT_OE	65	internal
RM_OCD	64	out
RX_DLINK_DATA	63	out

Pin/Enable Name	Bit #	Type
/TPHY_AEMPTY	62	out
RX_DLINK_CLK	61	out
RX_OOF	60	out
RO_EN	59	out
RX_FRAME	58	out
RO_RAI	57	out
RX_AIS	56	out
RX_LOS	55	out
RO_OOF	54	out
RO_LOF	53	out
RO_FRAME	52	out
RX_PAR_CLK_OUT	51	out
SER_IO_EN	50	in
E3 IN	49:42	in
E3 IN	41	in
TX_AIS	40	in
E3 IN	39	in
E3 OUT	38:31	out
TX_PAR_CLK_OUT	30	out
TO_FRAME	29	out
TO_FRAME_IN	28	in
TO_INSERT	27	in
TO_EXT_IN(0:7)	26:19	in
/TO_EXT_IN_OE	18	internal
TX_DLINK_DATA	17	in
TX_DLINK_CLK	16	out
TO_RAI	15	in
ADDR_LAT_EN	14	in
TX_FRAME	13	out
/TPHY_WRITE_EN	12	in
TPHY_SOC	11	in
TPHY_CLK	10	in
TPHY_DATA(0:7)	9:2	in
TO_EXT_STUFF	1	in
TPHY_CLAV	0	out

The output enable controls are as follows: Under normal operation, all outputs are tristated by the OUTPUT_EN pin being set to 0. For the INTEST and EXTEST operations, there are four separate active low output enables: /D_OE enables D(7:0), /RO_EXT_OUT_OE enables RO_EXT_OUT(7:0), /TO_EXT_IN_OE enables TO_EXT_IN(7:0), and /SCAN_OUTPUT_EN enables the rest of the outputs.

NOTE: /TO_EXT_IN_OE is used for production testing and should always be deasserted (set to a 1) during scan testing.

8. MICROPROCESSOR PORTS

8. 1. Write Ports Summary

NOTE: The external /RESET signal, when asserted, sets all microprocessor write ports to a default state. The default state is 0 unless otherwise shown.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
GEN_W1	00_h	0	0	GFC_EN	0	BIPOLAR_ DIS	RATE(1:0)		LOC_ LOOP_ON
TX_W1	01_h	0	0	0	0	0	0	0	TX_RESET
TX_W2	02_h	0	0	0	0	0	0	TX_BPV_ INS_ONCE	TX_LOS_ INS
TX_CNTR_W1	03_h	0	0	0	0	0	0	0	TX_CNTR_ LATCH
TM_W1	04_h	0	0	0	TM_HEC_ DIS	TM_ SCRAM_DIS [Default = 1]	TM_COSET_ DIS	TM_HEC_ INV_CONT	TM_HEC_ INV_ONCE
TM_W2	05_h	TM_HEC_INV_MASK(7:0)							
TM_W3	06_h	TM_NULL_HDI(7:0)							
TM_W4	07_h	TM_NULL_HD2(7:0)							
TM_W5	08_h	TM_NULL_HD3(7:0)							
TM_W6	09_h	TM_NULL_HD4(7:0)							
TM_W7	$0A_h$	TM_NULL_PAYLOAD(7:4) GFC_MASK(3:0)				TM_NULL_PAYLOAD(3:0)			
TO_W1	$0B_h$	0	0	0	0	TO_STUFF_ LOOP	TO_PLCP_ DIS	0	0
TO_W2	$0C_h$	0	TO_RAI_ INS	TO_POI_ INV_CONT	TO_POI_ INV_ONCE	TO_A2_ FERR_INS	TO_A1_ FERR_INS	TO_B1_ INV_CONT	TO_B1_ INV_ONCE
TX_DS3_W1	$1E_h$	0	0	0	TX_DS3_ AUTO_FEBE_ DIS	TX_DS3_M13	TX_DS3_AIS	TX_DS3_ IDLE	TX_DS3_ XBIT
TX_DS3_W2	$1F_h$	FEAC_EN	0	TX_DS3_FEAC(5:0)					
TX_DS3_W3	20_h	0	0	0	0	TX_DS3_ FEBE_IN	TX_DS3_ CPERR_INS	TX_DS3_ PERR_INS	TX_DS3_ FERR_INS
RX_W1	24_h	0	0	0	0	0	0	0	RX_RESET
RX_W2	25_h	0	0	0	0	0	0	0	RX_EXZ_ DIS
RX_CNTR_W1	26_h	0	0	0	RX_CNTR_LATCH_SEL(3:0)				RX_CNTR_ LATCH
RM_W1	27_h	0	RM_HEC_ CORRECT_ DIS [Default = 1]	0	RM_PASS_ OCD	RM_PASS_ UNASSIGNED	RM_PASS_ BAD_HEC	RM_ DESCRAM_ DIS [Default = 1]	RM_ COSET_DIS
RO_W1	28_h	0	0	0	0	RO_BLOCK_ CNT_EN	RO_PLCP_ DIS	0	RO_OOF_ INS
RX_DS3_W1	29_h	0	0	0	0	0	0	RX_DS3_ MLOS_2_3	RX_DS3_ FLOS_6_15
INTR_MASK_W1	$2A_h$	RO_LOF_ MASK	RO_OOF_ MASK	RM_OCD_ MASK	RM_FIFO_ OVERFLOW_ MASK	0	RO_RAI_ MASK	0	0
INTR_MASK_W2	$2B_h$	RX_DS3_ CPAR_ MASK	RX_DS3_ OOF_MASK	RX_DS3_ AIS_1010_ MASK	RX_DS3_ AIS_STUCKC_ MASK	RX_DS3_ YELLOW_ ALM_MASK	RX_DS3_ IDLE_MASK	RX_DS3_ FEAC_ MASK	RX_LOS_ MASK
TEST_W1	$2E_h$	TEST(7:0)							
TEST_W2	$2F_h$	TEST(15:8)							

8. 2. Read Ports Summary

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_CNTR_R1	03_h								TX_CNTR_ LATCH
RX_CNTR_R1	26_h								RX_CNTR_ LATCH
TX_CNTR_R2	27_h	TX_LATCHED_COUNT(7:0)							
TX_CNTR_R3	28_h	TX_LATCHED_COUNT(15:8)							
RX_CNTR_R2	29_h	RX_LATCHED_COUNT(7:0)							
RX_CNTR_R3	$2A_h$	RX_LATCHED_COUNT(15:8)							
RX_DS3_R1	$2B_h$			RX_DS3_FEAC(5:0)					
RX_DS3_R2	$2C_h$							RX_DS3_ X2_BIT	RX_DS3_ X1_BIT
INTR_R1	$2D_h$	RO_LOF_ INTR	RO_OOF_ INTR	RM_OCD_ INTR	RM_FIFO_ OVERFLOW_ INTR		RO_RAI_ INTR		
INTR_R2	$2E_h$	RX_DS3_ CPAR_ INTR	RX_DS3_ OOF_INTR	RX_DS3_ AIS_1010_ INTR	RX_DS3_ AIS_STUCKC_ INTR	RX_DS3_ YELLOW_ ALRM_INTR	RX_DS3_ IDLE_INTR	RX_DS3_ FEAC_ INTR	RX_LOS_ INTR
STATUS_R1	$2F_h$	RO_LOF	RO_OOF	RM_OCD	RM_FIFO_ OVERFLOW		RO_RAI		
STATUS_R2	30_h	RX_DS3_ CPAR	RX_DS3_ OOF	RX_DS3_ AIS_1010	RX_DS3_ AIS_STUCKC	RX_DS3_ YELLOW_ ALRM	RX_DS3_ IDLE		RX_LOS
HW_REV_R1	$3F_h$	0	0	0	0	0	0	0	0

8. 3. Write Ports

NOTES:

- The external /RESET signal, when asserted, sets all microprocessor write ports to a default state. The default state is 0 unless otherwise shown.
- All port bits marked "0" must be written with the value 0 to maintain software compatibility with future versions.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
GEN_W1	00_h	0	0	GFC_EN	0	BIPOLAR_ DIS	RATE(1:0)		LOC_ LOOP_ON

D(7:6) Write with a 0 to maintain compatibility with future software versions.
D5 GFC_EN
1 - Enables the insertion of GFC bits in the transmit data stream via TO_EXT_IN(7:4), and the reporting of GFC bits from the receive data stream via RO_EXT_OUT(7:4).
0 - Disables the insertion of GFC bits in the transmit data stream via TO_EXT_IN(7:4), and the reporting of GFC bits from the receive data stream via RO_EXT_OUT(7:4).

NOTE: GFC bits are only inserted if the corresponding GFC_MASK (Addr=$0A_h$, D[7:4]) bit is a 1.

D4 Write with a 0 to maintain compatibility with future software versions.
D3 BIPOLAR_DIS
1 - Transmission and reception at the serial input and output is dependent upon the positive signal only (TX_SER_DATA+ and RX_SER_DATA+).
0 - Enables bipolar transmission and reception at the serial input and output.
D(2:1) RATE
00 - Sets the framing format to DS3.
01 - Sets the framing format to E3.
10 - Sets the framing format to E4.
11 - Not used.
D0 LOC_LOOP_ON
1 - Enables the Local Loop (the transmit data and the transmit clock are fed back to the receiver).
0 - Disables the Local Loop.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_W1	01_h	0	0	0	0	0	0	0	TX_ RESET

D(7:1) Write with a 0 to maintain compatibility with future software versions.
D0 TX_RESET

NOTE: The transmitter enters the reset state when a 1 is written to this location, and remains in the reset state until a 0 is written to this location.

1 - Resets the transmitter.
0 - Allows the transmitter to resume normal operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_W2	02_h	0	0	0	0	0	0	TX_BPV_ INS_ONCE	TX_LOS_ INS

D(7:2) Write with a 0 to maintain compatibility with future software versions.

D1 TX_BPV_INS_ONCE

A rising edge on this bit will force the B3ZS encoder to insert one BPV without causing a false B3ZS sequence. After TX_BPV_INS_ONCE has been latched, additional pulsing of TX_BPV_INS_ONCE will be ignored until the BPV is inserted. To produce a rising edge, write a 0 followed by a 1 to this port bit location.

D0 TX_LOS_INS

1 - Forces TX_SER_DATA+/- to 0.

0 - Allows normal transmission.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_CNTR_W1	03_h	0	0	0	0	0	0	0	TX_CNTR_ LATCH

D(7:1) Write with a 0 to maintain compatibility with future software versions.

D0 TX_CNTR_LATCH

NOTE: The latch operation can be verified by ensuring that the TX_CNTR_LATCH bit in the TX_CNTR_R1 register is a 0.

1 - Initiates the latch operation for the transmit message cell counter.

0 - Normal operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TM_W1	04_h	0	0	0	TM_ HEC_DIS	TM_ SCRAM_ DIS [Default = 1]	TM_ COSET_DIS	TM_HEC_ INV_CONT	TM_HEC_ INV_ONCE

D(7:5) Write with a 0 to maintain compatibility with future software versions.

D4 TM_HEC_DIS

1 - Disables HEC insertion.

NOTE: For null cells the TM_NULL_PAYLOAD pattern is transmitted in the HEC location.

0 - Enables calculation and insertion of HEC in the fifth header byte.

D3 TM_SCRAM_DIS

1 - Disables the cell payload scrambling.

0 - Enables the cell payload scrambling.

D2 TM_COSET_DIS

1 - Disables the addition of the coset (55_h) to the HEC.

0 - Enables the addition of the coset (55_h) to the HEC.

D1 TM_HEC_INV_CONT

1 - Enables inversion of the HEC bits in accordance with the TM_HEC_INV_MASK bits.

0 - Disables inversion of the HEC bits.

D0 TM_HEC_INV_ONCE

A rising edge on this bit inverts the next HEC in accordance with the TM_HEC_INV_MASK bits. This control bit does not affect transmission if TM_HEC_INV_CONT is asserted. To produce a rising edge, write a 0 followed by a 1 to this port bit location

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TM_W2	05_h	TM_HEC_INV_MASK(7:0)							

D(7:0) TM_HEC_INV_MASK

A 1 in a bit location indicates that the associated HEC bit is to be inverted when TM_HEC_INV_CONT is asserted, or when a rising edge is detected on TM_HEC_INV_ONCE.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TM_W3	06_h	TM_NULL_HD1(7:0)							
TM_W4	07_h	TM_NULL_HD2(7:0)							
TM_W5	08_h	TM_NULL_HD3(7:0)							
TM_W6	09_h	TM_NULL_HD4(7:0)							
TM_W7	$0A_h$	TM_NULL_PAYLOAD(7:4) GFC_MASK(3:0)				TM_NULL_PAYLOAD(3:0)			

ADDR=06_h

D(7:0) TM_NULL_HD1

This is the first header byte of the null cell. D7 is the first bit to be transmitted in the serial data stream.

ADDR=07_h

D(7:0) TM_NULL_HD2

This is the second header byte of the null cell. D7 is the first bit to be transmitted in the serial data stream.

ADDR=08_h

D(7:0) TM_NULL_HD3

This is the third header byte of the null cell. D7 is the first bit to be transmitted in the serial data stream.

ADDR=09_h

D(7:0) TM_NULL_HD4

This is the fourth header byte of the null cell. D7 is the first bit to be transmitted in the serial data stream.

ADDR=$0A_h$

D(7:0) TM_NULL_PAYLOAD/GFC_MASK

This is the pattern that is transmitted in the entire 48-byte payload of the null cell. This pattern is also transmitted as the HEC byte of the null cell when TM_HEC_DIS is asserted. D7 is the first bit to be transmitted in the serial data stream.

When GFC_EN (Addr=00_h, D5) is a 1, the upper nibble of this register is also used to determine which of the TO_EXT_IN pins will overwrite the GFC bits of outgoing cells. If D7 is a 1, then TO_EXT_IN7 will overwrite GFC3. If D6 is a 1, then TO_EXT_IN6 will overwrite GFC2. If D5 is a 1, then TO_EXT_IN5 will overwrite GFC1. If D4 is a 1, then TO_EXT_IN4 will overwrite GFC0.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TO_W1	$0B_h$	0	0	0	0	TO_STUFF_ LOOP	TO_PLCP_ DIS	0	0

D(7:4) Write with a 0 to maintain compatibility with future software versions.

D3 TO_STUFF_LOOP
- 1 - Allows nibble stuffing of the PLCP to be controlled by the received PLCP stuffing sequence.
- 0 - Allows nibble stuffing of the PLCP to be controlled by the external signal TO_EXT_STUFF.

D2 TO_PLCP_DIS
- 1 - Disables PLCP overhead processing.
- 0 - Enables PLCP overhead processing.

D(1:0) Write with a 0 to maintain compatibility with future software versions.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TO_W2	$0C_h$	0	TO_RAI_ INS	TO_POI_ INV_CONT	TO_POI_ INV_ONCE	TO_A2_ FERR_INS	TO_A1_ FERR_INS	TO_B1_ INV_CONT	TO_B1_ INV_ONCE

D7 Write with a 0 to maintain compatibility with future software versions.

D6 TO_RAI_INS
- 1 - Sets the RAI bit of the G1 byte for transmission.
- 0 - Resets the RAI bit of the G1 byte for transmission.

D5 TO_POI_INV_CONT
- 1 - Inverts the parity bit of the POI value before transmission.
- 0 - Transmits the normal POI value.

D4 TO_POI_INV_ONCE

A rising edge on this bit inverts the parity bit of the next POI value to be transmitted. This control bit does not affect transmission if TO_POI_INV_CONT is asserted.

D3 TO_A2_FERR_INS
- 1 - Inverts the first bit of the A2 byte before transmission.
- 0 - Transmits the normal A2 byte.

D2 TO_A1_FERR_INS
- 1 - Inverts the first bit of the A1 byte before transmission.
- 0 - Transmits the normal A1 byte.

D1 TO_B1_INV_CONT
- 1 - Inverts the B1 value before transmission.
- 0 - Transmits the normal B1 value.

D0 TO_B1_INV_ONCE

A rising edge on this bit inverts the next B1 value to be transmitted. This control bit does not affect transmission if TO_B1_INV_CONT is asserted.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_DS3_W1	$1E_h$	0	0	0	TX_DS3_ AUTO_ FEBE_DIS	TX_DS3_ M13	TX_DS3_ AIS	TX_DS3_ IDLE	TX_DS3_ XBIT

D(7:5) Write with a 0 to maintain compatibility with future software versions.

D4 TX_DS3_AUTO_FEBE_DIS

1 - Disables automatic generation of FEBEs for the DS3 Transmitter.

0 - Automatically generates FEBEs when F-bit, M-bit, or CP-bit errors are received.

D3 TX_DS3_M13

1 - Selects M13 framing format for the DS3 Transmitter.

0 - Selects C-bit parity framing format for the DS3 Transmitter.

D2 TX_DS3_AIS

1 - Enables AIS transmission.

0 - Disables AIS transmission.

When transmitting AIS, the WAC-034-B will continue reading from the transmit ATM FIFO, thus causing the ATM FIFO data to be lost. However, the transmit message counter will not increment.

D1 TX_DS3_IDLE

1 - Enables Idle Signal transmission.

0 - Disables Idle Signal transmission.

When transmitting AIS, the WAC-034-B will continue reading from the transmit ATM FIFO, thus causing the ATM FIFO data to be lost. However, the transmit message counter will not increment.

D0 TX_DS3_XBIT

1 - Sets both X-bits to 1.

0 - Sets both X-bits to 0 (Yellow Alarm).

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_DS3_W2	$1F_h$	FEAC_EN	0	TX_DS3_FEAC(5:0)					

D7 FEAC_EN

1 - Enables FEAC generation and detection.

0 - Disables FEAC generation and transmits all 1s for the FEAC channel. This bit also disables FEAC detection.

D6 Write with a 0 to maintain compatibility with future software versions.

D(5:0) TX_DS3_FEAC(5:0)

These are the six programmable bits within the repeating, 16-bit FEAC code word. The FEAC code is defined as 11111111 0XXXXXX0, in which X can be a 0 or a 1. D5 is the first bit to be transmitted in the serial data stream.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_DS3_W3	20_h	0	0	0	0	TX_DS3_ FEBE_INS	TX_DS3_ CPERR_ INS	TX_DS3_ PERR_ INS	TX_DS3_ FERR_ INS

D(7:4) Write with a 0 to maintain compatibility with future software versions.

D3 TX_DS3_FEBE_INS

A rising edge on this bit forces all three FEBE-bits to 0 for one frame to generate one FEBE event.

D2 TX_DS3_CPERR_INS

A rising edge on this bit inverts all three CP-bits for one frame to generate one C-bit parity error.

D1 TX_DS3_PERR_INS

A rising edge on this bit inverts the two P-bits for one frame to generate one parity error.

D0 TX_DS3_FERR_INS

A rising edge on this bit inverts the first F-bit in the first subframe for one frame to generate one framing bit error.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_W1	24_h	0	0	0	0	0	0	0	RX_ RESET

D(7:1) Write with a 0 to maintain compatibility with future software versions.

D0 RX_RESET

NOTE: The receiver enters the reset state when a 1 is written to this location, and remains in the reset state until a 0 is written to this location.

1 - Resets the receiver.
0 - Allows receiver to resume normal operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_W2	25_h	0	0	0	0	0	0	0	RX_EXZ_ DIS

D(7:1) Write with a 0 to maintain compatibility with future software versions.

D0 RX_EXZ_DIS

1 - Configures the B3ZS decoder to ignore the occurrence of three or more consecutive 0s.
0 - Configures the B3ZS decoder to count three or more consecutive 0s as a line code violation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_CNTR_W1	26_h	0	0	0	RX_CNTR_LATCH_SEL(4:0)				RX_CNTR_LATCH

D(7:5) Write with a 0 to maintain compatibility with future software versions.

D(4:1) RX_CNTR_LATCH_SEL

Selects the counter to be latched.

0000 - Message received counter. Counts complete cells written to the receive ATM FIFO. This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_DS3_AIS_1010, RX_DS3_AIS_STUCKC, RX_DS3_IDLE, RM_OCD.

0001 - Incorrect HEC counter. Counts headers with uncorrectable HECs when the ATM cell header processing is in Correction Mode. Also counts all headers with incorrect HECs when the ATM cell header processing is in Detection Mode. The chip automatically selects Correction or Detection Mode in accordance with the ATM Forum's UNI specification (refer to "Appendix B. References" on page 123). This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_DS3_AIS_1010, RX_DS3_AIS_STUCKC, RX_DS3_IDLE, RM_OCD.

0010 - BIP-8 (B1) error counter. Counts all BIP errors per byte as a single error when RO_BLOCK_CNT_EN is set to 1, and individually counts each BIP error per byte when RO_BLOCK_CNT_EN is set to 0. This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_DS3_AIS_1010, RX_DS3_AIS_STUCKC, RX_DS3_IDLE.

0011 - PLCP FEBE counter. Individually counts each PLCP FEBE per byte. This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_DS3_AIS_1010, RX_DS3_AIS_STUCKC, RX_DS3_IDLE.

0100 - PLCP FERR counter. Counts one frame error per PLCP row when any of the A1, A2, or POI bytes are in error for that row. This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_DS3_AIS_1010, RX_DS3_AIS_STUCKC, RX_DS3_IDLE.

0101 - DS3 FERR counter. Counts all F-bit and M-bit errors. This counter is disabled by the following alarm: RX_LOS, RX_DS3_OOF.

0110 - DS3 PERR counter. Counts one error per frame for any parity mismatches. This counter is enabled when the C-bit parity framing format is detected (RX_DS3_CPAR), and disabled by the following alarm: RX_LOS, RX_DS3_OOF.

0111 - DS3 CPERR counter. Counts one error per frame if the majority of the CP-bits mismatch. This counter is enabled when the C-bit Parity framing format is detected (RX_DS3_CPAR) and disabled by the following alarm: RX_LOS, RX_DS3_OOF.

1000 - DS3 FEBE counter. Counts one error per frame if the DS3 FEBE bits form any pattern other than 111. This counter is enabled when the C-bit Parity framing format is detected (RX_DS3_CPAR) and disabled by the following alarm: RX_LOS, RX_DS3_OOF.

1001 - Line code violation counter. Counts all BPVs and excess 0s unless RX_EXZ_DIS is set to 1. This counter is disabled by RX_LOS.

1010-1111 - Not used.

D0 RX_CNTR_LATCH

NOTE: The latch operation can be verified by ensuring that the RX_CNTR_LATCH bit in the RX_CNTR_R1 register is a 0.

1 - Initiates the latch and clear operation for the selected receiver counter.

0 - Normal operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RM_W1	27_h	0	RM_CORRECT_ DIS	0	RM_PASS_ OCD	RM_PASS_ UNASSIGNED	RM_PASS_ BAD_HEC	RM_DESCRAM_ DIS	RM_COSET_ DIS

D7 Write with a 0 to maintain compatibility with future software versions.

D6 RM_CORRECT_DIS

1 - Forces the ATM header correction circuitry into Detection Mode. In this mode, the receive ATM mapper detects all errored headers and does not correct any of them. All cells with incorrect headers are counted by the Incorrect HEC Counter and then are dropped unless RM_PASS_BAD_HEC is a 1.

0 - Allows the receive ATM mapper to correct single bit errors in accordance with ITU Recommendation I.432 (refer to "Appendix B. References" on page 123). In Correction Mode, the receiver mapper corrects headers with single bit errors and detects headers with multiple bit errors. It detects all header errors in Detection Mode. It switches from Correction Mode to Detection Mode when it detects an error. It switches from Detection Mode to Correction Mode when it detects a valid HEC (see Figure 27).

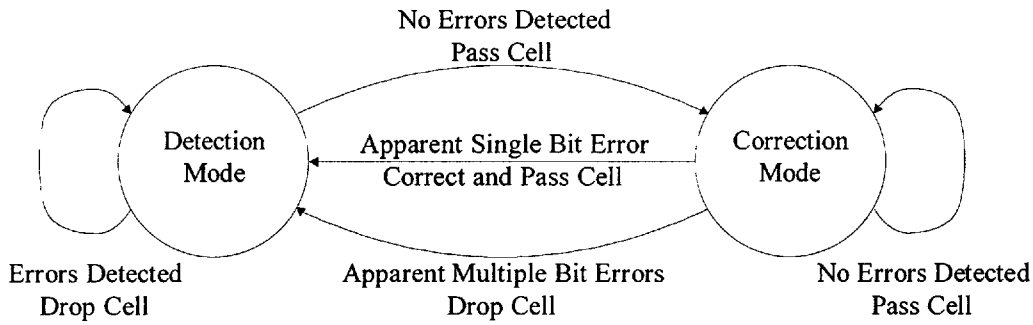

Figure 27. HEC Correction State Machine

D5 Write with a 0 to maintain compatibility with future software versions.

D4 RM_PASS_OCD

1 - Enables writing bytes to the receive ATM FIFO during OCD.

0 - Disables writing bytes to the receive ATM FIFO during OCD.

D3 RM_PASS_UNASSIGNED

1 - Enables writing physical layer and ATM layer unassigned cells to the receive ATM FIFO.

0 - Disables writing physical layer and ATM layer unassigned cells to the receive ATM FIFO.

Unassigned cells are defined as any header with the first five bytes matching $X000000XXX_h$, where X is any hexadecimal digit.

D2 RM_PASS_BAD_HEC

1 - Enables writing cells with incorrect headers to the receive ATM FIFO.

0 - Disables writing cells with incorrect headers to the receive ATM FIFO.

D1 RM_DESCRAM_DIS

1 - Disables cell payload descrambling.

0 - Enables cell payload descrambling.

D0 RM_COSET_DIS

1 - Disables the addition of the coset (55_h) to HEC values calculated by the receiver.

0 - Enables the addition of the coset (55_h) to HEC values calculated by the receiver.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RO_W1	28_h	0	0	0	0	RO_ BLOCK_ CNT_EN	RO_PLCP_ DIS	0	RO_ OOF_INS

D(7:4) Write with a 0 to maintain compatibility with future software versions.

D3 RO_BLOCK_CNT_EN

1 - Allows all BIP errors per byte to be counted as a single error in accordance with ITU Draft Recommendation G.826 (refer to "Appendix B. References" on page 123).

0 - Allows each BIP error per byte to be counted individually.

D2 RO_PLCP_DIS

1 - Disables the PLCP overhead reception.

0 - Enables PLCP overhead reception.

D1 Write with a 0 to maintain compatibility with future software versions.

D0 RO_OOF_INS

1 - Forces the receiver into the OOF state.

0 - Allows normal receiver framing operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_DS3_W1	29_h	0	0	0	0	0	0	RX_DS3_ MLOS_2_3	RX_DS3_ FLOS_6_16

D(7:2) Write with a 0 to maintain compatibility with future software versions.

D1 RX_DS3_MLOS_2_3

1 - Configures the device to lose frame synchronization when 2-out-of-3 M-bits are in error.

0 - Configures the device such that M-bit errors will not cause an out-of-frame synchronization.

D0 RX_DS3_FLOS_6_15

1 - Configures the device to lose frame synchronization when 6-out-of-15 F-bits are in error.

0 - Configures the device to lose frame synchronization when 3-out-of-15 F-bits are in error.

NOTE: The following _MASK bits disable the generation of an interrupt through the INTR pin. They do not, however, affect the operation of the associated interrupt or status bits.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
INTR_MASK_ W1	$2A_h$	RO_LOF_ MASK	RO_OOF_ MASK	RM_OCD_ MASK	RM_FIFO_ OVERFLOW_ MASK	0	RO_RAI_ MASK	0	0

D7 RO_LOF_MASK
- 1 - Disables the generation of an interrupt when a PLCP LOF event occurs.
- 0 - Enables the generation of an interrupt when a PLCP LOF event occurs.

D6 RO_OOF_MASK
- 1 - Disables the generation of an interrupt when a PLCP OOF event occurs.
- 0 - Enables the generation of an interrupt when a PLCP OOF event occurs.

D5 RM_OCD_MASK
- 1 - Disables the generation of an interrupt when the receive mapper loses or gains ATM cell delineation.
- 0 - Enables the generation of an interrupt when the receive mapper loses or gains ATM cell delineation.

D4 RM_FIFO_OVERFLOW_MASK
- 1 - Disables the generation of an interrupt when a receive ATM FIFO overflow event occurs.
- 0 - Enables the generation of an interrupt when a receive ATM FIFO overflow event occurs.

D3 Write with a 0 to maintain compatibility with future software versions.

D2 RO_RAI_MASK
- 1 - Disables the generation of an interrupt when an RAI event occurs.
- 0 - Enables the generation of an interrupt when an RAI event occurs.

D(1:0) Write with a 0 to maintain compatibility with future software versions.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
INTR_MASK_ W2	$2B_h$	RX_DS3_ CPAR_ MASK	RX_DS3_ OOF_ MASK	RX_DS3_ AIS_1010_ MASK	RX_DS3_AIS_ STUCKC_ MASK	RX_DS3_ YELLOW_ ALM_ MASK	RX_DS3_ IDLE_ MASK	RX_ DS3_ FEAC_ MASK	RX_ LOS_ MASK

D7 RX_DS3_CPAR_MASK
- 1 - Disables the generation of an interrupt when a C-bit parity framing event occurs.
- 0 - Enables the generation of an interrupt when a C-bit parity framing event occurs.

D6 RX_DS3_OOF_MASK
- 1 - Disables the generation of an interrupt when a DS3 OOF event occurs.
- 0 - Enables the generation of an interrupt when a DS3 OOF event occurs.

D5 RX_DS3_AIS_1010_MASK
- 1 - Disables the generation of an interrupt when an AIS 1010 signal event occurs.
- 0 - Enables the generation of an interrupt when an AIS 1010 signal event occurs.

D4 RX_DS3_AIS_STUCKC_MASK
- 1 - Disables the generation of an interrupt when an AIS with stuck C-bit event occurs.
- 0 - Enables the generation of an interrupt when an AIS with stuck C-bit event occurs.

D3 RX_DS3_YELLOW_ALM_MASK
- 1 - Disables the generation of an interrupt when a Yellow Alarm event occurs.
- 0 - Enables the generation of an interrupt when a Yellow Alarm event occurs.

D2 RX_DS3_IDLE_MASK
- 1 - Disables the generation of an interrupt when an Idle event occurs.
- 0 - Enables the generation of an interrupt when an Idle event occurs.

D1 RX_DS3_FEAC_MASK

1 - Disables the generation of an interrupt when a FEAC sequence other than the previous FEAC code is detected.

0 - Enables the generation of an interrupt when a FEAC sequence other than the previous FEAC code is detected.

D0 RX_LOS_MASK

1 - Disables the generation of an interrupt when a LOS event occurs.

0 - Enables the generation of an interrupt when a LOS event occurs.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TEST_W1	$2E_h$	TEST(7:0)							
TEST_W2	$2F_h$	TEST(15:8)							

ADDR=$2E_h$ and $2F_h$

D(7:0) TEST(15:0)

These registers are used for production testing. The value 00_h **must** be written into these registers for normal operation. All other values are used for production testing.

8. 4. Read Ports

NOTE: All port bits marked as "Not used" should be masked off by the software to maintain compatibility with future versions of the chip.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_CNTR_R1	03_h								TX_CNTR_ LATCH

D(7:1) Not used.
D0 TX_CNTR_LATCH

NOTE: This bit becomes a 1 when the microprocessor writes a 1 to the associated write register, indicating that the counter should be latched. This bit becomes a 0 when the latch process is completed.

1 - Counter latch in progress.
0 - Counter latch completed.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_CNTR_R1	26_h								RX_CNTR_ LATCH

D(7:1) Not used.
D0 RX_CNTR_LATCH

NOTE: This bit becomes a 1 when the microprocessor writes a 1 to the associated write register, indicating that the counter should be latched. This bit becomes a 0 when the latch process is completed.

1 - Counter latch in progress.
0 - Counter latch completed.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_CNTR_R2	27_h	TX_LATCH_COUNT(7:0)							
TX_CNTR_R3	28_h	TX_LATCH_COUNT(15:8)							

TX_LATCHED_COUNT(15:0)
This is the latched contents of the 16-bit transmit message cell counter.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_CNTR_R2	29_h	RX_LATCH_COUNT(7:0)							
RX_CNTR_R3	$2A_h$	RX_LATCH_COUNT(15:8)							

RX_LATCHED_COUNT(15:0)
This is the latched contents of one of the ten 16-bit receiver counters. The RX_CNTR_LATCH_SEL value in the RX_CNTR_W1 register determines which counter was latched.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_DS3_R1	$2B_h$			RX_FEAC(5:0)					

D(7:6) Not used.

D(5:0) RX_FEAC(5:0)

These are the six bits within the received, repeating, 16-bit FEAC code word. The FEAC code is defined as 11111110XXXXXX0, in which XXXXXX denotes RX_FEAC(5:0) and X can be a 0 or a 1. D5 is the first bit to be received from the serial data stream.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_DS3_R2	$2C_h$							RX_DS3_ X2_BIT	RX_DS3_ X1_BIT

D(7:2) Not used.

D1 RX_DS3_X2_BIT

This bit indicates the setting of the received X-bit in subframe 2.

D0 RX_DS3_X1_BIT

This bit indicates the setting of the received X-bit in subframe 1.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
INTR_R1	$2D_h$	RO_LOF_ INTR	RO_OOF_ INTR	RM_OCD_ INTR	RM_FIFO_ OVERFLOW_ INTR		RO_RAI_ INTR		

NOTE: This port is one of two interrupt registers which should be read to locate the source of an interrupt. For interrupts which are triggered on both entry and exit from a particular alarm state, an associated status bit in the STATUS_R1 register can be read to determine the current state of the alarm. This port also can be used to check for various status and alarm conditions since the last read of this port. These latched indications are cleared each time the port is read.

D7 RO_LOF_INTR: Indicates that the receiver has entered/exited the PLCP LOF state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D6 RO_OOF_INTR: Indicates that the receiver has entered/exited the PLCP OOF state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D5 RM_OCD_INTR: Indicates that the receiver has entered/exited the OCD state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D4 RM_FIFO_OVERFLOW_INTR: Indicates that the receiver has entered/exited the receive ATM FIFO overflow state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D3 Not used.

D2 RO_RAI_INTR: Indicates that the receiver has entered/exited the RAI state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D1-D0 Not used.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
INTR_R2	$2E_h$								

NOTE: This port is one of two interrupt registers which should be read to locate the source of an interrupt. For interrupts which are triggered on both entry and exit from a particular alarm state, an associated status bit in the STATUS_R2 register can be read to determine the current state of the alarm. This port can also be used simply to check for the occurrence of various status and alarm conditions since the last read of this port. These latched indications are cleared each time the port is read.

D7 RX_DS3_CPAR_INTR: Indicates that the receiver has entered/exited the DS3 C-bit parity framing state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D6 RX_DS3_OOF_INTR: Indicates that the receiver has entered/exited the DS3 OOF state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D5 RX_DS3_AIS_1010_INTR: Indicates that the receiver has entered/exited the AIS 1010 signal state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D4 RX_DS3_AIS_STUCKC_INTR: Indicates that the receiver has entered/exited the AIS with stuck C-bit state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D3 RX_DS3_YELLOW_ALM_INTR:Indicates that the receiver has entered/exited the Yellow Alarm state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D2 RX_DS3_IDLE_INTR: Indicates that the receiver has entered/exited the Idle state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D1 RX_DS3_FEAC_INTR: Indicates that the receiver has detected a change in the FEAC sequence since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D0 RX_LOS_INTR: Indicates that the receiver has entered/exited the LOS state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
STATUS_ R1	$2F_h$	RO_LOF	RO_OOF	RM_OCD	RM_FIFO_ OVERFLOW		RO_RAI		

D7 RO_LOF
- 1 - Indicates that the receiver is detecting a PLCP LOF.
- 0 - Indicates that the receiver is not detecting a PLCP LOF.

D6 RO_OOF
- 1 - Indicates that the receiver is detecting a PLCP OOF.
- 0 - Indicates that the receiver is not detecting a PLCP OOF.

D5 RM_OCD
- 1 - Indicates that the receiver is detecting OCD.
- 0 - Indicates that the receiver is not detecting OCD.

D4 RM_FIFO_OVERFLOW
- 1 - Indicates that the receive ATM FIFO is in overflow state.
- 0 - Indicates that the receive ATM FIFO is not in overflow state.

D3 Not used.

D2 RO_RAI
- 1 - Indicates that the receiver is detecting RAI.
- 0 - Indicates that the receiver is not detecting RAI.

D(1:0) Not used.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
STATUS_ R2	30_h	RX_DS3_ CPAR	RX_DS3_ OOF	RX_DS3_ AIS_1010	RX_DS3_ AIS_ STUCKC	RX_DS3_ YELLOW_ ALM	RX_DS3_ IDLE		RX_LOS

D7 RX_DS3_CPAR
- 1 - Indicates that the receiver is detecting a DS3 C-bit Parity framing format.
- 0 - Indicates that the receiver is not detecting a DS3 C-bit Parity framing format.

D6 RX_DS3_OOF
- 1 - Indicates that the receiver is detecting a DS3 OOF.
- 0 - Indicates that the receiver is not detecting a DS3 OOF.

D5 RX_DS3_AIS_1010
- 1 - Indicates that the receiver is detecting an AIS 1010 signal condition.
- 0 - Indicates that the receiver is not detecting an AIS 1010 signal condition.

D4 RX_DS3_AIS_STUCKC
- 1 - Indicates that the receiver is detecting an AIS stuck C-bit condition.
- 0 - Indicates that the receiver is not detecting an AIS stuck C-bit condition.

D3 RX_DS3_YELLOW_ALM
- 1 - Indicates that the receiver is detecting a Yellow Alarm.
- 0 - Indicates that the receiver is not detecting a Yellow Alarm.

D2 RX_DS3_IDLE
- 1 - Indicates that the receiver is detecting an Idle pattern.
- 0 - Indicates that the receiver is not detecting an Idle pattern.

D1 Not used.

D0 RX_LOS
- 1 - Indicates that the receiver is detecting LOS.
- 0 - Indicates that the receiver is not detecting LOS.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
HW_REV	$3F_h$	0	0	0	0	0	0	0	0

D(7:0) HW_REV

This is the hardware revision level of the device.

E3/E4 APPLICATION

9. SYSTEM FEATURES

9. 1. Rates

- Up to 139.264 Mbps (E4) using the parallel interface.
- 34.368 Mbps (E3) using the serial interface.

9. 2. Setup

- Transmitter and receiver can be set up and accessed independently.

9. 3. Loopback

- Local: TX_SER_DATA and TX_SER_CLK is fed back to RX_SER_DATA and RX_SER_CLK for E3 serial mode.
  TX_PAR_DATA and TX_PAR_CLK is fed back to RX_PAR_DATA and RX_PAR_CLK for parallel mode.

9. 4. Testability

- All outputs can be tristated.
- Boundary scan (JTAG) on all pins.

9. 5. Framing Format

The E4 framing format is shown in Figure 28. *Active* overhead bytes (bytes processed by the WAC-034-B) are labeled with the appropriate E4 symbols. Table 27 on page 65 describes the values used for coding the active E4 overhead bytes. *Inactive* overhead bytes (bytes not processed by the WAC-034-B) are transmitted as 00_h, and are ignored by the receiver. Descriptions of the processing performed on each one of the active bytes are given in section "10. Transmitter Features" on page 66 and section "11. Receiver Features" on page 67.

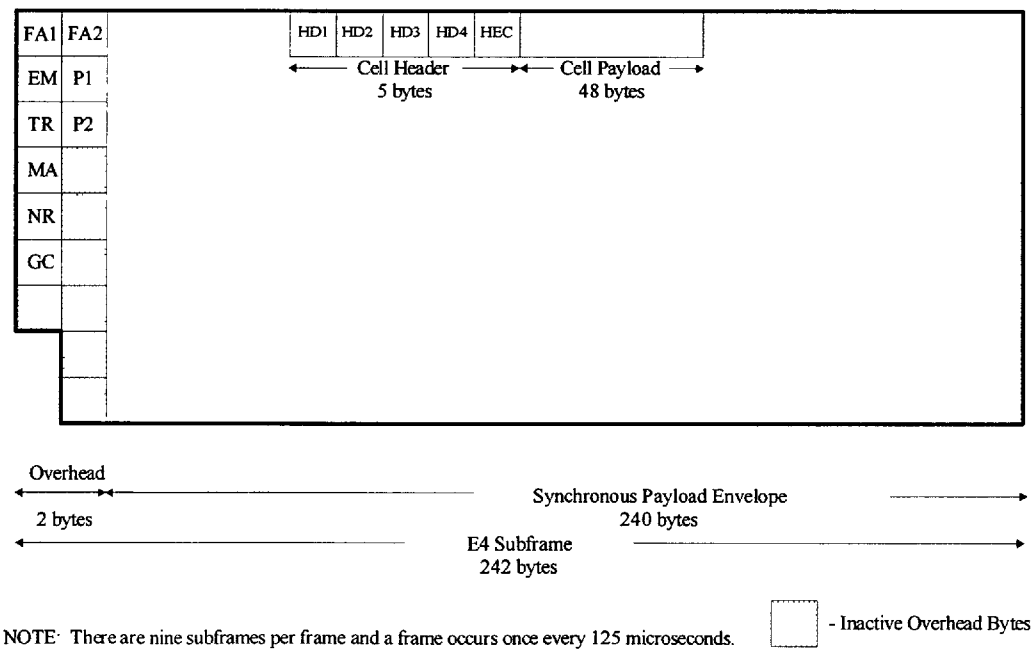

Figure 28. E4 Framing Format

The E3 framing format is shown in Figure 29. *Active* overhead bytes (bytes processed by the WAC-034-B) are labeled with the appropriate E3 symbols. Table 27 on page 65 describes the values used for coding the active E3 overhead bytes. *Inactive* overhead bytes (bytes not processed by the WAC-034-B) are transmitted as 00_h and are ignored by the receiver. Descriptions of the processing performed on each one of the active bytes is given in section "10. Transmitter Features" on page 66 and "11. Receiver Features" on page 67.

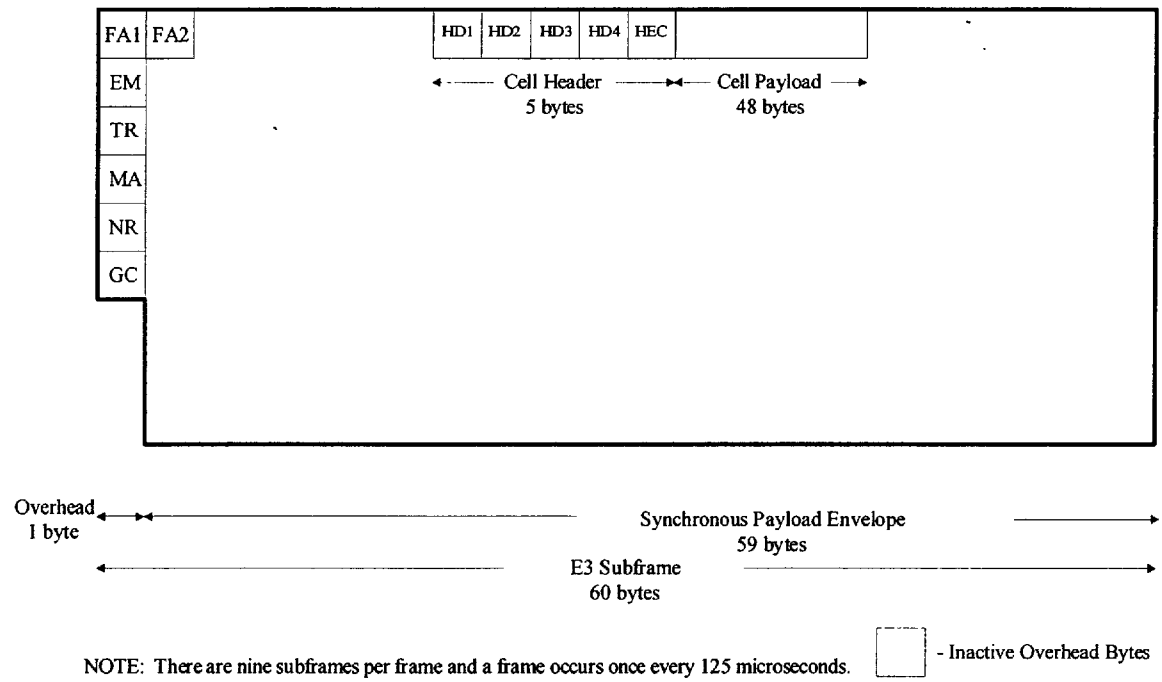

Figure 29. E3 Framing Format

Table 27 describes the values used for coding the active E3/E4 overhead bytes. Bits are shown in parentheses; bit 7 is the most significant bit and is the first bit to be transmitted in the data stream, and bit 0 is the least significant bit and is the last bit to be transmitted in the data stream. For example, the first bit of the MA byte is indicated as MA(7). This numbering scheme maintains consistency between the pin descriptions and the microprocessor port register descriptions. Default values used by the transmitter are indicated by (def).

Table 27. Values for the E3/E4 Overhead Bytes

Overhead Location	Function	Value
FA1	Frame alignment	$F6_h$
FA2	Frame alignment	28_h
EM	Error monitoring	BIP-8
TR	Trail trace	00_h
MA(7)	No alarm RDI	0 (def) 1
MA(6)	No EM errors Far-End Block Error (FEBE)	0 (def) 1
MA(5:3)	Payload type: ATM Payload type: unequipped	010 (def) 000
MA(2:1)	Payload dependent	00 (def)
MA(0)	Timing marker	0 (def)
NR	Network operator byte	00_h
GC	General purpose communications channel	FF_h
P1	Automatic protection switching	00_h
P2	Automatic protection switching	00_h

10. TRANSMITTER FEATURES

10. 1. General

10. 1. 1. PDH Data Insertion

- The default values for all PDH data, including the overhead, can be overwritten through a synchronous 8-bit interface.

10. 1. 2. Error Insertion

- Single and continuous error insertion capabilities are valid for all bytes specified as having a general error insertion feature.

10. 1. 3. Automatic Alarm Generation

- Dedicated internal circuitry or an external signal will generate the appropriate alarm signal upon detection of an alarm condition (for example, FEBE).
- Software can force alarm signal generation.

10. 2. ATM

- Provides a three cell deep, cell-by-cell FIFO to decouple system and line side clocks.
- Generates null cells with programmable header and programmable one-byte payload pattern.
- Optionally generates header error check (HEC) with error insertion on any bits.
- Optionally generates the HEC without the coset pattern.
- Optionally scrambles the cell payload.
- Counts the number of message cells transmitted.
- Detects transmit FIFO empty and begins sending a null cell immediately.

10. 3. Overhead Processing

- Generates Frame Alignment (FA1 and FA2) with continuous error insertion on the most significant bit (bit 7).
- Generates Error Monitoring (EM BIP-8) with error insertion on all 8 bits simultaneously.
- Generates Trail Trace (TR) message from programmable 16-byte RAM.
- Generates Memory Administration (MA) Remote Defect Indication (RDI) when the MA_RDI signal is asserted.
- Automatically generates MA Far-End Block Errors (FEBE) on reception of EM byte errors.
- Generates MA payload type as either ATM (010) or unequipped (000).
- Generates MA payload dependent bits.
- Generates MA timing marker bit.
- Generates Alarm Indication Signal (AIS - the transmit data stream is forced to 1).
- Generates the frame pulse to indicate Start-Of-Frame (TO_FRAME).
- Synchronizes the frame format to an external frame synchronization signal (TO_FRAME_IN).

10. 4. Line Interface Processing

- Generates Loss-Of-Signal (LOS - the transmit data stream is forced to 0).
- Optionally encodes E3 serial data in High Density Bipolar 3 (HDB3) or Alternating Mark Inversion (AMI) format.
- Optionally generates single Bipolar Violations (BPVs).

11. RECEIVER FEATURES

11. 1. General

11. 1. 1. PDH Data Monitoring

- Monitors the full PDH data stream, including all the overhead bytes, through a synchronous 8-bit interface.

11. 1. 2. Counters

- Counter length is 16 bits.
- Counters are latched synchronously and cleared when latched.

11. 1. 3. Alarms

- One hardware pin is associated with each alarm.
- One interrupt is generated with each alarm. Each interrupt has three microprocessor bits: mask, interrupt, and status.

11. 2. ATM

- Provides a three cell deep, cell-by-cell FIFO to decouple system and line side clocks.
- Performs cell delineation by checking for HEC matches.
- Detects out-of-cell delineation (RM_OCD) in accordance to ITU Recommendation I.432 (refer to "Appendix B. References" on page 123), where delta is 6 and alpha is 7.
- Detects FIFO overflow with RA_FIFO_OVERFLOW_INTR.
- Optionally corrects first header with a single apparent bit error (Correction Mode for ATM cell header processing).
- Optionally subtracts coset from HEC.
- Optionally passes cells with invalid HECs.
- Optionally passes unassigned cells. (Unassigned cells have the following five header bytes, $X000000XXX_h$ where X is any hexadecimal digit).
- Optionally passes data during receive out-of-cell delineation.
- Optionally descrambles the cell payload.
- Counts complete cells written to the receive FIFO.
- Counts all cells with invalid HECs in Detection Mode for ATM cell header processing, and counts all cells with uncorrectable HECs in Correction Mode.

11. 3. Overhead Processing

- Allows software to force a receive *Out-Of-Frame* (RO_OOF) condition.
- Detects Out-Of-Frame (RO_OOF).
  RO_OOF is set if four consecutive invalid frames are detected.
  RO_OOF is reset if two consecutive valid frames are detected.
- Detects Loss-Of-Frame (RO_LOF).
  RO_LOF is set if 3 ms of Out-Of-Frame (OOF) are accumulated with fewer than 3 ms of in-frame between OOFs.
  RO_LOF is reset if 3 consecutive ms of in-frame are detected.
- Optionally counts EM (BIP-8) errors individually or as a block.
- Provides microprocessor access to TR trail trace message bytes.
- Detects trail trace CRC7 calculation changes by comparing the calculated CRC7 value for the current 16-byte cycle to the calculated CRC7 value for the previous 16-byte cycle.
- Detects trail trace CRC7 calculation validity by comparing the calculated CRC7 value to the received CRC7 value for the current 16-byte cycle.
- Detects MA RDI.
  RO_RDI is set if 3 consecutive MA bytes are set to 1XXXXXXX
  RO_RDI is reset if 3 consecutive MA bytes are set to 0XXXXXXX
- Counts MA FEBEs.
- Detects MA payload type mismatches.
  Valid signal label values are ATM (010) and equipped-non specific (001).
- Detects AIS (RX_AIS).
  RX_AIS is valid if a continuous stream of 1's, in the presence of an error ratio of $1x10^{-3}$, is detected in each of two consecutive frame periods.
  RX_AIS is reset if a continuous stream of 1's, in the presence of an error ratio of $1x10^{-3}$, is not detected in each of two consecutive frame periods.

11. 4. Line Interface Processing

- Detects LOS (RX_LOS) for E3.
  RX_LOS is valid if the serial data stream is stuck at all 0s or all 1s for a period of 255 contiguous bit positions.
  RX_LOS is reset on the detection of an average pulse density of at least 12.5 percent over a period of 255 contiguous bit positions.
- Optionally decodes E3 serial data in HDB3 or AMI format.
- Counts BPVs as line code violations.
- Optionally counts excess 0s as line code violations.

12. PIN DESCRIPTIONS

12. 1. Package Diagram

Figure 30 shows the physical dimensions for the 144-pin plastic quad flat pack used for the WAC-034-B.

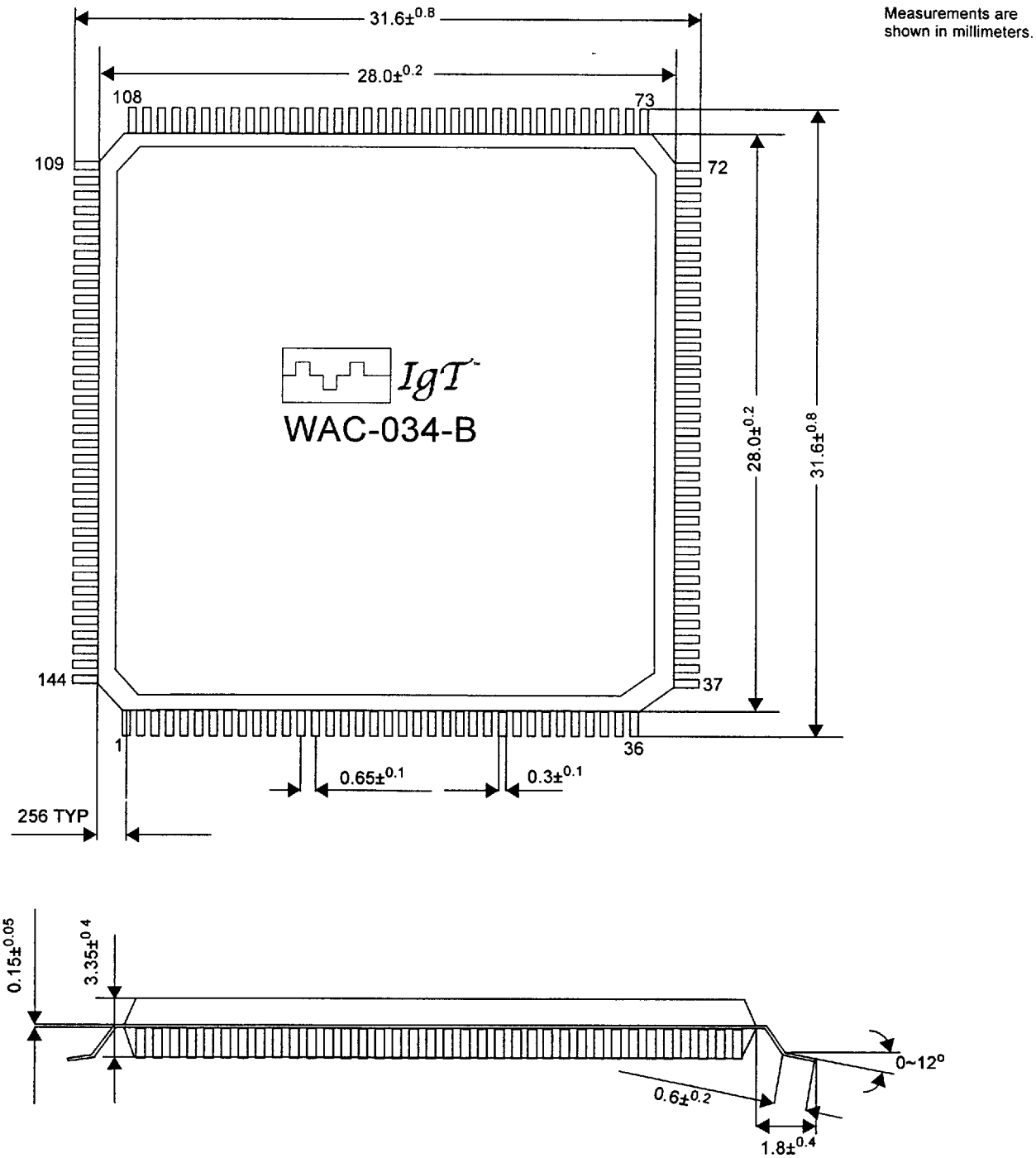

Figure 30. WAC-034-B Package (PQFP-144)

Figure 31 displays the pins of the WAC-034-B grouped by logical functions. Arrows heading toward the device are input pins, those heading away from the device are output pins, and those heading both toward and away from the device are bidirectional pins. Larger arrows are buses (multiple pins).

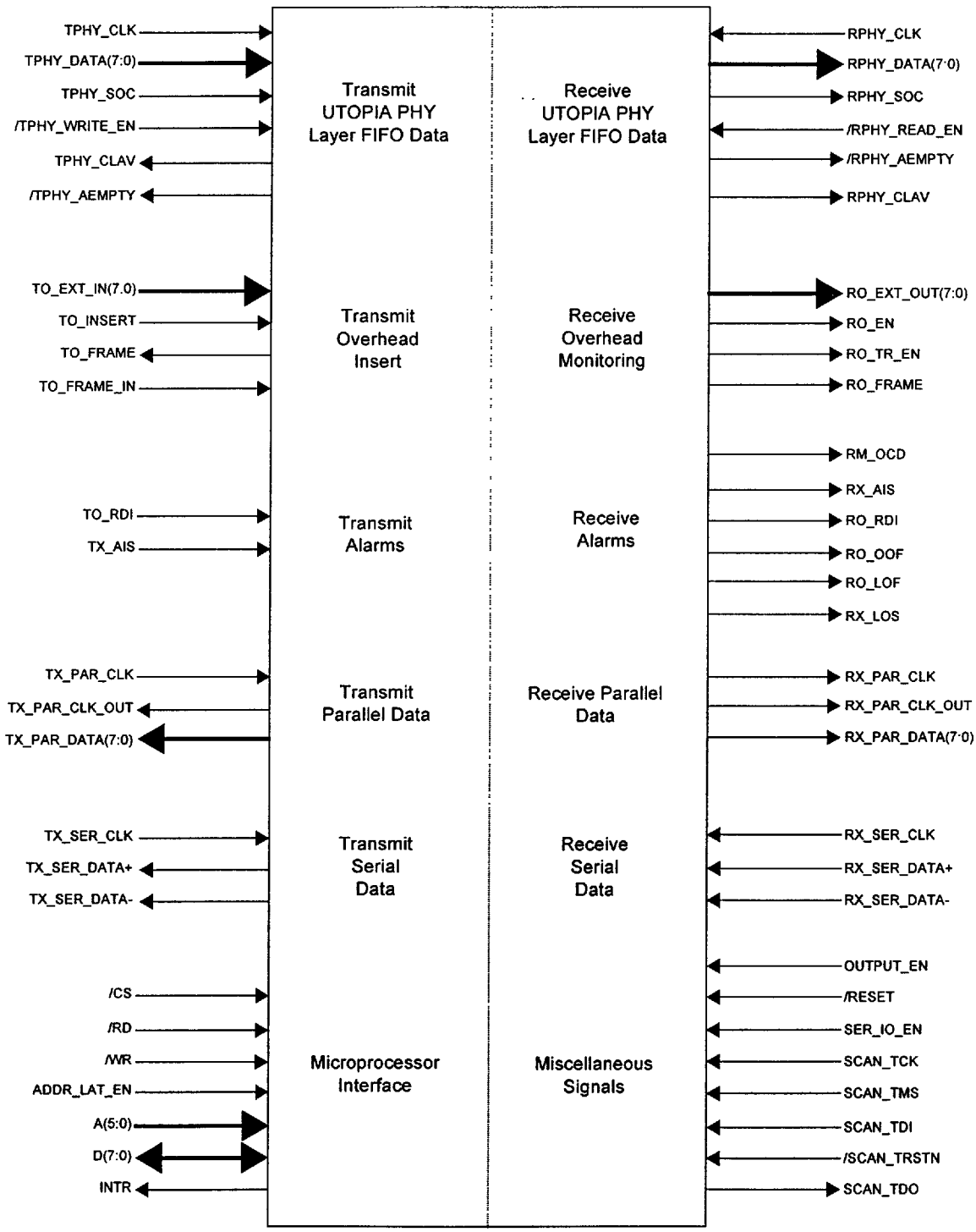

Figure 31. WAC-034-B Logical Pin Diagram for E3/E4 Applications

12. 2. Pin Locations

Refer to Table A-1 on page 121 for pin name prefix explanations.

Table 28. Pin Locations

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	/CS	37	VCC	73	VCC	109	VCC
2	/RD	38	RPHY_SOC	74	SER_IO_EN	110	TX_PAR_DATA6
3	/WR	39	RPHY_CLAV	75	RX_SER_DATA-	111	TX_PAR_DATA7
4	A0	40	/RPHY_AEMPTY	76	RX_SER_DATA+	112	TX_PAR_CLK_OUT
5	A1	41	RO_TR_EN	77	GND	113	TO_FRAME
6	A2	42	SCAN_TCK	78	N/C	114	TO_FRAME_IN
7	A3	43	SCAN_TMS	79	RX_SER_CLK	115	TO_INSERT
8	A4	44	SCAN_TDI	80	GND	116	TO_EXT_IN0
9	A5	45	SCAN_TDO	81	NC	117	TO_EXT_IN1
10	NC	46	RO_EXT_OUT0	82	RX_PAR_DATA0	118	TO_EXT_IN2
11	NC	47	RO_EXT_OUT1	83	RX_PAR_DATA1	119	TO_EXT_IN3
12	D0	48	RO_EXT_OUT2	84	RX_PAR_DATA2	120	TO_EXT_IN4
13	D1	49	RO_EXT_OUT3	85	RX_PAR_DATA3	121	TO_EXT_IN5
14	D2	50	RO_EXT_OUT4	86	RX_PAR_DATA4	122	TO_EXT_IN6
15	D3	51	RO_EXT_OUT5	87	RX_PAR_DATA5	123	TO_EXT_IN7
16	D4	52	RO_EXT_OUT6	88	RX_PAR_DATA6	124	DS3 IN
17	D5	53	RO_EXT_OUT7	89	RX_PAR_DATA7	125	DS3 OUT
18	GND	54	GND	90	RX_PAR_CLK	126	GND
19	VCC	55	VCC	91	N/C	127	VCC
20	D6	56	RM_OCD	92	GND	128	TO_RDI
21	D7	57	DS3 OUT	93	TX_AIS	129	ADDR_LAT_EN
22	INTR	58	/TPHY_AEMPTY	94	TX_SER_CLK	130	DS3 OUT
23	/RESET	59	DS3 OUT	95	VCC	131	/TPHY_WRITE_EN
24	OUTPUT_EN	60	DS3 OUT	96	GND	132	TPHY_SOC
25	RPHY_DATA0	61	RO_EN	97	TX_SER_DATA+	133	TPHY_CLK
26	RPHY_DATA1	62	DS3 OUT	98	TX_SER_DATA-	134	TPHY_DATA0
27	RPHY_DATA2	63	RO_RDI	99	GND	135	TPHY_DATA1
28	RPHY_DATA3	64	RX_AIS	100	VCC	136	TPHY_DATA2
29	GND	65	GND	101	TX_PAR_CLK	137	TPHY_DATA3
30	RPHY_DATA4	66	RX_LOS	102	TX_PAR_DATA0	138	TPHY_DATA4
31	RPHY_DATA5	67	RO_OOF	103	TX_PAR_DATA1	139	TPHY_DATA5
32	RPHY_DATA6	68	RO_LOF	104	TX_PAR_DATA2	140	TPHY_DATA6
33	RPHY_DATA7	69	RO_FRAME	105	TX_PAR_DATA3	141	TPHY_DATA7
34	/RPHY_READ_EN	70	RX_PAR_CLK_OUT	106	TX_PAR_DATA4	142	DS3 IN
35	RPHY_CLK	71	/SCAN_TRSTN	107	TX_PAR_DATA5	143	TPHY_CLAV
36	GND	72	N/C	108	GND	144	GND

12. 3. Pin Descriptions

Refer to Table A-1 on page 121 for pin name prefix explanations.

12. 3. 1. UTOPIA PHY Layer FIFO Data Signals

12. 3. 1. 1. Transmit UTOPIA PHY Layer FIFO Data Signals

Table 29. Transmit UTOPIA PHY Layer FIFO Data Signals

Signal Name	Pin #	Type	Description
TPHY_CLK	133	In	*Transmit UTOPIA PHY Layer Clock* is used to write data from the ATM layer into the transmit ATM FIFO.
TPHY_DATA(7:0)	141-134	In	*Transmit UTOPIA PHY Layer Data Bits 7 to 0* are part of the 8-bit ATM data byte being written into the transmit ATM FIFO. Bit 7 is the first bit transmitted once the parallel byte is serialized. Bit 0 is the last bit transmitted once the parallel byte is serialized
TPHY_SOC	132	In	*Transmit UTOPIA PHY Layer Start-Of-Cell* indicates that the data being written into the transmit ATM FIFO is the first byte of the 53-byte ATM cell.
/TPHY_WRITE_EN	131	In	*Transmit UTOPIA PHY Layer Write Enable* is an active low signal used to enable writing data into the transmit ATM FIFO.
TPHY_CLAV	143	Out	*Transmit UTOPIA PHY Layer Cell Available* is an active high signal used to indicate that the transmit ATM FIFO can accept a complete cell. When this signal is low, the transmit ATM FIFO is able to accept at most four more bytes of data before it becomes full.
/TPHY_AEMPTY	58	Out	*Transmit UTOPIA PHY Layer FIFO Almost Empty* is an active low signal used to indicate that the transmit ATM FIFO has fewer than 51 bytes of data left. Note that this signal is synchronous to the transmit line clock (TX_SER_CLK or TX_PAR_CLK) and not to TPHY_CLK.

12. 3. 1. 2. Receive UTOPIA PHY Layer FIFO Data Signals

Table 30. Receive UTOPIA PHY Layer FIFO Data Signals

Signal Name	Pin #	Type	Description
RPHY_CLK	35	In	*Receive UTOPIA PHY Layer Clock* is used by the ATM layer to read data from the receive ATM FIFO.
RPHY_DATA(7:4) RPHY_DATA(3:0)	33 - 30 28 - 25	Out	*Receive UTOPIA PHY Layer Data Bits 7 to 0* are part of the 8-bit ATM data byte being read from the receive ATM FIFO. Bit 7 the first bit received once the parallel byte is serialized. Bit 0 is the last bit received once the parallel byte is serialized.
RPHY_SOC	38	Out	*Receive UTOPIA PHY Layer Start-Of-Cell* indicates that the data being read from the receive ATM FIFO is the first byte of the 53-byte ATM cell.
/RPHY_READ_EN	34	In	*Receive UTOPIA PHY Layer Read Enable* is an active low signal used to indicate that the ATM layer is reading data from the receive ATM FIFO.
/RPHY_AEMPTY	40	Out	*Receive UTOPIA PHY Layer Almost Empty* is an active low signal used to indicate that the receive ATM FIFO contains fewer than 50 bytes.
RPHY_CLAV	39	Out	*Receive UTOPIA PHY Layer Cell Available* is an active high signal used to indicate that the receive ATM FIFO contains a full cell (53 or more bytes).

12. 3. 2. Overhead Signals

12. 3. 2. 1. Transmit Overhead Insert Signals

Table 31. Transmit Overhead Insert Signals

Signal Name	Pin #	Type	Description
TO_EXT_IN7	123	In	*Transmit Overhead External In Bit 7* is bit 7 of the 8-bit parallel data that can overwrite the default PDH data stream. This pin can also be used to overwrite GFC3 of each cell when GFC_EN (A=00_h, D5) is a 1 and GFC_MASK3 (A=$0A_h$, D7) is a 1. This is the first bit transmitted once the parallel byte is serialized.
TO_EXT_IN6	122	In	*Transmit Overhead External In Bit 6* is bit 6 of the 8-bit parallel data that can overwrite the default PDH data stream. This pin can also be used to overwrite GFC2 of each cell when GFC_EN (A=00_h, D5) is a 1 and GFC_MASK2 (A=$0A_h$, D6) is a 1.
TO_EXT_IN5	121	In	*Transmit Overhead External In Bit 5* is bit 5 of the 8-bit parallel data that can overwrite the default PDH data stream. This pin can also be used to overwrite GFC1 of each cell when GFC_EN (A=00_h, D5) is a 1 and GFC_MASK1 (A=$0A_h$, D5) is a 1.
TO_EXT_IN4	120	In	*Transmit Overhead External In Bit 4* is bit 4 of the 8-bit parallel data that can overwrite the default PDH data stream. This pin can also be used to overwrite GFC0 of each cell when GFC_EN (A=00_h, D5) is a 1 and GFC_MASK0 (A=$0A_h$, D4) is a 1.
TO_EXT_IN(3:0)	119-116	In	*Transmit Overhead External In Bits 3 to 0* are part of the 8-bit parallel data that can overwrite the default PDH data stream.
TO_INSERT	115	In	*Transmit Overhead Insert* indicates that the current *Transmit Overhead External In* (TO_EXT_IN) byte should overwrite the default PDH data stream.
TO_FRAME	113	Out	*Transmit Overhead Frame* is an active high signal which is asserted once per frame when *Transmit Parallel Data* (TX_PAR_DATA) contains the FA2 byte.
TO_FRAME_IN	114	In	*Transmit Overhead Frame Input* is an active high signal which can be asserted to synchronize the transmitter to an external event. This signal should be asserted when the FA2 byte is desired at *Transmit Parallel Data* (TX_PAR_DATA).
TO_RDI	128	In	*Transmit Overhead Remote Defect Indicator* inserts RDI into the transmit data stream.

12. 3. 2. 2. Receive Overhead Monitoring Signals

Table 32. Receive Overhead Monitoring Signals

Signal Name	Pin #	Type	Description
RO_EXT_OUT7	53	Out	*Receive Overhead External Out Bit 7* is bit 7 of the 8-bit PDH data when GFC_EN (Addr=00_h, D5) is a 0. This pin is used to report GFC3 of each valid cell when GFC_EN is a 1. This bit is the first bit received once the parallel byte is serialized. If GFC_EN is a 0, then the *Receive Overhead External Out* signals, in conjunction with *Receive Overhead Frame* (RO_FRAME), *Receive Overhead Enable* (RO_EN), and *Receive Overhead Trail Trace Enable* (RO_TR_EN), can be used to monitor the PDH overhead data.
RO_EXT_OUT6	52	Out	*Receive Overhead External Out Bit 6* is bit 6 of the 8-bit PDH data when GFC_EN (Addr=00_h, D5) is a 0. This pin is used to report GFC2 of each valid cell when GFC_EN is a 1.
RO_EXT_OUT5	51	Out	*Receive Overhead External Out Bit 5* is bit 5 of the 8-bit PDH data when GFC_EN (Addr=00_h, D5) is a 0. This pin is used to report GFC1 of each valid cell when GFC_EN is a 1.
RO_EXT_OUT4	50	Out	*Receive Overhead External Out Bit 4* is bit 4 of the 8-bit PDH data when GFC_EN (Addr=00_h, D5) is a 0. This pin is used to report GFC0 of each valid cell when GFC_EN is a 1.
RO_EXT_OUT(3:0)	49 - 46	Out	*Receive Overhead External Out Bits 3 to 0* are bits 3 to 0 of the 8-bit PDH data. Bit 0 is the last bit received once the parallel byte is serialized
RO_EN	61	Out	*Receive Overhead Enable* indicates that the current *Receive Overhead External Out* (RO_EXT_OUT) is a PDH overhead byte.
RO_TR_EN	41	Out	*Receive Overhead Trail Trace Enable* indicates that the current *Receive Overhead External Out* (RO_EXT_OUT) contains the TR byte.
RO_FRAME	69	Out	*Receive Overhead Frame* is an active high signal asserted to indicate that a framing pattern was detected. This frame pulse is asserted when the *Receive Overhead External Out* (RO_EXT_OUT) signal contains the third payload data byte.

12. 3. 3. Alarms

12. 3. 3. 1. Transmit Alarms

Table 33. Transmit Alarms

Signal Name	Pin #	Type	Description
TO_RDI	128	In	*Transmit Overhead Remote Defect Indicator* inserts RDI into the transmit data stream.
TX_AIS	93	In	*Transmit Alarm Indication Signal* inserts the AIS into the transmit data stream.

12. 3. 3. 2. Receive Alarms

Table 34. Receive Alarms

Signal Name	Pin #	Type	Description
RM_OCD	56	Out	*Receive Mapper Out-Of-Cell Delineation* indicates that the receiver has lost ATM cell delineation.
RX_AIS	64	Out	*Receive Alarm Indication Signal* indicates that the receiver is detecting AIS.
RO_RDI	63	Out	*Receive Overhead Remote Defect Indicator* indicates that the receiver is detecting RDI.
RO_OOF	67	Out	*Receive Overhead Out-Of-Frame* indicates that the receiver is out-of-frame.
RO_LOF	68	Out	*Receive Overhead Loss-Of-Frame* indicates that the receiver has entered the loss-of-frame alarm state.
RX_LOS	66	Out	*Receive Loss-Of-Signal* indicates that the receiver is detecting loss-of-signal (the incoming data is stuck at 1 or 0). This signal is applicable only to E3.

12. 3. 4. Parallel Data Signals

12. 3. 4. 1. Transmit Parallel Data Signals

Table 35. Transmit Parallel Data Signals

Signal Name	Pin #	Type	Description
TX_PAR_CLK	101	In	*Transmit Parallel Clock* is the parallel clock used to generate *Transmit Parallel Data* (TX_PAR_DATA). This clock's frequency is 17.408 MHz for E4, and 4.296 MHz for E3.
TX_PAR_CLK_OUT	112	Out	*Transmit Parallel Clock Out* is the transmit parallel clock output of the chip, and is configured to provide an appropriate output clock depending on the setting of *Serial Input/Output Enable* (SER_IO_EN). When SER_IO_EN is low, *Transmit Parallel Clock Out* is equivalent to *Transmit Parallel Clock* (TX_PAR_CLK). When SER_IO_EN is high, *Transmit Parallel Clock Out* is equivalent to *TransmitSerial Clock* (TX_SER_CLK) divided by eight.
TX_PAR_DATA(7:6) TX_PAR_DATA(5:0)	111-110 107-102	Out	*Transmit Parallel Data Bits 7 to 0* are part of the 8-bit parallel data. Bit 7 is the first bit transmitted once the parallel byte is serialized. Bit 0 is the last bit transmitted once the parallel byte is serialized.

12. 3. 4. 2. Receive Parallel Data Signals

Table 36. Receive Parallel Data Signals

Signal Name	Pin #	Type	Description
RX_PAR_CLK	90	In	*Receive Parallel Clock* is the clock used to write parallel PDH data into the receiver.
RX_PAR_CLK_OUT	70	Out	*Receive Parallel Clock Out* is the receive parallel clock output of the chip, and is configured to provide an appropriate output clock depending on the setting of *Serial Input/Output Enable* (SER_IO_EN). When SER_IO_EN is low, *Receive Parallel Clock Out* is equivalent to *Receive Parallel Clock* (RX_PAR_CLK). When SER_IO_EN is high, *Receive Parallel Clock Out* is equivalent to *Receive Serial Clock* (RX_SER_CLK) divided by eight.
RX_PAR_DATA(7:0)	89-82	In	*Receive Parallel Data Bits 7 to 0* are part of the 8-bit parallel PDH data to be written into the receiver. Bit 7 and Bit 0 data does not have to be byte-aligned to the PDH frame. Bit 7 is the first bit received once the parallel byte is serialized. Bit 0 is the last bit received once the parallel byte is serialized.

12. 3. 5. Serial Data Signals

12. 3. 5. 1. Transmit Serial Data Signals

Table 37. Transmit Serial Data Signals

Signal Name	Pin #	Type	Description
TX_SER_CLK	94	In	*Transmit Serial Clock* is the serial clock used to generate *Transmit PHY Layer Serial Data* (TX_SER_DATA). This clock's frequency is 34.368 MHz for E3.
TX_SER_DATA+	97	Out	*Transmit Serial Data Plus* is the Non-Return to Zero (NRZ) data when bipolar is disabled, and represents a positive AMI/HDB3-encoded pulse when bipolar is enabled.
TX_SER_DATA-	98	Out	*Transmit Serial Data Minus* is the inverted NRZ data when bipolar is disabled, and represents a negative AMI/HDB3-encoded pulse when bipolar is enabled.

12. 3. 5. 2. Receive Serial Data Signals

Table 38. Receive Serial Data Signals

Signal Name	Pin #	Type	Description
RX_SER_CLK	79	In	*Receive Serial Clock* is the serial clock used to write serial data into the receiver. This clock's frequency is 34.368 MHz for E3.
RX_SER_DATA+	76	In	*Receive Serial Data Plus* is the serial data stream that is written into the receiver. This signal is NRZ data when bipolar is disabled, and the positive half of the AMI/HDB3 encoded pulse when bipolar is enabled.
RX_SER_DATA-	75	In	*Receive Serial Data Minus* is the negative half of the AMI/HDB3 encoded signal that is written into the receiver when bipolar is enabled.

12. 3. 6. Microprocessor Interface Signals

Table 39. Microprocessor Interface Signals

Signal Name	Pin #	Type	Description
/CS	1	In	*Chip Select* is an active low signal used to select the device.
/RD	2	In	*Read* is an active low read signal from the external microprocessor.
/WR	3	In	*Write* is an active low write signal from the external microprocessor.
ADDR_LAT_EN	129	In	*Address Latch Enable* is used to latch the value of the bus. A high value enables the internal transparent latches on the address bus. The value on the address bus is latched on the falling edge of address latch enable. If not used, this signal should be tied high.
A(5:0)	9 - 4	In	*Address Bits 5 to 0* are part of the 6-bit microprocessor address bus.
D(7:6) D(5:0)	21 - 20 17 - 12	Bi	*Data Bits 7 to 0* are part of the 8-bit microprocessor data bus.
INTR	22	Out	*Interrupt* goes high when an alarm condition is detected. Each condition is independently maskable. *Interrupt* goes low after all INTR read ports are read.

12. 3. 7. Miscellaneous Signals

Table 40. Miscellaneous Signals

Signal Name	Pin #	Type	Description
OUTPUT_EN	24	In	*Output Enable* is an active high signal used to enable all output signals. A low on this signal forces all output pins into a high impedance state.
/RESET	23	In	*Reset* is an active low signal used to force all microprocessor write ports to the default setting, and to reset both the transmitter and the receiver.
SER_IO_EN	74	In	*Serial Input/Output Enable* is used to enable the serial PDH section input/output streams. When *Serial Input/Output Enable* is high, the PDH interface is configured to handle serial I/O. When *Serial Input/ Output Enable* is low, the PDH interface is configured to handle parallel I/O. For E3 HDB3 encoded/decoded data, *Serial Input/Output Enable* must be set high.
SCAN_TCK	42	In	*Scan Test Clock* is an independent clock used to drive the internal boundary scan test logic. This signal should be connected to +5 volts through a pull-up resistor.
SCAN_TMS	43	In	*Scan Test Mode Select* controls the operation of the internal boundary scan test logic. This signal should be connected to +5 volts through a pull-up resistor.
SCAN_TDI	44	In	*Scan Test Data Input* is the serial input for boundary scan test data and instruction bits. This signal should be connected to +5 volts through a pull-up resistor.
/SCAN_TRSTN	71	In	*Scan Test Reset* is an active low signal used to reset the internal boundary scan test logic. When not using boundary scan, this signal should be connected to ground through a pull-down resistor.
SCAN_TDO	45	Out	*Scan Test Data Output* is the serial output for boundary scan test data.
VCC	19, 37, 55, 73, 95, 100, 109, 127	In	Supply voltage 5 ± 0.25 volts.
GND	18, 29, 36, 54, 65, 77, 80, 92, 96, 99, 108, 126, 144	In	Ground.
N/C	10, 11, 72, 78, 81, 91		No connection. All no-connection pins should be connected to ground through a resistor to maintain compatibility with future hardware revisions.
DS3 IN	124, 142	In	DS3 inputs are input signals used for different applications. All DS3 input pins should be connected to ground through a resistor.
DS3 OUT	57, 59, 60, 62, 125, 130	Out	DS3 outputs are output signals used for different applications. All DS3 outputs should be left unconnected.

13. PHYSICAL CHARACTERISTICS

Table 41. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3	6.5	V
I_{OUT}	DC output current, per pin	All outputs except TX_SER_DATA+/-	-12	12	mA
I_{OUT}	DC output current, per pin	TX_SER_DATA+/-	-25	50	mA
T_{STG}	Storage temperature		-65	150	°C

Table 42. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature		-40	85	°C
t_R	Input rise time			10	ns
t_F	Input fall time			10	ns

Table 43. DC Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ITH}	High-level TTL input voltage	All TTL inputs except clocks	2.0			V
V_{ITL}	Low-level TTL input voltage	All TTL inputs except clocks			0.8	V
V_{ISH}	High-level Schmitt-triggered TTL input voltage	All TTL clock inputs			2.4	V
V_{ISL}	Low-level Schmitt-triggered TTL input voltage	All TTL clock inputs	0.6			V
V_{IHys}	Hysteresis Schmitt-triggered TTL input voltage	All TTL clock inputs	0.1			
V_{OCH1}	CMOS high-level output voltage	I_{OL} = -1 mA DC	V_{CC}=0.4			
V_{OCL1}	CMOS low-level output voltage	I_{OL} = 2 mA DC			0.4	
V_{OCH4}	CMOS high-level output voltage	I_{OH} = -8 mA DC TX_SER_DATA+/-	V_{CC}=0.4			V
V_{OCL4}	CMOS low-level output voltage	I_{OL} = 24 mA DC TX_SER_DATA+/-			0.4	V
I_{TYP}	Typical operating current	139.264 MHz, parallel 44.736 MHz, serial		215 180		mA mA

NOTES: • V_{CC}= 5 V ± 5%, T_A = -40° C to 85° C for industrial use.
• Typical values are T_A = 25° C and V_{CC} = 5 V.

Table 44. Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance			10	pF
C_{OUT}	Output capacitance			6	pF

NOTES: • Capacitance measured at 25° C.
• Sample tested only.

14. TIMING DIAGRAMS

All pin names are described in section "12. 3. Pin Descriptions" starting on page 72. Refer to Table A-1 on page 121 for PDH pin name prefix explanations. Unless otherwise indicated, all output timing delays assume a capacitive loading of 30 pF.

14. 1. Transmitter Timing

14. 1. 1. UTOPIA PHY Layer FIFO Input

The transmit UTOPIA PHY layer FIFO timing signals are compatible with the UTOPIA (refer to "Appendix B. References" on page 123) cell-by-cell specification. Table 45 indicates the transmit FIFO signal names and their corresponding UTOPIA designations.

Table 45. Transmit Signal Names and Corresponding UTOPIA Designations

Signal Name	UTOPIA Name
TPHY_DATA	TxData
TPHY_SOC	TxSOC
/TPHY_WRITE_EN	TxEnb*
TPHY_CLAV	TxFull*/TxClav
TPHY_CLK	TxClk
TO_FRAME	TxRef*
/TPHY_AEMPTY	Not Available
Not Available	TxPrty

Figure 32 and Figure 33 display the data input format for the internal transmit UTOPIA PHY layer FIFO. The parameter symbols used in Figure 32 and Figure 33 are defined in the table following Figure 33. Table 46 defines the contents of the TPHY_DATA bytes. The transmitter accepts data from the TPHY_DATA pins on the rising edge of TPHY_CLK only when /TPHY_WRITE_EN is asserted (low). The transmit UTOPIA PHY layer FIFO indicates that it has room to accept a full cell by asserting TPHY_CLAV. TPHY_CLAV will be deasserted (low) when the FIFO has accepted the 43rd payload data byte of the third cell. The clock cycles on which data is accepted are marked by an asterisk.

The start-of-cell marker, TPHY_SOC, is asserted when the first byte of the header is written into the FIFO. Under normal circumstances, the TPHY_SOC should be asserted once for every 53 bytes written into the FIFO. If more than 53 bytes are written into the FIFO before the next TPHY_SOC is asserted, the transmitter will ignore all bytes after the 53rd byte until the next TPHY_SOC. If a cell with fewer than 53 bytes (a runt cell) is written into the FIFO before the next TPHY_SOC is asserted, the transmitter will assume that the next TPHY_SOC is the start of a new cell, and discard the runt cell data.

The HEC fill byte is a dummy byte written into the FIFO and replaced by the transmitter with an HEC calculated for the first four header bytes. TPHY_DATA7 is the first bit transmitted in the serial data stream. TPHY_DATA0 is the last bit transmitted in the serial data stream.

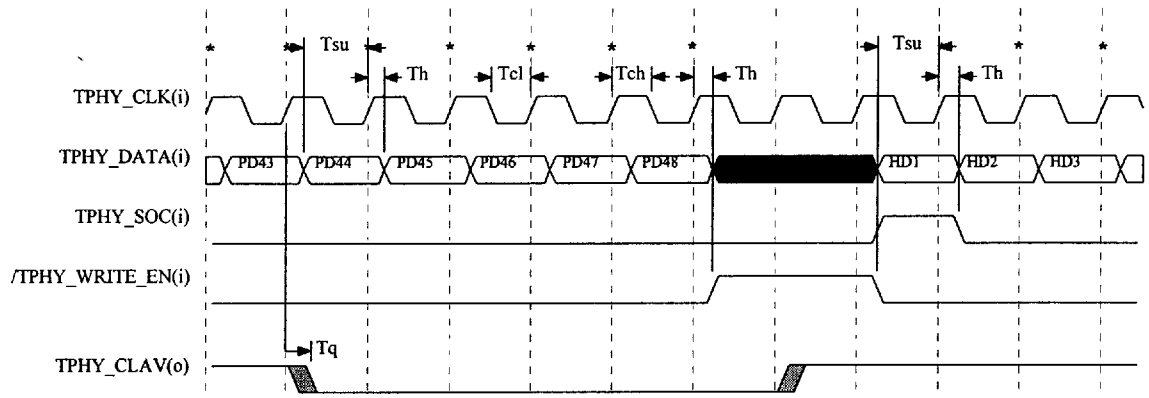

Figure 32. Transmit UTOPIA PHY Layer FIFO Timing

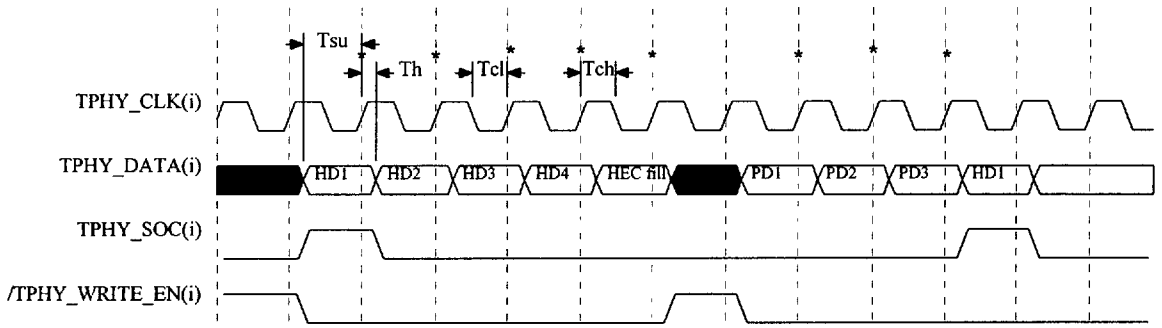

Figure 33. Transmit UTOPIA PHY Layer FIFO Timing with HEC Fill

Symbol	Parameter	Signals	Min	Max	Unit
Fc	TPHY_CLK frequency			25	MHz
Tch	TPHY_CLK high		18		ns
Tcl	TPHY_CLK low		18		ns
Th	TPHY_CLK hold time	TPHY_DATA, /TPHY_WRITE_EN, TPHY_SOC	1		ns
Tsu	TPHY_CLK setup time	TPHY_DATA, /TPHY_WRITE_EN, TPHY_SOC	8		ns
Tq	TPHY_CLK-to-output delay	TPHY_CLAV		19	ns

Table 46. Definitions of TPHY_DATA Byte Contents

Symbol	Definition	Symbol	Definition
HD1	1st header byte	HEC fill	HEC filler byte
HD2	2nd header byte	PD1	1st payload byte
HD3	3rd header byte	PD2	2nd payload byte
HD4	4th header byte	PD48	48th payload byte

14. 1. 2. Transmit PDH Parallel Timing

NOTE: The timing parameter symbols for all the diagrams in this section are presented in the table following Figure 37 on page 84.

Figure 34 displays the relationship between the parallel transmit input and output clocks. The nominal frequency of TX_PAR_CLK is 17.41 MHz for E4, and 4.30 MHz for E3.

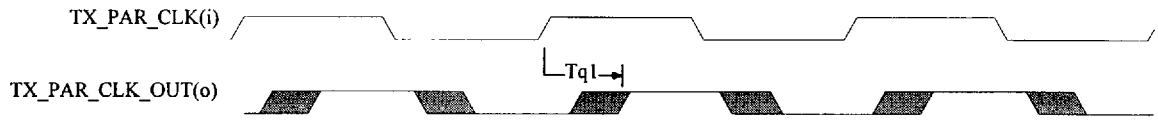

Figure 34. Transmit Parallel Clock Timing

Figure 35 presents the relationship between TO_FRAME and TX_PAR_DATA for the E3 and E4 format. The frame pulse, TO_FRAME, occurs once per frame (once every 2176 clock cycles for E4 and once every 537 clock cycles for E3) when the FA2 byte is present on TX_PAR_DATA. The TO_FRAME_IN signal can be used to synchronize the transmitter to an external event (for example, a frame pulse can be used to synchronize multiple transmitters to each other to multiplex the synchronized data to a faster rate.) The TO_FRAME_IN signal should be asserted one clock cycle before the FA1 byte is desired on TX_PAR_DATA. The TO_FRAME_IN signal needs to be asserted only once to synchronize the transmitter.

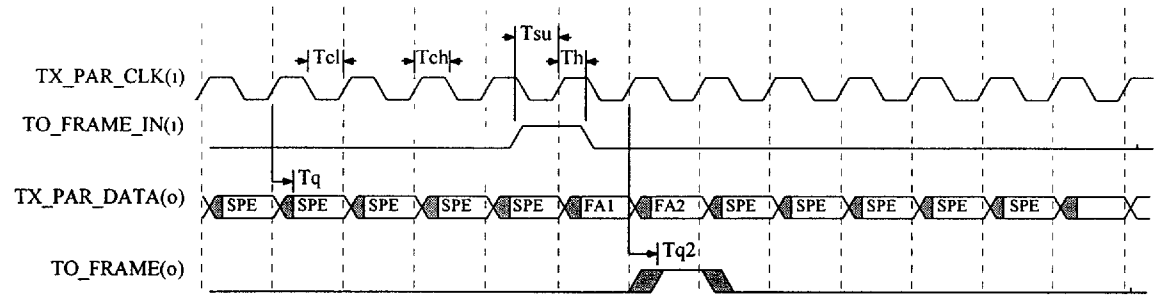

Figure 35. Transmit Parallel Timing for E3 and E4 Operation

Figure 36 shows that all the transmit alarm signals are sampled on the rising edge of TX_PAR_CLK. The transmit alarms include TX_AIS and TO_RDI. An alarm is transmitted while its associated pin is held high. The example in Figure 36 displays the assertion of an alarm for four clock cycles.

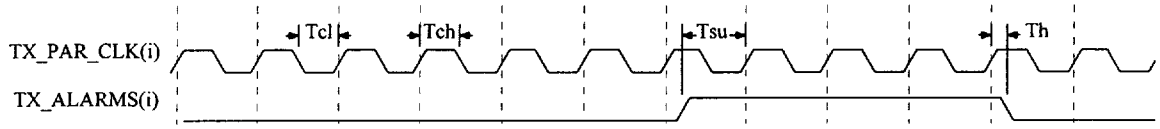

Figure 36. Transmit Alarm Timing

Figure 37 shows the relationship between TO_FRAME, TX_PAR_DATA, and the insertion data through the TO_EXT_IN and TO_INSERT signals. Bytes in the PDH data stream are overwritten only when TO_INSERT is asserted. The pulse on TO_INSERT shown in Figure 37, for example, overwrites the fourth and fifth SPE bytes of the current frame with the TO_EXT_IN data (EXT3 and EXT4). The frame pulse, TO_FRAME, occurs once per frame (once every 2176 clock cycles for E4 and once every 537 clock cycles for E3), and can be used to determine when to assert TO_INSERT to overwrite any particular byte of the PDH data stream. The frame pulse is asserted when the second SPE byte can be overwritten with the TO_EXT_IN signal. Note that if GFC_EN ($A=00_h$, D5) is a 1, then TO_EXT_IN(7:4) are used to overwrite GFC(3:0) of each cell header, and should not be used to overwrite the PDH data stream.

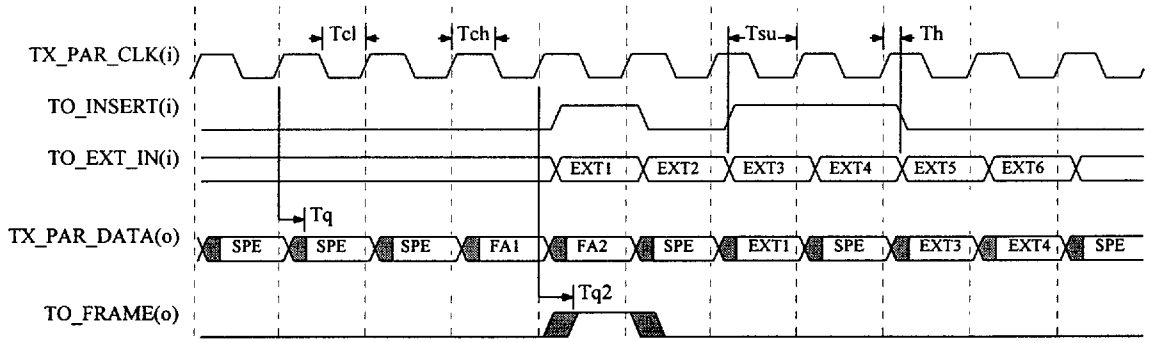

Figure 37. Transmit PDH Insertion Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	TX_PAR_CLK frequency			20	MHz
Tch	TX_PAR_CLK high		20		ns
Tcl	TX_PAR_CLK low		20		ns
Th	TX_PAR_CLK hold time	TX_AIS, TO_RDI, TO_FRAME_IN, TO_INSERT, TO_EXT_IN	1		ns
Tsu	TX_PAR_CLK setup time	TX_AIS, TO_RDI, TO_FRAME_IN, TO_INSERT, TO_EXT_IN	8		ns
Tq	TX_PAR_CLK-to-output delay	TX_PAR_DATA		23	ns
Tq1	TX_PAR_CLK-to-output delay	TX_PAR_CLK_OUT		17	ns
Tq2	TX_PAR_CLK-to-output delay	TO_FRAME, /TPHY_AEMPTY		28	ns

14. 1. 3. Transmit E3 Serial Timing

The serial outputs and the serial timing are used only for E3 operation. Serial timing and the relationship between serial and parallel timing are shown in Figure 38. When the transmitter is configured for serial timing through the SER_IO_EN signal, the parallel clock input, TX_PAR_CLK, is ignored. All parallel inputs and outputs must instead be associated with the parallel clock output signal, TX_PAR_CLK_OUT. All logical relationships displayed in section "14. 1. 2. Transmit PDH Parallel Timing" are still valid as long as TX_PAR_CLK is replaced with TX_PAR_CLK_OUT, and timing parameters Tsu, Th, Tq1, Tq, and Tq2 (refer to the table following Figure 37 on page 84) are replaced with timing parameters Tsu1, Th1, Tq4, Tq5, and Tq6.

NOTE: Do not switch dynamically between serial and parallel configurations.

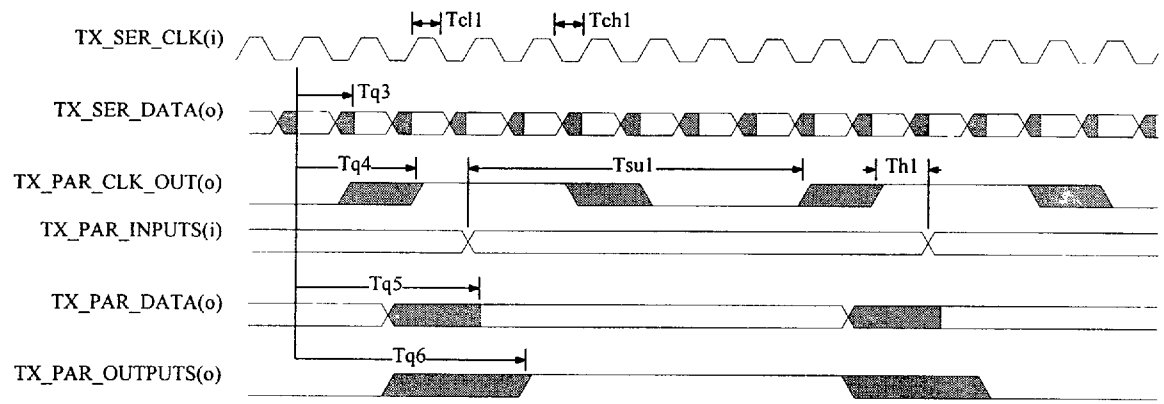

Figure 38. Transmit Serial Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	TX_SER_CLK frequency			35	MHz
Tch1	TX_SER_CLK high		11		ns
Tcl1	TX_SER_CLK low		11		ns
Th1	TX_PAR_CLK_OUT hold time	TX_AIS, TO_RDI, TO_FRAME_IN, TO_INSERT, TO_EXT_IN	0		ns
Tsu1	TX_PAR_CLK_OUT setup time	TX_AIS, TO_RDI, TO_FRAME_IN, TO_INSERT, TO_EXT_IN	31		ns
Tq3	TX_SER_CLK-to-output delay	TX_SER_DATA+, TX_SER_DATA-		16	ns
Tq4	TX_SER_CLK-to-output delay	TX_PAR_CLK_OUT		23	ns
Tq5	TX_SER_CLK-to-output delay	TX_PAR_DATA		28	ns
Tq6	TX_SER_CLK-to-output delay	TO_FRAME, /TPHY_AEMPTY		30	ns

14. 2. Receiver Timing

14. 2. 1. UTOPIA PHY Layer FIFO Output

The receive UTOPIA PHY layer FIFO timing signals are compatible with the UTOPIA cell-by-cell specification (refer to "Appendix B. References" on page 123). Table 47 indicates the receive FIFO signal names and their corresponding UTOPIA designations.

Table 47. Receive Signal Names and Corresponding UTOPIA Designations

Signal Name	UTOPIA Name
RPHY_DATA	RxData
RPHY_SOC	RxSOC
/RPHY_READ_EN	RxEnb*
RPHY_CLAV	RxEmpty*/RxClav
RPHY_CLK	RxClk
RO_FRAME	RxRef*
/RPHY_AEMPTY	Not Available
Not Available	RxPrty

The symbols used in Figure 39 are defined in the table following Figure 39. Table 48 defines the contents of the RPHY_DATA byte. Figure 39 shows the output format of the internal receive UTOPIA PHY layer FIFO data. The receiver presents new data on the rising edge of RPHY_CLK one clock cycle after /RPHY_READ_EN is asserted (low) and the receive FIFO has at least one cell. The deassertion of /RPHY_READ_EN will cause RPHY_DATA and RPHY_SOC to go into tristate. The RPHY_CLAV flag is deasserted (low) one clock cycle after the last data byte is presented at RPHY_DATA. The /RPHY_AEMPTY flag is asserted when fewer than 50 bytes are left in the FIFO. The start-of-cell marker, RPHY_SOC, is asserted when the first byte of the header is available on the RPHY_DATA pins. Under normal circumstances, the RPHY_SOC is asserted once for every 53 bytes read from the FIFO. RPHY_DATA7 is the first of the eight bits received in the serial data stream. RPHY_DATA0 is the last of the eight bits received in the serial data stream.

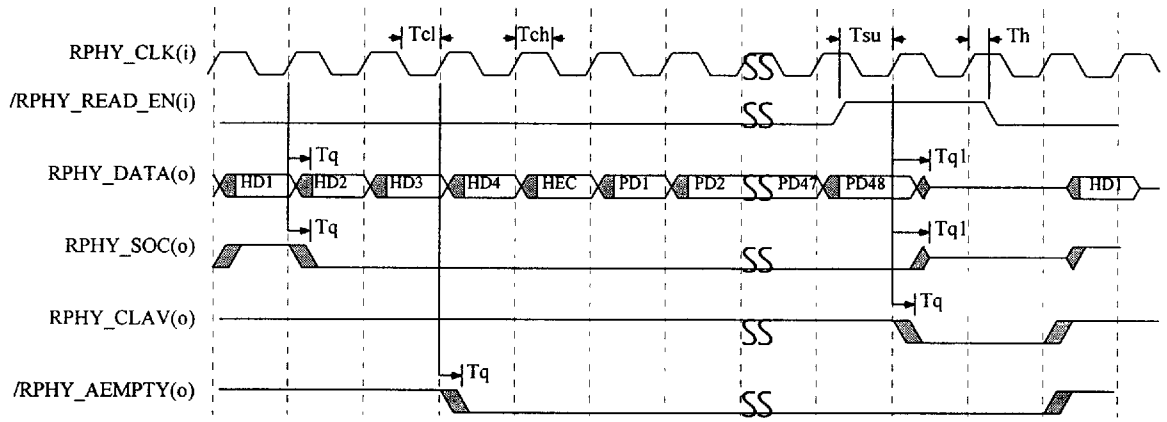

Figure 39. Receive UTOPIA PHY Layer FIFO Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	RPHY_CLK frequency			25	MHz
Tch	RPHY_CLK high		18		ns
Tcl	RPHY_CLK low		18		ns
Th	RPHY_CLK hold time	/RPHY_READ_EN	1		ns
Tsu	RPHY_CLK setup time	/RPHY_READ_EN	8		ns
Tq	RPHY_CLK-to-output delay	RPHY_DATA, RPHY_SOC, /RPHY_AEMPTY, RPHY_CLAV		19	ns
Tq1	RPHY_CLK-to-output enable delay	RPHY_DATA, RPHY_SOC		24	ns

Table 48. Definitions of RPHY_DATA Byte Contents

Symbol	Definition	Symbol	Definition
HD1	1st header byte	HEC	Corrected HEC byte
HD2	2nd header byte	PD1	1st payload byte
HD3	3rd header byte	PD2	2nd payload byte
HD4	4th header byte	PD48	48th payload byte

14. 2. 2. Receive PDH Parallel Timing

NOTE: The timing parameters for all the diagrams in this section are the same and are presented in the table following Figure 44 on page 89.

Figure 40 displays the delay between RX_PAR_CLK and RX_PAR_CLK_OUT, and the setup and hold requirements for RX_PAR_DATA. The nominal frequency for RX_PAR_CLK is 17.41 MHz for E4, and 4.30 MHz for E3. RX_PAR_DATA is the PDH serial data taken eight bits at a time. RX_PAR_DATA7 is the first of the eight bits in the serial data stream, and RX_PAR_DATA0 is the last of the eight bits in the serial data stream. *For E3 and E4, the 8-bit word does **not** need to be byte-aligned to the PDH frame.* The receiver detects E3 and E4 G.804 framing and byte-aligns the received data to the frame before processing it.

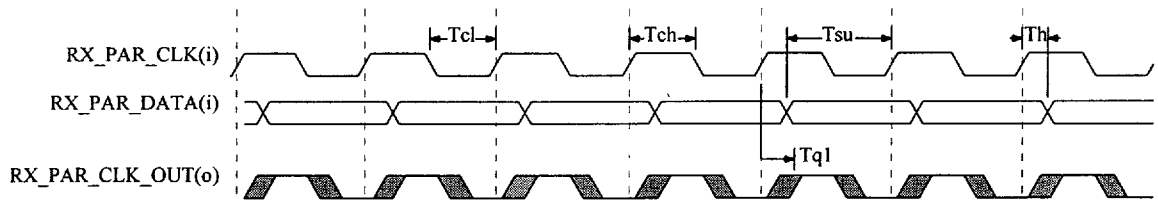

Figure 40. Receive Parallel Timing

The timing for the PDH alarms is shown in Figure 41. All alarms are active high and remain high for the duration of the event. The alarms detected by the receiver include RM_OCD, RO_RDI, RO_OOF, RO_LOF, and RX_AIS. The example in Figure 41 shows the detection of an alarm for four clock cycles.

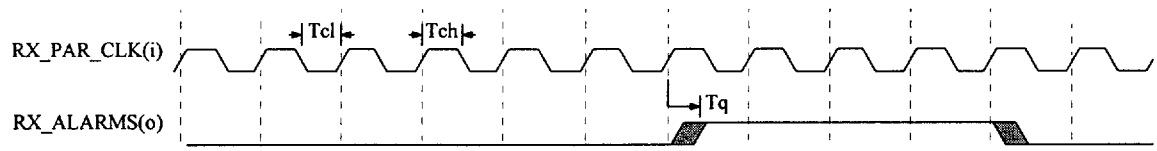

Figure 41. Receive Alarm Timing

Figure 42 shows the relationship for RO_EXT_OUT, RO_FRAME, and RO_EN for the parallel operation of E3 and E4. These signals can be used to determine the location of the overhead and SPE bytes of the PDH frame. (See Figure 28 on page 63 and Figure 29 on page 64 for details on E4 and E3 framing structures.) RO_FRAME is asserted for one clock cycle when valid frame words (FA1 and FA2) are detected. Typically, the RO_FRAME pulse occurs once per frame (once every 2176 clock cycles for E4 and once every 537 clock cycles for E3) and when RO_EXT_OUT contains the third SPE byte after the FA2 byte. RO_EN is an active high signal indicating that an overhead byte is present on RO_EXT_OUT. Note: if GFC_EN (A=00_h, D5) is a 1, then RO_EXT_OUT(7:4) are used to present the received GFC(3:0) of each cell header, and should not be used to extract the bytes within the PDH data stream.

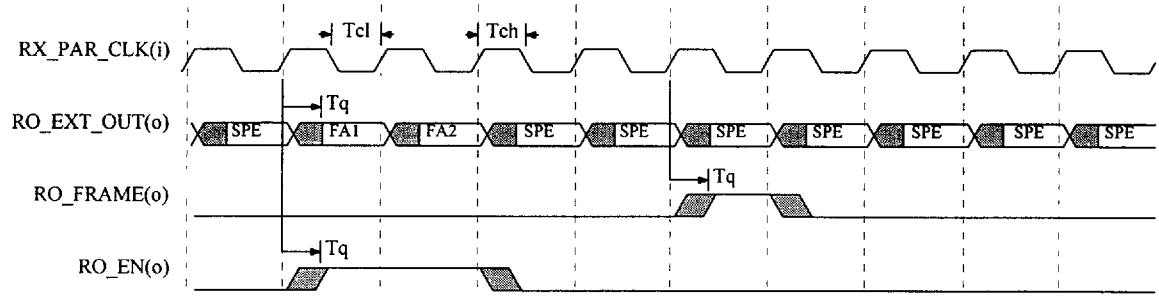

Figure 42. Receive External Timing

Figure 43 shows the relationship for RO_EXT_OUT, RO_EN, and RO_TR_EN for the parallel operation of E4. RO_TR_EN is an active high signal indicating that the Trail Trace byte is present on RO_EXT_OUT.

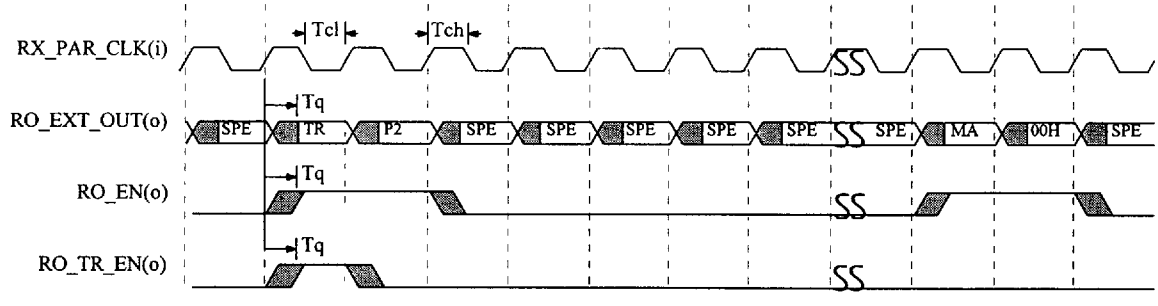

Figure 43. Receive External Timing for E4

Figure 44 shows the relationship for RO_EXT_OUT, RO_EN, and RO_TR_EN for the parallel operation of E3. RO_TR_EN is an active high signal indicating that the trail trace byte is present on RO_EXT_OUT.

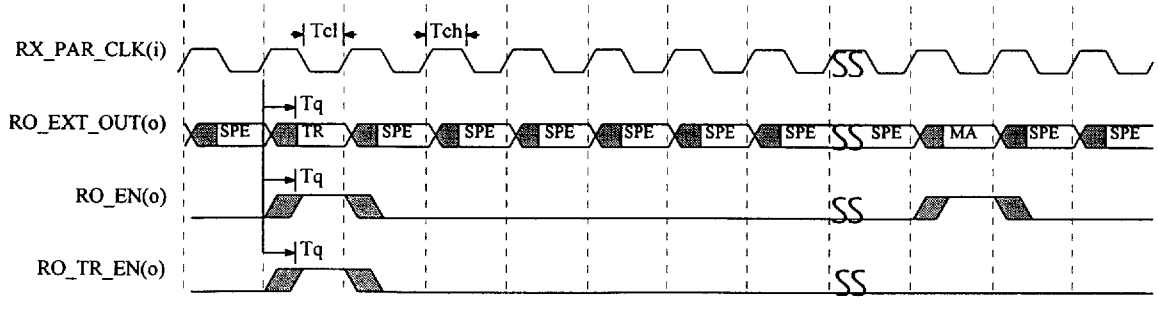

Figure 44. Receive External Timing for E3

Symbol	Parameter	Signals	Min	Max	Unit
Fc	RX_PAR_CLK frequency			20	MHz
Tch	RX_PAR_CLK high		20		ns
Tcl	RX_PAR_CLK low		20		ns
Th	RX_PAR_CLK hold time	RX_PAR_DATA	1		ns
Tsu	RX_PAR_CLK setup time	RX_PAR_DATA	8		ns
Tq	RX_PAR_CLK-to-output delay	RM_OCD, RO_RDI, RO_OOF, RO_LOF, RO_FRAME, RO_EN, RO_TR_EN, RX_AIS		28	ns
Tql	RX_PAR_CLK-to-output delay	RX_PAR_CLK_OUT		18	ns

14. 2. 3. Receive E3 Serial Timing

The serial inputs and the serial timing are used only for E3 operation. Serial timing and the relationship between serial and parallel timing are shown in Figure 45. When the receiver is configured for serial timing through the SER_IO_EN pin, the parallel clock input, RX_PAR_CLK, and the parallel data input, RX_PAR_DATA, are ignored. All parallel outputs must instead be associated with the parallel clock output signal, RX_PAR_CLK_OUT. All logical relationships displayed in section "14. 2. 2. Receive PDH Parallel Timing" are still valid as long as RX_PAR_CLK is replaced with RX_PAR_CLK_OUT, and timing parameter Tq and Tq1 are replaced with the timing parameters Tq4 and Tq3 shown in Figure 45.

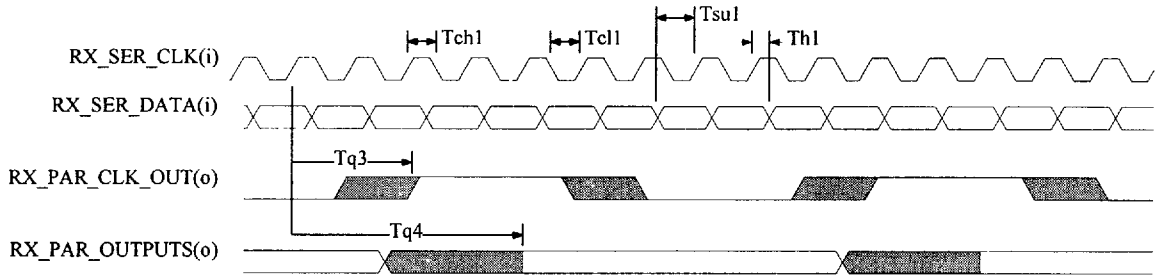

Figure 45. Receive Serial Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	RX_SER_CLK frequency			35	MHz
Tch1	RX_SER_CLK high		11		ns
Tcl1	RX_SER_CLK low		11		ns
Th1	RX_SER_CLK hold time	RX_SER_DATA	3		ns
Tsu1	RX_SER_CLK setup time	RX_SER_DATA	2		ns
Tq3	RX_SER_CLK-to-output delay	RX_PAR_CLK_OUT		23	ns
Tq4	RX_SER_CLK-to-output delay	RM_OCD, RO_RDI, RO_OOF, RO_LOF, RO_FRAME, RO_EN, RO_TR_EN, RX_AIS		33	ns

14. 3. Microprocessor Timing

Figure 46 displays the timing for typical microprocessor read/write cycles without the use of ADDR_LAT_EN. In the example below, the read cycle precedes the write cycle. The setup, hold, and delay times are given with respect to several signals (/CS, /RD, and /WR). Parameter times are determined by the relationships of the various signals as shown in the table following Figure 47. For example, the Tdsu parameter definition is "data setup time prior to /CS or /WR, whichever comes first". This definition indicates that the data, D, must be valid *Tdsu* nanoseconds before /CS or /WR, whichever comes first. In the write cycle example below, since /WR is deasserted before /CS, the data must be valid *Tdsu* nanoseconds before the /WR signal, and has no minimum setup time with respect to the /CS signal.

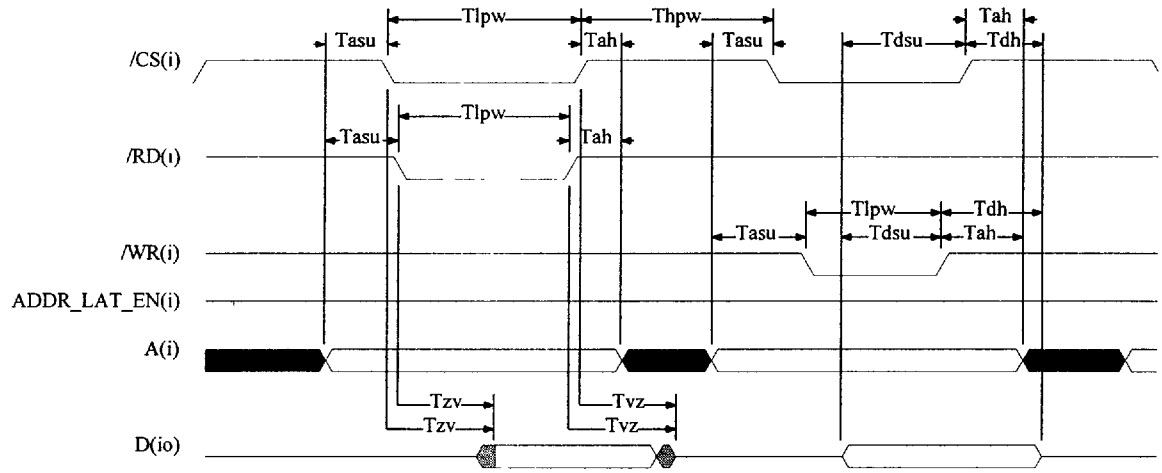

Figure 46. Microprocessor Read and Write Cycle Timing

Figure 47 displays the timing for typical microprocessor read/write cycles with the use of ADDR_LAT_EN. In the example below, the read cycle precedes the write cycle.

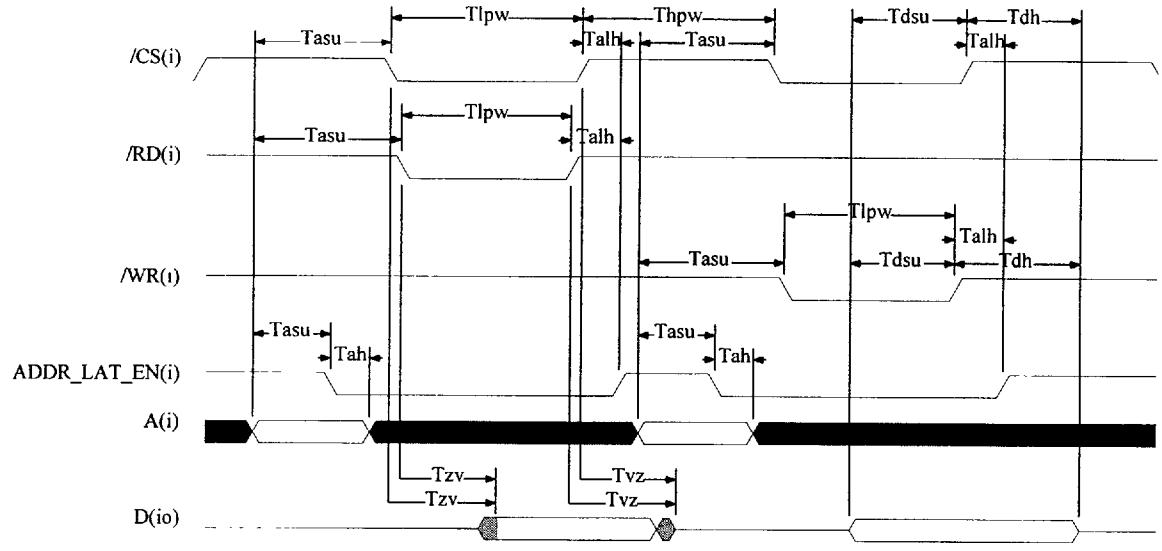

Figure 47. Microprocessor Read and Write Cycle Timing with ADDR_LAT_EN

Symbol	Parameter	Signals	Min	Max	Unit
Tasu	address setup time prior to /CS, /RD, /WR, or ADDR_LAT_EN, whichever comes last	A	12		ns
Tah	address hold time prior to /CS, /RD, /WR, or ADDR_LAT_EN, whichever comes first	A	2		ns
Talh	address latch hold time prior to /CS, /RD, or /WR, whichever comes first	ADDR_LAT_EN	0		ns
Tdsu	data setup time prior to /CS or /WR, whichever comes first	D	12		ns
Tdh	data hold time prior to /CS or /WR, whichever comes first	D	0		ns
Tzv	data valid after /CS or /RD, whichever comes last	D		28	ns
Tvz	data tristate after /CS or /RD, whichever comes first	D	2	23	ns
Tlpw	low pulse width	/CS, /RD, /WR	11		
Thpw	high pulse width	/CS, /RD, /WR	23		

Figure 48 displays the interrupt timing constraints. The interrupt is asserted asynchronously with respect to the / RD and /CS signals when a non-masked interrupt occurs. The interrupt is cleared when the interrupt register ($2D_h$ or $2E_h$) containing the active interrupt is read, assuming that no additional interrupts are generated during the read cycle. If interrupts occurred in both $2D_h$ and $2E_h$, both registers must be read to clear the interrupt line.

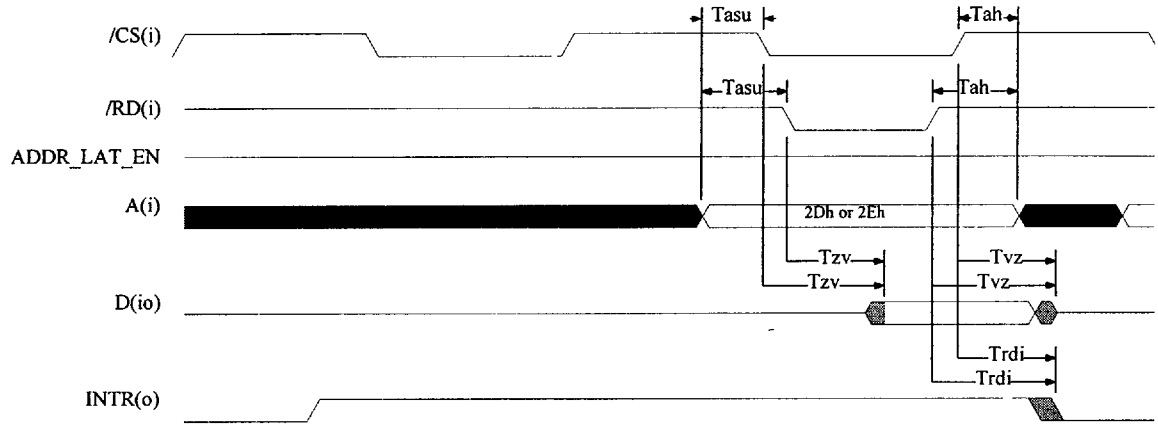

Figure 48. Interrupt Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tasu	address setup to /CS, /RD, or /WR, whichever comes last	A	12		ns
Tah	address hold to /CS, /RD, or /WR, whichever comes first	A	2		ns
Trdi	interrupt cleared after /CS or /RD, whichever comes first	INTR		23	ns
Tzv	data valid after /CS or /RD, whichever comes last	D		28	ns
Tvz	data tristate after /CS or /RD, whichever comes first	D	2	23	ns

14. 4. Miscellaneous Timing

Figure 49 displays the reset pin timing. The /RESET signal must be asserted for a minimum time (Tres) to be registered properly. The WAC-034-B remains in reset while /RESET is asserted, and starts performing normally within three to seven transmit parallel/receive parallel clock cycles after the reset is removed. Since the reset is synchronous, the reset time for E3 is four times longer than the reset time for E4.

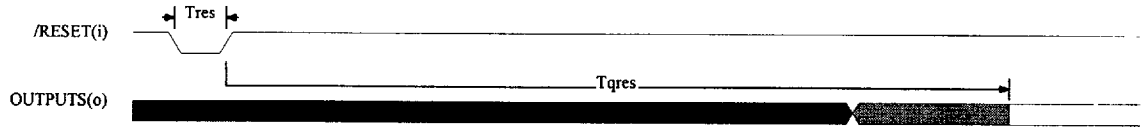

Figure 49. Reset Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tres	minimum reset pulse	/RESET	20		ns
Tqres	reset deasserted to normal operation	all outputs	3	7	clock cycles

All outputs of the chip are tristated when OUTPUT_EN is deasserted. The output enable timing is displayed in Figure 50.

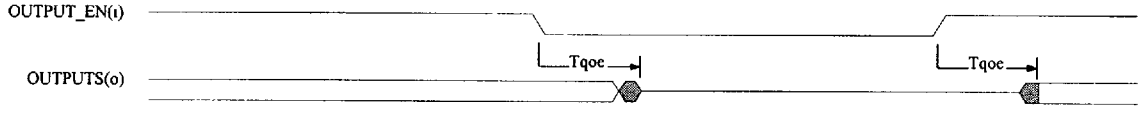

Figure 50. Output Enable Timing

Symbol	Parameter	Signals	Min	Max	Unit
Tqoe	output enable	all outputs		28	ns

The timing for the JTAG port is shown in Figure 51. The /SCAN_TRSTN signal is asynchronous to SCAN_TCK.

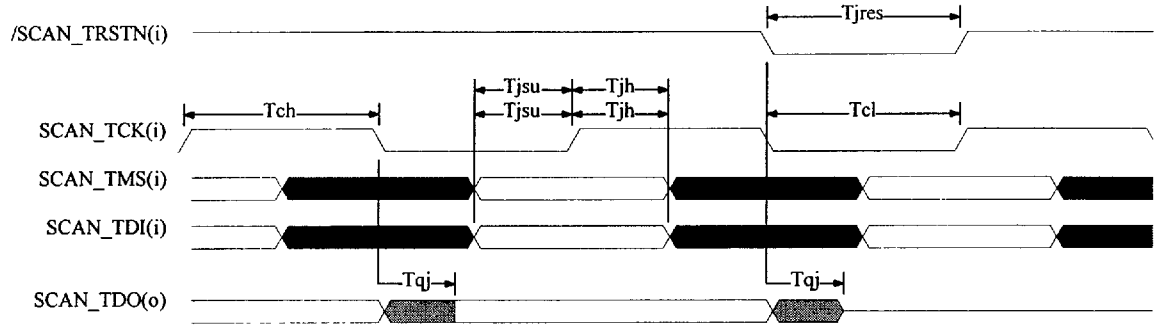

Figure 51. JTAG Timing

Symbol	Parameter	Signals	Min	Max	Unit
Fc	SCAN_TCK frequency			5	MHz
Tch	SCAN_TCK high		80		ns
Tcl	SCAN_TCK low		80		ns
Tjh	SCAN_TCK hold time	SCAN_TMS, SCAN_TDI	40		ns
Tjres	/SCAN_TRSTN low		80		ns
Tjsu	SCAN_TCK setup time	SCAN_TMS, SCAN_TDI	40		ns
Tqj	SCAN_TCK-to-output delay /SCAN_TRSTN-to-output delay	SCAN_TDO	2	40	ns

15. BOUNDARY SCAN

Table 49 lists the boundary scan instructions and instruction codes supported by the WAC-034-B. Bit 3 is the most significant bit and should be the first bit shifted into SCAN_TMS. Bit 0 is the least significant bit and should be the last bit shifted into SCAN_TMS.

Table 49. Boundary Scan Instructions Codes

Instruction Name	Instruction Code, IR(3:0)
EXTEST	0000
INTEST (not supported)	0001
SAMPLE	0010
SAMPLE	0011
BYPASS	0100
BYPASS	0101
BYPASS	0110
BYPASS	0111
BYPASS	1000
BYPASS	1001
BYPASS	1010
BYPASS	1011
BYPASS	1100
BYPASS	1101
BYPASS	1110
BYPASS	1111

Table 50 shows the boundary scan registers and the order in which they will be shifted out on SCAN_TDO.

Table 50. Boundary Scan Registers

Pin/Enable Name	Bit #	Type
/CS	117	in
/RD	116	in
/WR	115	in
A(0:5)	114:109	in
D0	108	in
D0	107	out
D1	106	in
D1	105	out
D2	104	in
D2	103	out
D3	102	in
D3	101	out
D4	100	in
D4	99	out
D5	98	in
D5	97	out
D6	96	in
D6	95	out
D7	94	in
D7	93	out
/D_OE	92	internal
INTR	91	out
/RESET	90	in
/SCAN_OUTPUT_EN	89	internal
OUTPUT_EN	88	in
RPHY_DATA(0:7)	87:80	out
/RPHY_READ_EN	79	in
RPHY_CLK	78	in
RPHY_SOC	77	out
RPHY_CLAV	76	out
/RPHY_AEMPTY	75	out
RO_TR_EN	74	out
RO_EXT_OUT(0:7)	73:66	out
/RO_EXT_OUT_OE	65	internal
RM_OCD	64	out
DS3 OUT	63	out
/TPHY_AEMPTY	62	out
DS3 OUT	61	out
DS3 OUT	60	out
RO_EN	59	out
DS3 OUT	58	out
RO_RDI	57	out
RX_AIS	56	out
RX_LOS	55	out
RO_OOF	54	out
RO_LOF	53	out
RO_FRAME	52	out
RX_PAR_CLK_OUT	51	out
SER_IO_EN	50	in
RX_PAR_DATA(0:7)	49:42	in
RX_PAR_CLK	41	in
TX_AIS	40	in
TX_PAR_CLK	39	in
TX_PAR_DATA(0:7)	38:31	out
TX_PAR_CLK_OUT	30	out
TO_FRAME	29	out
TO_FRAME_IN	28	in
TO_INSERT	27	in
TO_EXT_IN(0:7)	26:19	in
/TO_EXT_IN_OE	18	internal
DS3 IN	17	in
DS3 OUT	16	out
TO_RDI	15	in
ADDR_LAT_EN	14	in
DS3 OUT	13	out
/TPHY_WRITE_EN	12	in
TPHY_SOC	11	in
TPHY_CLK	10	in
TPHY_DATA(0:7)	9:2	in
DS3 IN	1	in
TPHY_CLAV	0	out

The output enable controls are as follows: Under normal operation, all outputs are tristated by the OUTPUT_EN pin being set to 0. For the INTEST and EXTEST operations, there are four separate active low output enables: /D_OE enables D(7:0), /RO_EXT_OUT_OE enables RO_EXT_OUT(7:0), /TO_EXT_IN_OE enables TO_EXT_IN(7:0), and /SCAN_OUTPUT_EN enables the rest of the outputs.

NOTE: /TO_EXT_IN_OE is used for production testing and should always be deasserted (set to a 1) during scan testing.

16. MICROPROCESSOR PORTS

16. 1. Write Ports Summary

NOTE: The external /RESET signal, when asserted, sets all microprocessor write ports to a default state. The default state is 0 unless otherwise shown.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
GEN_W1	00_h	0	0	GFC_EN	HDB3_DIS	BIPOLAR_ DIS	RATE(1:0)		LOC_LOOP_ ON
TX_W1	01_h	0	0	0	0	0	0	0	TX_RESET
TX_W2	02_h	0	0	0	0	0	0	TX_BPV_ INS_ONCE	TX_LOS_ INS
TX_CNTR_W1	03_h	0	0	0	0	0	0	0	TX_CNTR_ LATCH
TM_W1	04_h	0	0	0	TM_HEC_ DIS	TM_ SCRAM_DIS [Default = 1]	TM_COSET_ DIS	TM_HEC_ INV_CONT	TM_HEC_ INV_ONCE
TM_W2	05_h	TM_HEC_INV_MASK(7:0)							
TM_W3	06_h	TM_NULL_HDI(7:0)							
TM_W4	07_h	TM_NULL_HD2(7:0)							
TM_W5	08_h	TM_NULL_HD3(7:0)							
TM_W6	09_h	TM_NULL_HD4(7:0)							
TM_W7	$0A_h$	TM_NULL_PAYLOAD(7:4) GFC_MASK(3:0)				TM_NULL_PAYLOAD(3:0)			
TO_W1	$0B_h$	0	0	0	TO_AIS_EN	0	TO_OVH_ DIS	0	0
TO_W2	$0C_h$	TO_ TIMARK	TO_RDI_ INS	TO_PAYDEP(1:0)		TO_ UNEQUIP	TO_FERR_ INS	TO_EM_ INV_CONT	TO_EM_ INV_ONCE
TO_W3	$0D_h$	TO_TRAIL_TRACE1(7:0)							
TO_W4	$0E_h$	TO_TRAIL_TRACE2(7:0)							
TO_W5	$0F_h$	TO_TRAIL_TRACE3(7:0)							
TO_W6	10_h	TO_TRAIL_TRACE4(7:0)							
TO_W7	11_h	TO_TRAIL_TRACE5(7:0)							
TO_W8	12_h	TO_TRAIL_TRACE6(7:0)							
TO_W9	13_h	TO_TRAIL_TRACE7(7:0)							
TO_W10	14_h	TO_TRAIL_TRACE8(7:0)							
TO_W11	15_h	TO_TRAIL_TRACE9(7:0)							
TO_W12	16_h	TO_TRAIL_TRACE10(7:0)							
TO_W13	17_h	TO_TRAIL_TRACE11(7:0)							
TO_W14	18_h	TO_TRAIL_TRACE12(7:0)							
TO_W15	19_h	TO_TRAIL_TRACE13(7:0)							
TO_W16	$1A_h$	TO_TRAIL_TRACE14(7:0)							
TO_W17	$1B_h$	TO_TRAIL_TRACE15(7:0)							
TO_W18	$1C_h$	TO_TRAIL_TRACE16(7:0)							
RX_W1	24_h	0	0	0	0	0	0	0	RX_RESET
RX_W2	25_h	0	0	0	0	0	0	0	RX_EXZ_ DIS
RX_CNTR_W1	26_h	0	0	0	RX_CNTR_LATCH_SEL(3:0)				RX_CNTR_ LATCH

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RM_W1	27_h	0	RM_HEC_ CORRECT_ DIS [Default = 1]	0	RM_PASS_ OCD	RM_PASS_ UNASSIGNED	RM_PASS_ BAD_HEC	RM_ DESCRAM_ DIS [Default = 1]	RM_ COSET_DIS
RO_W1	28_h	0	0	0	0	RO_BLOCK_ CNT_EN	RO_OVH_ DIS	0	RO_OOF_ INS
INTR_MASK_W1	$2A_h$	RO_LOF_ MASK	RO_OOF_ MASK	RM_OCD_ MASK	RM_FIFO_ OVERFLOW_ MASK	RO_PAYTYP_ MISMATCH_ MASK	RO_RDI_ MASK	RO_ TIMARK_ MASK	RO_AIS_ MASK
INTR_MASK_W2	$2B_h$	0	0	0	0	0	RO_CRC7_ VAL_MASK	RO_CRC7_ CHG_MAS K	RX_LOS_ MASK
TEST_W1	$2E_h$	TEST(7:0)							
TEST_W2	$2F_h$	TEST(15:8)							

16. 2. Read Ports Summary

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_CNTR_R1	03_h								TX_CNTR_ LATCH
RO_R1	$0D_h$	RO_TRAIL_TRACE1(7:0)							
RO_R2	$0E_h$	RO_TRAIL_TRACE2(7:0)							
RO_R3	$0F_h$	RO_TRAIL_TRACE3(7:0)							
RO_R4	10_h	RO_TRAIL_TRACE4(7:0)							
RO_R5	11_h	RO_TRAIL_TRACE5(7:0)							
RO_R6	12_h	RO_TRAIL_TRACE6(7:0)							
RO_R7	13_h	RO_TRAIL_TRACE7(7:0)							
RO_R8	14_h	RO_TRAIL_TRACE8(7:0)							
RO_R9	15_h	RO_TRAIL_TRACE9(7.0)							
RO_R10	16_h	RO_TRAIL_TRACE10(7:0)							
RO_R11	17_h	RO_TRAIL_TRACE11(7:0)							
RO_R12	18_h	RO_TRAIL_TRACE12(7:0)							
RO_R13	19_h	RO_TRAIL_TRACE13(7:0)							
RO_R14	$1A_h$	RO_TRAIL_TRACE14(7:0)							
RO_R15	$1B_h$	RO_TRAIL_TRACE15(7:0)							
RO_R16	$1C_h$	RO_TRAIL_TRACE16(7:0)							
RO_R17	$1D_h$							RO_PAYDEP(1:0)	
RX_CNTR_R1	26_h								RX_CNTR_ LATCH
TX_CNTR_R2	27_h	TX_LATCHED_COUNT(7:0)							
TX_CNTR_R3	28_h	TX_LATCHED_COUNT(15:8)							
RX_CNTR_R2	29_h	RX_LATCHED_COUNT(7:0)							
RX_CNTR_R3	$2A_h$	RX_LATCHED_COUNT(15:8)							
INTR_R1	$2D_h$	RO_LOF_ INTR	RO_OOF_ INTR	RM_OCD_ INTR	RM_FIFO_ OVERFLOW_ INTR	RO_PAYTYP_ MISMATCH_ INTR	RO_RDI_ INTR	RO_TIMARK_ INTR	RO_AIS_ INTR
INTR_R2	$2E_h$						RO_CRC7_ VAL_INTR	RO_CRC7_CH G_INTR	RX_LOS_ INTR
STATUS_R1	$2F_h$	RO_LOF	RO_OOF	RM_OCD	RM_FIFO_ OVERFLOW	RO_PAYTYP_ MISMATCH	RO_RDI	RO_TIMARK	RO_AIS
STATUS_R2	30_h						RO_CRC7_ VAL		RX_LOS
HW_REV_R1	$3F_h$	0	0	0	0	0	0	0	0

16. 3. Write Ports

NOTES:

- The external /RESET signal, when asserted, sets all microprocessor write ports to a default state. The default state is 0 unless otherwise shown.
- All port bits marked "Not used" must be written with the value 0 to maintain software compatibility with future versions.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
GEN_W1	00_h	0	0	GFC_EN	HDB3_DIS	BIPOLAR _DIS	RATE(1:0)		LOC_ LOOP_ON

D(7:6) Write with a 0 to maintain compatibility with future software versions.

D5 GFC_EN

1 - Enables the insertion of GFC bits in the transmit data stream via TO_EXT_IN(7:4), and the reporting of GFC bits from the receive data stream via RO_EXT_OUT(7:4).

0 - Disables the insertion of GFC bits in the transmit data stream through TO_EXT_IN(7:4), and the reporting of GFC bits from the receive data stream through RO_EXT_OUT(7:4).

NOTE: GFC bits are only inserted if the corresponding GFC_MASK (Addr=$0A_h$, D7-D4) bit is a 1.

D4 HDB3_DIS

1 - Enables alternate mark inversion (AMI) for serial input and output.

0 - Enables HDB3 encoding and decoding for serial input and output.

D3 BIPOLAR_DIS

1 - Transmission and reception at the serial input and output is dependent upon the positive signal only.

0 - Enables bipolar transmission and reception at the serial input and output.

D(2:1) RATE

00 - Sets the framing format to DS3.

01 - Sets the framing format to E3.

10 - Sets the framing format to E4.

11 - Not used.

D0 LOC_LOOP_ON

1 - Enables the Local Loop.

0 - Disables the Local Loop.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_W1	01_h	0	0	0	0	0	0	0	TX_RESET

D(7:1) Write with a 0 to maintain compatibility with future software versions.

D0 TX_RESET

NOTE: The transmitter enters the reset state when a 1 is written to this location, and remains in the reset state until a 0 is written to this location.

1 - Resets the transmitter.

0 - Allows the transmitter to resume normal operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_W2	02_h	0	0	0	0	0	0	TX_BPV_INS_ONCE	TX_LOS_INS

D(7:2) Write with a 0 to maintain compatibility with future software versions.

D1 TX_BPV_INS_ONCE

A rising edge on this bit will force the HDB3 encoder to insert one BPV without causing a false HDB3 sequence. After TX_BPV_INS_ONCE has been latched, additional pulsing of TX_BPV_INS_ONCE will be ignored until the BPV is inserted. To produce a rising edge, write a 0 followed by a 1 to this port bit location.

D0 TX_LOS_INS

1 - Forces TX_SER_DATA to 0 and TX_PAR_DATA to 00_h.

0 - Allows normal transmission.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_CNTR_W1	03_h	0	0	0	0	0	0	0	TX_CNTR_LATCH

D(7:1) Write with a 0 to maintain compatibility with future software versions.

D0 TX_CNTR_LATCH

NOTE: The latch operation can be verified by ensuring that the TX_CNTR_LATCH bit in the TX_CNTR_R1 register is a 0.

1 - Initiates the latch and clear operation for the transmit message cell counter.

0 - Normal operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TM_W1	04_h	0	0	0	TM_HEC_DIS	TM_SCRAM_DIS [Default=1]	TM_COSET_DIS	TM_HEC_INV_CONT	TM_HEC_INV_ONCE

D(7:5) Write with a 0 to maintain compatibility with future software versions.

D4 TM_HEC_DIS

1 - Disables HEC insertion.

NOTE: For null cells, the TM_NULL_PAYLOAD pattern is transmitted in the HEC location.

0 - Enables calculation and insertion of HEC in the fifth header byte.

D3 TM_SCRAM_DIS

1 - Disables the cell payload scrambling.

0 - Enables the cell payload scrambling.

D2 TM_COSET_DIS

1 - Disables the addition of the coset (55_h) to the HEC.

0 - Enables the addition of the coset (55_h) to the HEC.

D1 TM_HEC_INV_CONT

1 - Enables inversion of the HEC bits in accordance with the TM_HEC_INV_MASK bits.

0 - Disables inversion of the HEC bits.

D0 TM_HEC_INV_ONCE

A rising edge on this bit inverts the next HEC in accordance with the TM_HEC_INV_MASK bits. This control bit does not affect transmission if TM_HEC_INV_CONT is asserted. To produce a rising edge, write a 0 followed by a 1 to this port bit location.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TM_W2	05_h	TM_HEC_INV_MASK(7:0)							

D(7:0) TM_HEC_INV_MASK

A 1 in a bit location indicates that the associated HEC bit is to be inverted when TM_HEC_INV_CONT is asserted, or when a rising edge is detected on TM_HEC_INV_ONCE.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TM_W3	06_h	TM_NULL_HD1(7:0)							
TM_W4	07_h	TM_NULL_HD2(7:0)							
TM_W5	08_h	TM_NULL_HD3(7:0)							
TM_W6	09_h	TM_NULL_HD4(7:0)							
TM_W7	$0A_h$	TM_NULL_PAYLOAD(7:4) GFC_MASK(3:0)				TM_NULL_PAYLOAD(3:0)			

D(7:0) TM_NULL_HD1

The first header byte of the null cell. D7 is the first bit to be transmitted in the serial data stream.

D(7:0) TM_NULL_HD2

The second header byte of the null cell. D7 is the first bit to be transmitted in the serial data stream.

D(7:0) TM_NULL_HD3

The third header byte of the null cell. D7 is the first bit to be transmitted in the serial data stream.

D(7:0) TM_NULL_HD4

The fourth header byte of the null cell. D7 is the first bit to be transmitted in the serial data stream.

D(7:0) TM_NULL_PAYLOAD/GFC_MASK

The pattern that is transmitted in the entire 48-byte payload of the null cell. This pattern is also transmitted as the HEC byte of the null cell when TM_HEC_DIS is asserted. D7 is the first bit to be transmitted in the serial data stream.

When GFC_EN (Addr=00_h, D5) is a 1, the upper nibble of this register is also used to determine which of the TO_EXT_IN pins will overwrite the GFC bits of outgoing cells. If D7 is a 1, then TO_EXT_IN7 will overwrite GFC3. If D6 is a 1, then TO_EXT_IN6 will overwrite GFC2. If D5 is a 1, then TO_EXT_IN5 will overwrite GFC1. If D4 is a 1, then TO_EXT_IN4 will overwrite GFC0.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TO_W1	$0B_h$	0	0	0	TO_AIS_EN	0	TO_OVH_DIS	0	0

D7 Write with a 0 to maintain compatibility with future software versions.

D4 TO_AIS_EN
- 1 - Enables AIS transmission.
- 0 - Disables AIS transmission.

When transmitting AIS, the WAC-034-B will continue reading from the transmit ATM FIFO, thus causing the ATM FIFO data to be lost. However, the transmit message counter will not increment.

D3 Write with a 0 to maintain compatibility with future software versions.

D2 TO_OVH_DIS
- 1 - Allows access of ATM cells without overhead processing through TX_PAR_DATA.
- 0 - Allows transmission of E3 or E4 framed cells.

D(1:0) Write with a 0 to maintain compatibility with future software versions.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TO_W2	$0C_h$	TO_ TIMARK	TO_PAYDEP(1:0)		TO_UNEQIP	TO_RDI_INS	TO_FERR_ INS	TO_EM_ INV_CONT	TO_EM_ INV_ONCE

D7 TO_TIMARK
- 1 - Sets the timing marker bit of the MA byte for transmission.
- 0 - Resets the timing marker bit of the MA byte for transmission.

D(6:5) TO_PAYDEP
- 1 - Sets the payload dependent bits of the MA byte for transmission.
- 0 - Resets the payload dependent bits of the MA byte for transmission.

D4 TO_UNEQUIP
- 1 - Enables transmission of the unequipped signal label code (XX000XXX) in the MA byte.
- 0 - Enables transmission of the ATM signal label code (XX010XXX) in the MA byte.

D3 TO_RDI_INS
- 1 - Sets the RDI bit of the MA byte for transmission.
- 0 - Resets the RDI bit of the MA byte for transmission.

D2 TO_FERR_INS
- 1 - Inverts the first bit of the FA1 and FA2 bytes before transmission.
- 0 - Transmits normal FA1 and FA2 bytes.

D1 TO_EM_INV_CONT
- 1 - Inverts the EM value before transmission.
- 0 - Transmits the normal EM value.

D0 TO_EM_INV_ONCE

A rising edge on this bit inverts the next EM value to be transmitted. This control bit does not affect transmission if TO_EM_INV_CONT is asserted.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TO_W3	$0D_h$	TO_TRAIL_TRACE1(7:0)							
TO_W4	$0E_h$	TO_TRAIL_TRACE2(7:0)							
TO_W5	$0F_h$	TO_TRAIL_TRACE3(7:0)							
TO_W6	10_h	TO_TRAIL_TRACE4(7:0)							
TO_W7	11_h	TO_TRAIL_TRACE5(7:0)							
TO_W8	12_h	TO_TRAIL_TRACE6(7:0)							
TO_W9	13_h	TO_TRAIL_TRACE7(7:0)							
TO_W10	14_h	TO_TRAIL_TRACE8(7:0)							
TO_W11	15_h	TO_TRAIL_TRACE9(7:0)							
TO_W12	16_h	TO_TRAIL_TRACE10(7:0)							
TO_W13	17_h	TO_TRAIL_TRACE11(7:0)							
TO_W14	18_h	TO_TRAIL_TRACE12(7:0)							
TO_W15	19_h	TO_TRAIL_TRACE13(7:0)							
TO_W16	$1A_h$	TO_TRAIL_TRACE14(7:0)							
TO_W17	$1B_h$	TO_TRAIL_TRACE15(7:0)							
TO_W18	$1C_h$	TO_TRAIL_TRACE16(7:0)							

D(7:0) TO_W3 through TO_W18

Contain the contents of the 16-byte transmit trail trace message. D7 of each byte is the first bit to be transmitted in the serial data stream.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_W1	24_h	0	0	0	0	0	0	0	RX_RESET

D(7:1) Write with a 0 to maintain compatibility with future software versions.

D0 RX_RESET

NOTE: The receiver enters the reset state when a 1 is written to this location, and remains in the reset state until a 0 is written to this location.

1 - Resets the receiver.

0 - Allows the receiver to resume normal operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_W2	25_h	0	0	0	0	0	0	0	RX_EXZ_DIS

D(7:1) Write with a 0 to maintain compatibility with future software versions.

D0 RX_EXZ_DIS

1 - Configures the HDB3 decoder to ignore the occurrence of four or more consecutive 0s.

0 - Configures the HDB3 decoder to count four or more consecutive 0s as a line code violation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_CNTR_W1	26_h	0	0	0	RX_CNTR_LATCH_SEL(3:0)				RX_CNTR_LATCH

D(7:5) Write with a 0 to maintain compatibility with future software versions.

D(4:1) RX_CNTR_LATCH_SEL

Selects the counter to be latched.

0000 - Message received counter. Counts complete cells written to the receive ATM FIFO. This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_AIS, RM_OCD.

0001 - Incorrect HEC counter. Counts headers with uncorrectable HECs when the ATM cell header processing is in Correction Mode. Also counts all headers with incorrect HECs when the ATM cell header processing is in Detection Mode. The chip automatically selects Correction or Detection Mode in accordance with the ATM Forum's UNI specification. This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_AIS, RM_OCD.

0010 - BIP-8 (EM) error counter. Counts all BIP errors per byte as a single error when RO_BLOCK_CNT_EN is set to 1 and individually counts each BIP error per byte when RO_BLOCK_CNT_EN is set to 0. This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_AIS.

0011 - FEBE counter. Individually counts each FEBE per byte. This counter is disabled by the following alarms: RX_LOS, RO_LOF, RX_AIS.

0100 - Not used.

0101 - Not used.

0110 - Not used.

0111 - Not used.

1000 - Not used.

1001 - Line code violation counter. Counts all BPVs and excess 0s unless RX_EXZ_DIS is set to 1. This counter is disabled by RX_LOS.

1010 - 1111 Not used.

D0 RX_CNTR_LATCH

NOTE: The latch operation can be verified by ensuring that the RX_CNTR_LATCH bit in the RX_CNTR_R1 register is a 0.

1 - Initiates the latch and clear operation for the selected receiver counter.

0 - Normal operation.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RM_W1	27_h	0	RM_ CORRECT_ DIS [Default=1]	0	RM_PASS_ OCD	RM_PASS_ UNASSIGNED	RM_PASS_ BAD_ HEC	RM_ DESCRAM_ DIS [Default=1]	RM_COSET_ DIS

D7 Write with a 0 to maintain compatibility with future software versions.

D6 RM_CORRECT_DIS

1 - Forces the ATM header correction circuitry into Detection Mode. In this mode, the receive ATM mapper detects all errored headers and does not correct any of them. All cells with incorrect headers are counted by the Incorrect HEC Counter and then are dropped unless RM_PASS_BAD_HEC is a 1.

0 - Allows the receive ATM mapper to correct single bit errors in accordance with ITU Recommendation I.432 (refer to "Appendix B. References" on page 123). The receiver mapper corrects headers with single bit errors, and detects headers with multiple bit errors in Correction Mode. It detects all header errors in Detection Mode. It switches from Correction Mode to Detection Mode when it detects an error. It switches from Detection Mode to Correction Mode when it detects a valid HEC (see Figure 52).

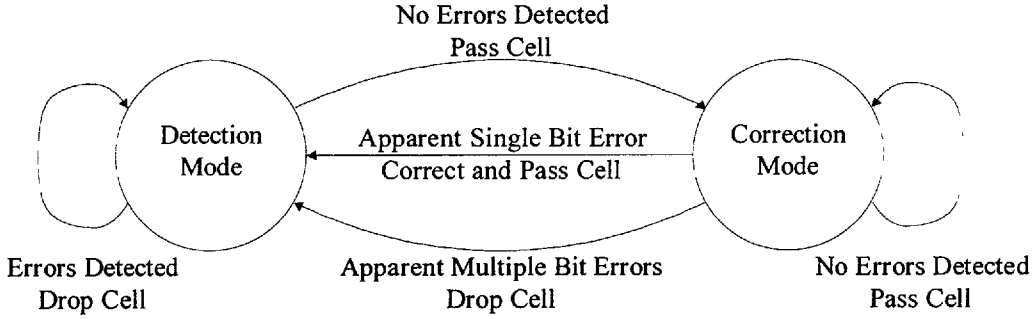

Figure 52. HEC Correction State Machine

D5 Write with a 0 to maintain compatibility with future software versions.

D4 RM_PASS_OCD

1 - Enables writing bytes to the receive ATM FIFO during OCD.

0 - Disables writing bytes to the receive ATM FIFO during OCD.

D3 RM_PASS_UNASSIGNED

1 - Enables writing physical layer and ATM layer unassigned cells to the receive ATM FIFO.

0 - Disables writing physical layer and ATM layer unassigned cells to the receive ATM FIFO.

Unassigned cells are defined as any header with the first five bytes matching $X000000XXX_h$, where X is any hexadecimal digit.

D2 RM_PASS_BAD_HEC

1 - Enables writing cells with incorrect headers to the receive ATM FIFO.

0 - Disables writing cells with incorrect headers to the receive ATM FIFO.

D1 RM_DESCRAM_DIS

1 - Disables cell payload descrambling.

0 - Enables cell payload descrambling.

D0 RM_COSET_DIS

1 - Disables the addition of the coset (55_h) to HEC values calculated by the receiver.

0 - Enables the addition of the coset (55_h) to HEC values calculated by the receiver.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RO_W1	28_h	0	0	0	0	RO_BLOCK_ CNT_EN	RO_OVH_DIS	0	RO_OOF_INS

D(7:4) Write with a 0 to maintain compatibility with future software versions.

D3 RO_BLOCK_CNT_EN
- 1 - Allows all BIP errors per byte to be counted as a single error in accordance to ITU G.826.
- 0 - Allows each BIP error per byte to be counted individually.

D2 RO_OVH_DIS
- 1 - Disables the E3 or E4 overhead processor.
- 0 - Allows reception of E3 or E4 framed cells.

D1 Write with a 0 to maintain compatibility with future software versions.

D0 RO_OOF_INS
- 1 - Forces the receiver into the OOF state.
- 0 - Allows normal receiver framing operation.

NOTE: The following _MASK bits disable the generation of an interrupt through the INTR pin. They do not, however, affect the operation of the associated interrupt or status bits.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
INTR_ MASK_W1	$2A_h$	RO_LOF_ MASK	RO_OOF_ MASK	RM_OCD_ MASK	RM_FIFO_ OVERFLOW_ MASK	RO_PAYTYP_ MISMATCH_ MASK	RO_RDI_ MASK	RO_ TIMARK_ MASK	RO_AIS_ MASK

D7 RO_LOF_MASK
- 1 - Disables the generation of an interrupt when a Loss-Of-Frame (LOF) event occurs.
- 0 - Enables the generation of an interrupt when a LOF event occurs.

D6 RO_OOF_MASK
- 1 - Disables the generation of an interrupt when an OOF event occurs.
- 0 - Enables the generation of an interrupt when an OOF event occurs.

D5 RM_OCD_MASK
- 1 - Disables the generation of an interrupt when the receive mapper loses or gains ATM cell delineation.
- 0 - Enables the generation of an interrupt when the receive mapper loses or gains ATM cell delineation.

D4 RM_FIFO_OVERFLOW_MASK
- 1 - Disables the generation of an interrupt when the receive ATM FIFO overflow event occurs.
- 0 - Enables the generation of an interrupt when the receive ATM FIFO overflow event curs.

D3 RO_PAYTYP_MISMATCH_MASK
- 1 - Disables the generation of an interrupt when a signal label mismatch event occurs.
- 0 - Enables the generation of an interrupt when a signal label mismatch event occurs.

D2 RO_RDI_MASK
- 1 - Disables the generation of an interrupt when an RDI event occurs.
- 0 - Enables the generation of an interrupt when an RDI event occurs.

D1 RO_TIMARK_MASK
- 1 - Disables the generation of an interrupt when a time marker event occurs.
- 0 - Enables the generation of an interrupt when a time marker event occurs.

D0 RO_AIS_MASK
1 - Disables the generation of an interrupt when an AIS event occurs.
0 - Enables the generation of an interrupt when an AIS event occurs.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
INTR_MASK_ W2	$2B_h$	0	0	0	0	0	RO_CRC7_ VAL_MASK	RO_CRC7_ CHG_MASK	RX_LOS_ MASK

D(7:3) Write with a 0 to maintain compatibility with future software versions.
D2 RO_CRC7_VAL_MASK
1 - Disable the generation of an interrupt when a Trail Trace CRC7 valid event occurs.
0 - Enables the generation of an interrupt when a Trail Trace CRC7 valid event occurs.
D1 RO_CRC7_CHG_MASK
1 - Disable the generation of an interrupt when a Trail Trace CRC7 change event occurs.
0 - Enables the generation of an interrupt when a Trail Trace CRC7 change event occurs.
D0 RX_LOS_MASK
1 - Disable the generation of an interrupt when an LOS event occurs.
0 - Enables the generation of an interrupt when an LOS event occurs.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TEST_W1	$2E_h$	TEST(7:0)							
TEST_W2	$2F_h$	TEST(15:8)							

TEST(15:0)
These registers are used for production testing. The value 00_h **must** be written into these registers for normal operation. All other values are used for production testing.

16. 4. Read Ports

NOTE: All port bits marked "Not used" should be masked off by the software to maintain compatibility with future versions of the chip.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_CNTR_W1	03_h								TX_CNTR_ LATCH

D(7:1) Not used.
D0 TX_CNTR_LATCH

NOTE: This bit becomes a 1 when the microprocessor writes a 1 to the associated write register, indicating that the counter should be latched. This bit becomes a 0 when the latch process is completed.

1 - Counter latch and clear in progress.
0 - Counter latch and clear completed.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RO_R1	$0D_h$	RO_TRAIL_TRACE1(7:0)							
RO_R2	$0E_h$	RO_TRAIL_TRACE2(7:0)							
RO_R3	$0F_h$	RO_TRAIL_TRACE3(7:0)							
RO_R4	10_h	RO_TRAIL_TRACE4(7:0)							
RO_R5	11_h	RO_TRAIL_TRACE5(7:0)							
RO_R6	12_h	RO_TRAIL_TRACE6(7:0)							
RO_R7	13_h	RO_TRAIL_TRACE7(7:0)							
RO_R8	14_h	RO_TRAIL_TRACE8(7:0)							
RO_R9	15_h	RO_TRAIL_TRACE9(7:0)							
RO_R10	16_h	RO_TRAIL_TRACE10(7:0)							
RO_R11	17_h	RO_TRAIL_TRACE11(7:0)							
RO_R12	18_h	RO_TRAIL_TRACE12(7:0)							
RO_R13	19_h	RO_TRAIL_TRACE13(7:0)							
RO_R14	$1A_h$	RO_TRAIL_TRACE14(7:0)							
RO_R15	$1B_h$	RO_TRAIL_TRACE15(7:0)							
RO_R16	$1C_h$	RO_TRAIL_TRACE16(7:0)							

D(7:0) RO_W1 through RO_W16
Contain the contents of the 16-byte receive trail trace message. D7 of each byte is the first bit to be received in the serial data stream.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RO_R17	$1D_h$							RO_PAYDEP(1:0)	

D(7:2) Not used.
D(1:0) RO_PAYDEP
Contains the received contents of the payload dependent bits of the MA byte.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_CNTR_R1	26_h								RX_CNTR_ LATCH

D(7:1) Not used.
D0 RX_CNTR_LATCH

NOTE: This bit becomes a 1 when the microprocessor writes a 1 to the associated write register, indicating that the counter should be latched. This bit becomes a 0 when the latch process is completed.

1 - Counter latch and clear in progress.
0 - Counter latch and clear completed.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
TX_CNTR_R2	27_h	TX_LATCHED_COUNT(7:0)							
TX_CNTR_R3	28_h	TX_LATCHED_COUNT(15:8)							

TX_LATCHED_COUNT(15:0)
This is the latched contents of the 16-bit transmit message cell counter.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
RX_CNTR_R2	29_h	RX_LATCHED_COUNT(7:0)							
RX_CNTR_R3	$2A_h$	RX_LATCHED_COUNT(15:8)							

RX_LATCHED_COUNT(15:0)
This is the latched contents of one of the five 16-bit receiver counters. The RX_CNTR_LATCH_SEL value in the RX_CNTR_W1 register determines which counter was latched.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
INTR_R1	$2D_h$	RO_LOF_ INTR	RO_OOF_ INTR	RM_OCD_ INTR	RM_FIFO_ OVERFLOW_ INTR	RO_ PAYTYP_ MISMATCH_ INTR	RO_RDI_ INTR	RO_ TIMARK_ INTR	RO_AIS_ INTR

NOTE: This port is one of two interrupt registers which should be read to locate the source of an interrupt. For interrupts which are triggered on both entry and exit from a particular alarm state, an associated status bit in the STATUS_R1 register can be read to determine the current state of the alarm. This port can also be used simply to check for the occurrence of various status and alarm conditions since the last read of this port. These latched indications are cleared each time the port is read.

D7 RO_LOF_INTR: Indicates that the receiver has entered/exited the LOF state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D6 RO_OOF_INTR: Indicates that the receiver has entered/exited the OOF state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D5 RM_OCD_INTR: Indicates that the receiver has entered/exited the OCD state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D4 RM_FIFO_OVERFLOW_INTR: Indicates that the receiver has entered/exited the receive ATM FIFO overflow state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D3 RO_PAYTYP_MISMATCH_INTR: Indicates that the receiver has entered/exited the signal label mismatch state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D2 RO_RDI_INTR: Indicates that the receiver has entered/exited the RDI state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D1 RO_TIMARK_INTR: Indicates that the receiver has detected a change of state for the time marker bit since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D0 RO_AIS_INTR: Indicates that the receiver has entered/exited the AIS state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
INTR_R2	$2E_h$						RO_CRC7_VAL_INTR	RO_CRC7_CHG_INTR	RX_LOS_INTR

NOTE: This port is one of two interrupt registers which should be read to locate the source of an interrupt. For interrupts which are triggered on both entry and exit from a particular alarm state, an associated status bit in the STATUS_R2 register can be read to determine the current state of the alarm. This port can also be used simply to check for the occurrence of various status and alarm conditions since the last read of this port. These latched indications are cleared each time the port is read.

D(7:3) Not used.

D2 RO_CRC7_VAL_INTR: Indicates that the receiver has entered/exited the Trail Trace CRC7 valid state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D1 RO_CRC7_CHG_INTR: Indicates that the receiver has detected a change in the Trail Trace CRC7 calculation since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

D0 RX_LOS_INTR: Indicates that the receiver has entered/exited the LOS state since the last time the register was read.
1 - A status change has occurred.
0 - No status changes have occurred.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
STATUS_R1	$2F_h$	RO_LOF	RO_OOF	RM_OCD	RM_FIFO_ OVERFLOW	RO_ PAYTYP_ MISMATCH	RO_RDI	RO_ TIMARK	RO_AIS

D7 RO_LOF
- 1 - Indicates that the receiver is detecting LOF.
- 0 - Indicates that the receiver is not detecting LOF.

D6 RO_OOF
- 1 - Indicates that the receiver is detecting OOF.
- 0 - Indicates that the receiver is not detecting OOF.

D5 RM_OCD
- 1 - Indicates that the receiver is detecting OCD.
- 0 - Indicates that the receiver is not detecting OCD.

D4 RM_FIFO_OVERFLOW
- 1 - Indicates that the receive ATM FIFO is in overflow state.
- 0 - Indicates that the receive ATM FIFO is not in overflow state.

D3 RO_PAYTYP_MISMATCH
- 1 - Indicates that the receiver is detecting a signal label mismatch.
- 0 - Indicates that the receiver is not detecting a signal label mismatch.

D2 RO_RDI
- 1 - Indicates that the receiver is detecting RDI.
- 0 - Indicates that the receiver is not detecting RDI.

D1 RO_TIMARK:
- 1 - Indicates that the receiver is detecting a 1 for the time marker bit.
- 0 - Indicates that the receiver is detecting a 0 for the time marker bit.

D0 RO_AIS
- 1 - Indicates that the receiver is detecting AIS.
- 0 - Indicates that the receiver is not detecting AIS.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
STATUS_R2	30_h						RO_CRC7_ VAL		RX_LOS

D(7:1) Not used.

D2 RO_CRC7_VAL

1 - Indicates that the receiver is detecting a valid Trail Trace CRC7 calculation.

0 - Indicates that the receiver is not detecting a valid Trail Trace CRC7 calculation.

D1 Not used.

D0 RX_LOS

1 - Indicates that the receiver is detecting LOS.

0 - Indicates that the receiver is not detecting LOS.

NAME	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
HW_REV_R1	$3F_h$	0	0	0	0	0	0	0	0

D(7:0) HW_REV

This is the hardware revision level of the device.

APPLICATION NOTES

1. CONNECTING TO A GENERIC PHYSICAL MEDIUM-DEPENDENT LAYER

Figure 1 depicts the WAC-034-B connected to a generic physical medium-dependent layer. The transmit timing, which is not shown, can be the recovered timing or can be synthesized from a local clock. The received data is fed to a clock recovery circuit which generates separate recovered timing and data signals. The recovered timing and data signals can then be fed into the WAC-034-B.

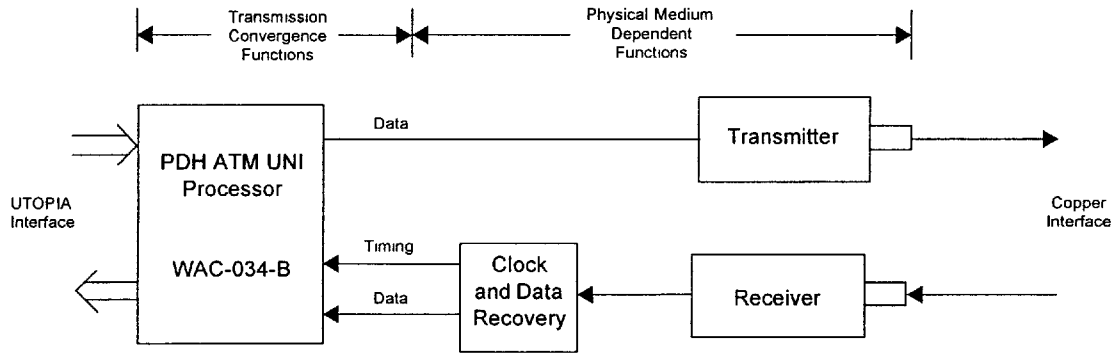

Figure 1. Connection to a Generic Physical Medium-Dependent Layer

2. CONNECTING TO SSI LIUS

The WAC-034-B can be connected directly to an SSI 78P7200 (E3/DS3 Line Interface with Receive Equalizer). Figure 2 shows the interface between the WAC-034-B and the 78P7200-IP.

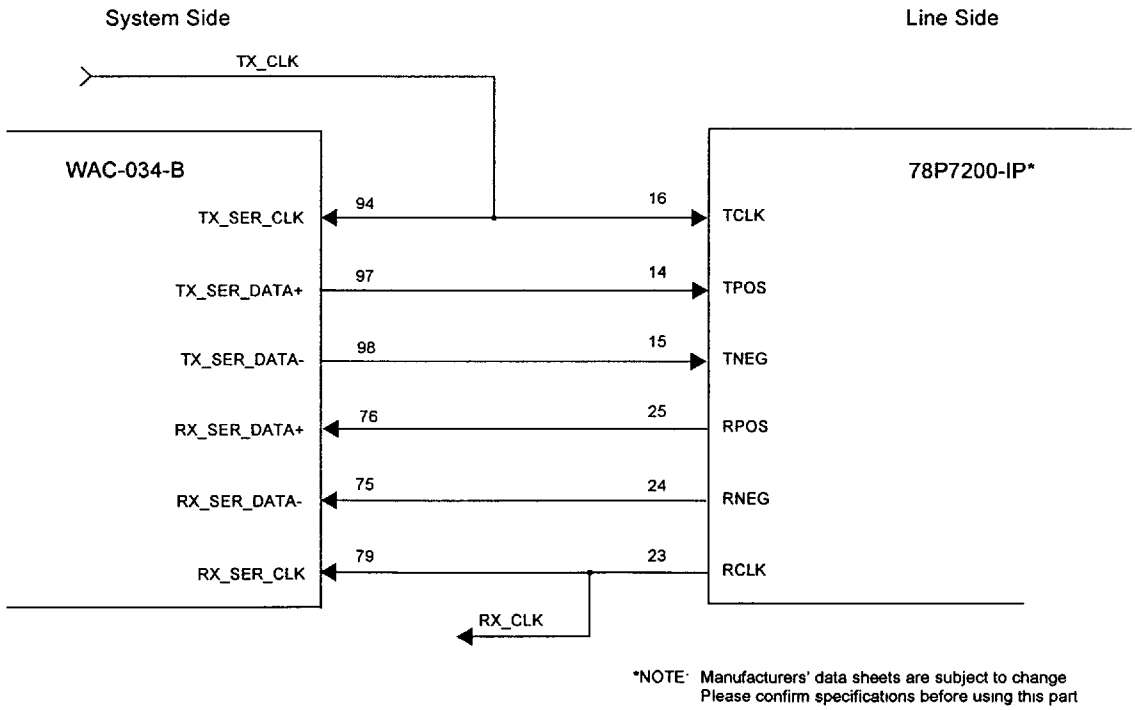

Figure 2. Connection to an SSI Line Interface

3. CONNECTING TO AT&T OR CRYSTAL LIUS

To use the WAC-034-B with the AT&T T7295, the Crystal CS7295, or the Crystal CS6300 DS3/STS-1 Line Receivers, an inverter must be used for the receiver clock input as shown in Figure 3. The inverter should have a maximum propagation delay of 5.5 ns to meet proper setup and hold times. A fast (5ns) PAL, such as the PAL20 series produced by Cypress Semiconductor, is the recommended part for this application.

To use the WAC-034-B with the AT&T T7296, or the Crystal CS7296 Line Transmitter, a pair of flip-flops must be used for the transmit data outputs as shown in Figure 3. The flip-flops should have a maximum propagation delay of 5.5 ns to meet proper setup and hold times. A fast (5 ns) PAL, such as the PAL20 series produced by Cypress Semiconductor, is the recommended part for this application.

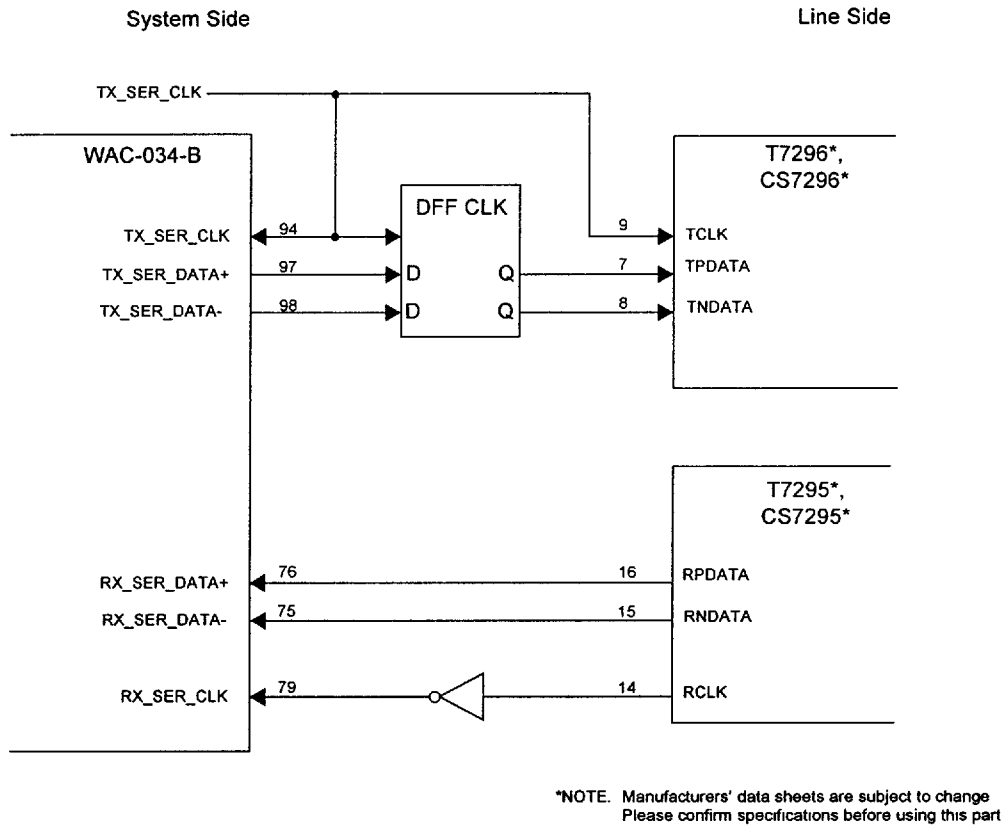

Figure 3. Connection to an AT&T or Crystal Line Interface

4. CONNECTING TO A DS1 FRAMER

The WAC-034-B can be connected to off-the-shelf DS1 framers by using some external circuitry. The external circuit block shown in Figure 4 provides the following functions:

- The parallel-to-serial/serial-to-parallel conversion.
- Byte alignment with the framing bit.
- The gapped parallel clocks.

Figure 4 shows the interface between the WAC-034-B and the external circuit block, and the interface between the external circuit block and the Dallas DS2180A, the EXAR XR-T5690, or the Level One LXP2180A. To use this configuration, SER_IO_EN must be low, RATE (A=00_h, D2 and D1) must be set to 01 or 10, TO_OVH_DIS (A=$0B_h$, D2) must be set to 1, and RO_OVH_DIS (A=28_h, D2) must be set to 1.

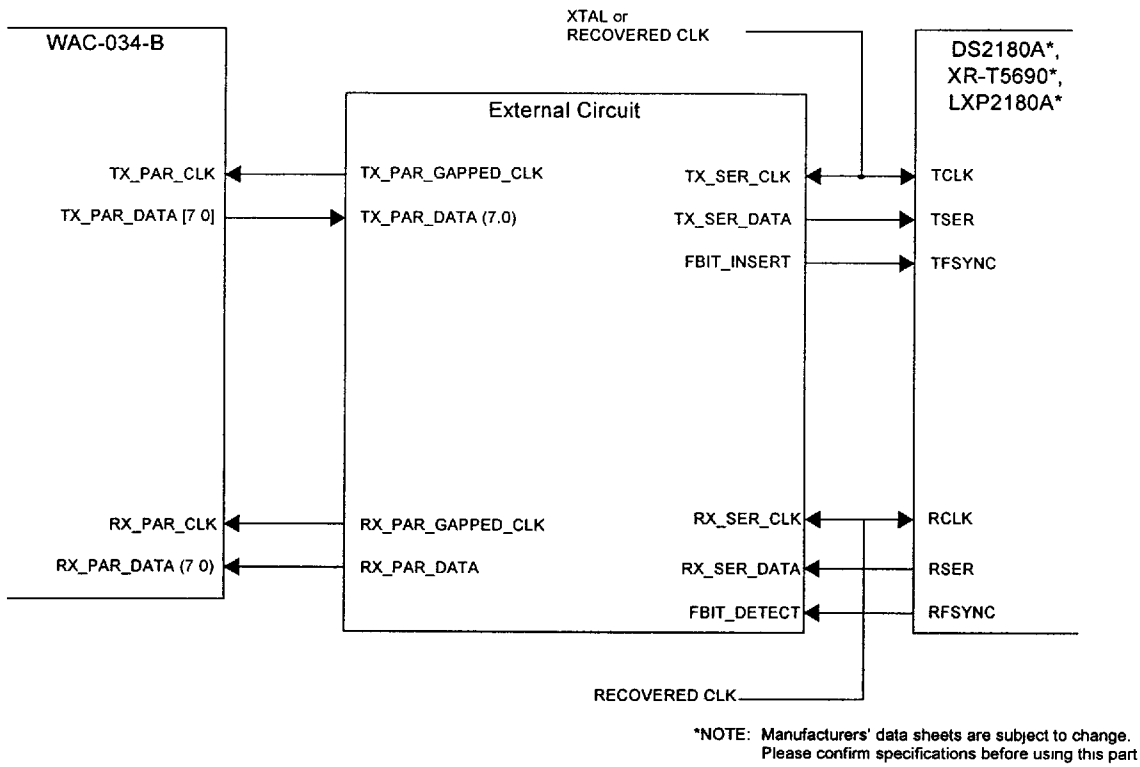

Figure 4. Connection to a DS1 Framer

5. CONNECTING TO AN E1 FRAMER

The WAC-034-B can be connected to off-the-shelf E1 framers by using some external circuitry. The external circuit block shown in Figure 5 provides the following functions:

- The parallel-to-serial/serial-to-parallel conversion.
- Byte alignment with the framing bit.
- The gapped parallel clocks.

Figure 5 shows the interface between the WAC-034-B and the external circuit block, and the interface between the external circuit block and the Dallas DS2181A or the Level One LXP2181A. To use this configuration, SER_IO_EN must be low, RATE (A=00_h, D2 and D1) must be set to 01 or 10, TO_OVH_DIS (A=$0B_h$, D2) must be set to 1, and RO_OVH_DIS (A=28_h, D2) must be set to 1.

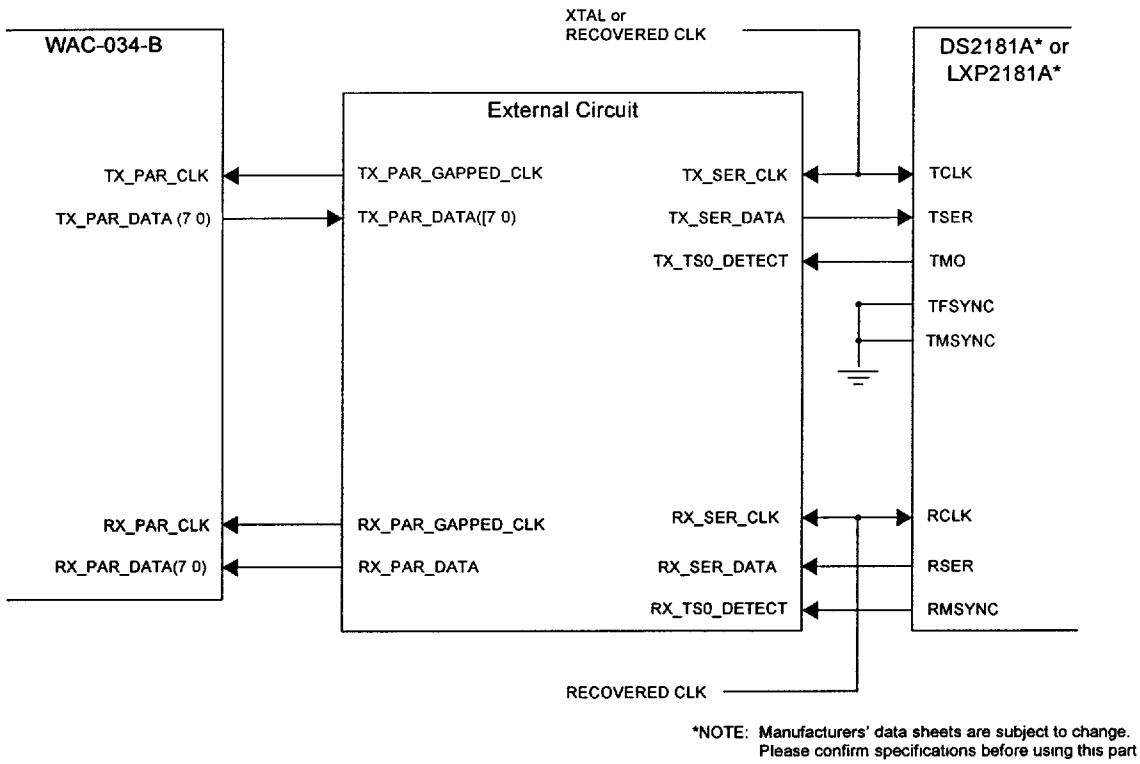

Figure 5. Connection to an E1 Framer

6. BOARD-LEVEL SIGNAL TESTING

The WAC-034-B has two test modes which may be of use when performing board-level signal testing. The WAC-034-B can generate:

- an All 1s pattern for signal power measurement, and
- a 100 pattern for waveform measurement.

To generate the All 1s pattern, set the TEST_W2(A=$2F_h$) registers to 05_h. To generate the 100 pattern, set the TEST_W2(A=$2F_h$) registers to 06_h. Note that for normal operation the TEST_W2 registers must have the value 00_h.

APPENDICES

APPENDIX A. NOMENCLATURE

A. 1. Definitions

Transmit Signals: all signals related to processing the data heading towards the optical/electrical layer.
Receive Signals: all signals related to processing the data heading towards the ATM layer.

A. 2. Signal Name Prefixes

All pins and alarm names in the WAC-034-B have prefixes indicating the functional layer they are associated with (refer to Table A-1).

Table A-1. Prefixes and Associated Functional Layers

Pin Name Prefix	Associated Functional Layer
TM	Transmit Mapper
TO	Transmit Overhead
TPHY	Transmit UTOPIA PHY Layer
TX	Transmit
RM	Receive Mapper
RO	Receive Overhead
RPHY	Receive UTOPIA PHY Layer
RX	Receive

A. 3. Numbers

Hexadecimal numbers are followed by the suffix "$_h$", for example: 1_h, $2C_h$. Binary and decimal numbers appear without suffixes.

A. 4. Glossary of Abbreviations

Table A-2. Standard Abbreviations

Abbreviation	Description
AIS	Alarm Indication Signal
AMI	Alternating Mark Inversion
ATM	Asynchronous Transfer Mode
B3ZS	Bipolar 3 Zero Substitution
BIP	Bit Interleaved Parity
BPV	Bipolar Violation
EM	Error Monitoring
FA	Frame Alignment
FEAC	Far-End Alarm and Control
FEBE	Far-End Block Error
GFC	Generic Flow Control
HDB3	High Density Bipolar 3
HEC	Header Error Check
LOF	Loss-Of-Frame
LOS	Loss-Of-Signal
MA	Memory Administration
NRZ	Non-Return to Zero
OCD	Out-Of-Cell Delineation
OOF	Out-Of-Frame
PDH	Plesiochronous Digital Hierarchy
PHY	Physical
PLCP	Physical Layer Convergence Protocol
POI	Path Overhead Indentifier
POH	Path Overhead
RAI	Remote Alarm Indication
RDI	Remote Defect Indication
SOC	Start-Of-Cell
SPE	Synchronous Payload Envelope
TR	Trail Trace
UNI	User Network Interface
WAN	Wide Area Network

APPENDIX B. REFERENCES

- ATM Forum, "ATM User-Network Interface Specification", V2.0, June 1, 1992.
- ATM Forum, "ATM User-Network Interface Specification", V3.0, September 10, 1993.
- Bell Communications Research, "SONET Transport Systems: Common Generic Criteria", TR-NWT-000253, Issue 2, December 1991.
- Bell Communications Research, "Local Access System Generic Requirements, Objectives, and Interfaces in Support of Switched Multi-megabit Data Service", TR-TSV-000773, Issue 1, June 1991.
- IEEE 1149.1, "Standard Test Access Port and Boundary Scan Architecture", May 21, 1990.
- ITU (CCITT) Recommendation G.783, "Characteristics of Synchronous Digital Hierarchy (SDH) Multiplexing Equipment Functional Blocks", 1990.
- ITU (CCITT) Draft Recommendation G.804, "ATM Cell Mapping Into Plesiochronous Digital Hierarchy (PDH)", January 1993.
- ITU (CCITT) Draft Recommendation G.832, "Transport of SDH Elements on PDH Networks: Frame and Multiplexing Structures", January 1993.
- ITU (CCITT) Recommendation G.709, "Synchronous Multiplexing Structure", Volume III, Fascicle III.4, 1988.
- ITU (CCITT) Recommendation G.751, "Digital Multiplex Equipments Operating at the Third Order Bit Rate of 34368 kbits/s and the Fourth Order Bit Rate of 139264 kbit/s and Using Positive Justification".
- ITU (CCITT) Draft Recommendation G.775, "Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection Criteria for Equipment Based on the Hierarchy Bit Rates in Recommendation G.702".
- ITU (CCITT) Recommendation I.432, "B-ISDN User-Network Interface - Physical Interface Specification", June 1990.
- ITU (CCITT) Draft Recommendation G.826, "Error Performance Parameters and Objectives for International Constant Bit Rate Digital Paths At or Above the Primary Rate", March 12, 1993.
- ETSI Draft prETS 300 337, "Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including ATM cells) at the CCITT Recommendation G.702 hierarchical rates of 2048 kbit/s, 34368 kbit/s and 139264 kbit/s", August 1993.
- UTOPIA, "An ATM PHY Data Path Interface", V1.02-Draft, August, 1993.
- UTOPIA, "An ATM PHY Data Path Interface", Level 1, V2.01, February, 1994.

APPENDIX C. NEW FEATURES IN THIS RELEASE

Changes in the WAC-034-B version from the WAC-034-A version are as follows:

- Two interrupt bits (RO_CRC7_VAL_INTR and RO_CRC7_CHG_INTR) and a status bit (RO_CRC7_VAL) were added to indicate the status of the Trail Trace for E3 and E4.
- The timing for some signals has changed. Please refer to section "6. Timing Diagrams" starting on page 27 and to section "14. Timing Diagrams" starting on page 81 for the correct timing.
- The HW_REV_R1 (A=$3F_h$, D7:D0) register contains the value 01_h.