V51C259HL FAMILY
HIGH PERFORMANCE LOW POWER
STATIC COLUMN 64K x 4 BIT
CMOS DYNAMIC RAM

	V51C259HL-12	V51C259HL-15	V51C259HL-20
Maximum Access Time (ns)	120	150	200
Maximum Column Address Access Time (ns)	55	65	85
Maximum CMOS Standby Current (mA)	0.1	0.1	0.1

Features

- Static Column Mode Operation
  - Continuous data rate over 13 MHz
  - Random access from address within row
  - t_{CAC} = 25, 30, 35 ns
  - t_{OAC} = 20, 25, 30 ns
- Low Input/Output Capacitance
- Low Power Data Retention
  - Standby current, CMOS—100 μA (max.)
  - Refresh period, $\overline{RAS}$-Only—32 ms (max.)
  - Data Retention Current—230 μA (max.)
- TTL and HCT Compatible
- High Reliability Plastic—18 Pin DIP

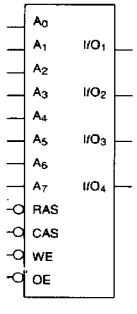
Description

The Vitelic V51C259HL is a high speed 65,536 x 4 dynamic Random Access Memory. Fabricated with Vitelic's VICMOS III technology, the V51C259HL offers features not provided by an NMOS dynamic RAM: Static Column Mode for high data bandwidth, fast useable speed, and CMOS standby current and extended $\overline{RAS}$-Only refresh for low standby power. All inputs and outputs are compatible to both TTL and HCT logic families while the input and output capacitances are significantly lowered to allow increased system performance.

Static Column Mode operation allows random or sequential access of all 256 bits within a row simply by changing the column address. Because column address access time is as fast as 55 ns, a continuous data rate of over 13 million 4 bit nibbles per second can be achieved. The V51C259HL offers high performance while relaxing many critical system timing requirements for fast usable speed. These features make the V51C259HL ideally suited for graphics, digital signal processing, and high performance systems.

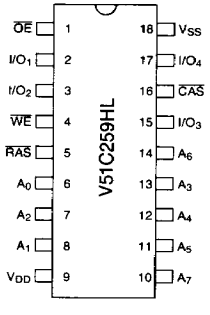
The V51C259HL offers a maximum standby current of 100 μA when $\overline{RAS} \geq V_{DD} - 0.5V$. During standby (i.e. refresh only cycles), the refresh period can be extended to 32 ms to reduce the total current required to retain data to less than 230 μA (max.). The V51C259HL combines this low power with high density for portable and battery backup applications.

LOGIC SYMBOL



PIN CONFIGURATION

(Top View)



PIN NAMES

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A_{0-A7}	Address Inputs
$I/O_{1-I/O4}$	Data In/Data Out
V_{DD}	Power (+5V)
V_{SS}	Ground

Absolute Maximum Ratings†

Ambient Temperature
Under Bias . . . . . –10°C to +80°C
Storage
Temperature (Plastic) . . . . . –55°C to +125°C
Voltage on Any Pin except V_{DD} and D_{OUT}
Relative to V_{SS} . . . . . –2.0V to 7.5V
Voltage on V_{DD}
Relative to V_{SS} . . . . . –1.0V to 7.5V
Voltage on D_{OUT}
Relative to V_{SS} . . . . . –2.0V to V_{DD} + 1V
Data Out Current . . . . . .50 ma
Power Dissipation 1.0W

†COMMENT
Stresses above those listed under "Absolute Maximum Rating" may cause damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

D.C. Characteristics[1]

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	V51C259HL Min.	V51C259HL Typ[2]	V51C259HL Max.	Unit	Test Conditions		Notes
I_{DD1}	V_{DD} Supply Current, Operating		60	70	mA	t_{RC} = t_{RC} (min.)	-12	3,4
			49	60			-15	
			40	50			-20	
I_{DD2}	V_{DD} Supply Current, TTL Standby		0.5	2	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, all other inputs and outputs ≥ V_{SS}		
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh		57	70	mA	t_{RC} = t_{RC} (min.)	-12	4
			45	60			-15	
			36	50			-20	
I_{DD4}	V_{DD} Supply Current, Static Column Mode		27	70	mA	Minimum Cycle	-12	3,4
			23	60			-15	
			21	50			-20	
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		1.5	4	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs and outputs ≥ V_{SS}		3
I_{DD6}	V_{DD} Supply Current, CMOS Standby		0.01	0.1	mA	$\overline{RAS}$ ≥ V_{DD} –0.5V and $\overline{CAS}$ at V_{IH}, all other inputs and output ≥ V_{SS}		
$\|I_{LI}\|$	Input Load Current (any pin)			1	μA	V_{IN} = V_{SS} to V_{DD}		
$\|I_{LO}\|$	Output Leakage Current, High Impedance State			1	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, D_{OUT} = V_{SS} to V_{DD}		
V_{IL}	Input Low Voltage (all inputs)	–0.3		0.8	V			5
V_{IH}	Input High Voltage (all inputs)	2.4		V_{DD} + 1	V			6
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA		6
				0.1	V	I_{OL} = 100 μA		
V_{OH}	Output High Voltage (all outputs)	2.4			V	I_{OH} = –5 mA		6
		V_{DD}–0.1			V	I_{OH} = –100 μA		

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and V_{DD} = +5V.
3. I_{DD} is dependent upon output loading when the device output is selected. I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max) is measured with a maximum of two transitions per address cycle in Static Column Mode.
5. Specified V_{IL} (min) is steady state operation. During transitions, V_{IL} may undershoot to –1.0V for periods not to exceed 20 ns. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
6. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured as noted in the A.C. Characteristics section.

Capacitance

T_A = 25°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	4	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	3	5	pF
$C_{I/O}$	Data In/Out	4	6	pF

A.C. Characteristics[1, 2, 3]

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Read, Write and Refresh Cycles

No.	JEDEC Symbol	Symbol	Parameter	V51C259HL-12		V51C259HL-15		V51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	120	75000	150	75000	200	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	185		240		310		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	55		80		100		ns	
4	t_{RL1CH1}	t_{CSH}*	$\overline{CAS}$ Hold Time	120		150		200		ns	
5	t_{CL1CH1}	t_{CAS}*	$\overline{CAS}$ Pulse Width	25		30		35		ns	
6	t_{WH2RL2}	t_{WRP}	$\overline{Write\ Enable}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns	
7	t_{RL1WL2}	t_{RWH}	$\overline{RAS}$ to $\overline{Write\ Enable}$ Hold Time	20		20		25		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		20		25		ns	
10	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High Impedance		20		25		30	ns	4,5
11	t_{CL2QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low Impedance	0		0		0		ns	4,5
	t_{RVRV}	t_{REF1}	Time Between Refresh		4		4		4	ms	6
	t_{RVRV}	t_{REF2}	Time Between Refresh ($\overline{RAS}$-Only)		32		32		32	ms	6
	t_T	t_T	Transition Time (Rise and Fall)	1	25	1	25	1	25	ns	7

NOTES:

*This parameter not applicable if operated with $\overline{CAS}$ grounded.

1. All voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as a $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).
3. A.C. Characteristics assume t_T = 5 ns. All A.C. parameters are measured with V_{OL} = 0.8V at I_{OL} – 2.2 mA, V_{OH} = 2.4V at I_{OH} = – 2.0 mA with a 50 pF load, V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
4. Assumes three state test load (5 pF and a 380 Ohm Thevenin equivalent).
5. At any given temperature and voltage combination, coincident deselection/selection is permissible for wired-OR devices.
6. The V51C259HL extends the refresh period to 32 ms during $\overline{RAS}$-Only refresh periods.
7. t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. Characteristics (Cont'd.)

Read Cycle

No.	JEDEC Symbol	Symbol	Parameter	V51C259HL-12		V51C259HL-15		V51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
12	t_{RL1QV}	t_{RAC}	Access Time From $\overline{RAS}$		120		150		200	ns	8
13	t_{CL1QV}	t_{CAC}	Access Time From $\overline{CAS}$		25		30		35	ns	
14	t_{GL1QV}	t_{OAC}	Access Time From $\overline{OE}$		20		25		30	ns	
15	t_{AVQV}	t_{CAA}	Access Time From Column Address		55		65		85	ns	14
16	t_{CL1RH1}	$t_{RSH(R)}$*	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		10		ns	
17	t_{WH2CL2}	t_{RCS}*	Read Command Set-up Time	0		0		0		ns	
18	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	55		65		85		ns	
19	t_{RL1AX}	t_{ARR}	Column Address Hold Time From $\overline{RAS}$ (Read)	110		140		190		ns	
20	t_{CH2WX}	t_{RCH}*	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		ns	
21	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	10		10		10		ns	
22	t_{RH2AX}	t_{ARH}	Column Address Hold Time to $\overline{RAS}$	0		0		0		ns	
23	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	65	25	85	30	115	ns	9
24	t_{AXQX}	t_{OHA}	Output Hold Time From Address Change	10		10		10		ns	
25	t_{GH1QX}	t_{OH}	Output Hold Time From $\overline{OE}$ or $\overline{CAS}$	0		0		0		ns	

Write Cycle

No.	JEDEC Symbol	Symbol	Parameter	V51C259HL-12		V51C259HL-15		V51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
26	t_{CL1RH1}	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	30		35		40		ns	
27	t_{RL1WL2}	t_{WDR}	$\overline{RAS}$ to Write Command Lead Time	25	90	30	115	35	160	ns	
28	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		35		ns	
29	t_{WL1CH1}	t_{CWL}*	Write Command to $\overline{CAS}$ Lead Time	25		30		35		ns	
30	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	25		30		35		ns	
31	t_{WH2WL2}	t_{WCP}	Write Command Precharge Time	5		10		15		ns	
32	t_{WL1CL2}	t_{WCS}*	Write Command Set-up Time	0		0		0		ns	10
33	t_{CL1WH1}	t_{WCH}*	Write Command Hold Time	25		30		35		ns	
34	t_{RL1WH1}	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	80		90		100		ns	
35	t_{AVWL2}	t_{AWS}	Column Address to Write Command Set-up Time	0		0		0		ns	
36	t_{WL1AX}	t_{AWH}	Column Address to Write Command Hold Time	20		25		30		ns	

NOTES:

*This parameter not applicable if operated with $\overline{CAS}$ grounded.

8. Assumes that $t_{RAD} \leq t_{RAD}$ (max) if $t_{RAD} > t_{RAD}$ (max), then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max).
9. t_{RAD} is specified for reference only.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{OWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle and the data out pin will remain in high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{OWD} \geq t_{OWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-modify-write cycle.

A.C. Characteristics (Cont'd.)

Write Cycle (Cont'd.)

No.	JEDEC Symbol	Symbol	Parameter	V51C259HL-12		V51C259HL-15		V51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
37	t_{RL1AX}	t_{ARW}	Column Address Hold Time From $\overline{RAS}$ (Write)	70		80		90		ns	
38	t_{DVWL2}	t_{DS}	Data-In Set-up Time	0		0		0		ns	
39	t_{WL1DX}	t_{DH}	Data-In Hold Time	20		25		30		ns	
40	t_{GH2WH1}	t_{OWS}	$\overline{OE}$ Set-up Time From End of Write	15		20		25		ns	
41	t_{CH1GL2}	t_{COH}	$\overline{OE}$ Hold Time From $\overline{CAS}$	20		25		30		ns	

Read-Modify-Write Cycle (11)

No.	JEDEC Symbol	Symbol	Parameter	V51C259HL-12		V51C259HL-15		V51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
42	t_{RL2RL2}	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	240		305		385		ns	
43	t_{RL1RH1}	t_{RRW}	$\overline{RAS}$ Pulse Width (RMW)	175	75000	215	75000	275	75000	ns	
44	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	80		95		110		ns	
45	t_{RL1AX}	t_{AR}	Column Address Hold Time From $\overline{RAS}$ (RMW)	165		205		265		ns	
46	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	145		95		120		ns	12
47	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	80		95		120		ns	12
48	t_{CL1WL2}	t_{CWD}*	$\overline{CAS}$ to $\overline{WE}$ Delay	50		60		70		ns	12
49	t_{GH2WL2}	t_{OWD}	$\overline{OE}$ to $\overline{WE}$ Delay	25		30		35		ns	12

Static Column Mode (13)

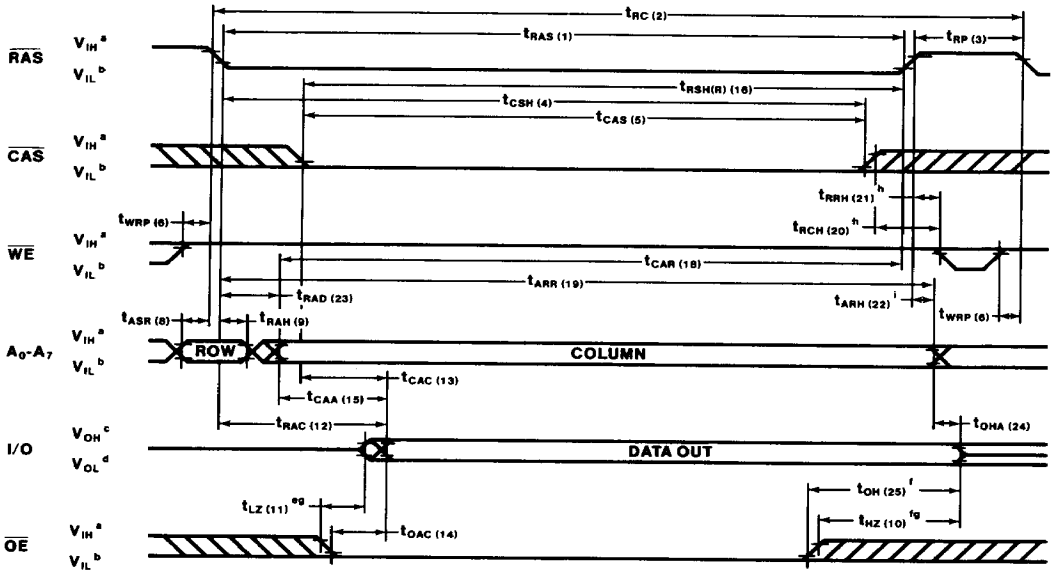
No.	JEDEC Symbol	Symbol	Parameter	V51C259HL-12		V51C259HL-15		V51C259HL-20		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
50	t_{WL2WL2}	t_{SWC}	Static Column Write Cycle Time	55		65		85		ns	
51	t_{WH2QV}	t_{WPA}	Write Precharge Access Time		55		65		85	ns	14
52	t_{WL1QV}	t_{WRA}	Write-Read Access Time		105		120		145	ns	14
53	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	25		30		35		ns	
54	t_{RL1WL2}	t_{SWH}	Delay from $\overline{RAS}$ to Second Write Command	120		150		200		ns	

NOTES:

*This parameter not applicable if operated with $\overline{CAS}$ grounded.

11. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{OWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle and the data out pin will remain in high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{OWD} \geq t_{OWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-modify-write cycle.
13. All previously specified A.C. characteristics are applicable.
14. Access time from a write command or a read command is determined by the longer of t_{CAA} or t_{WPA} or t_{WRA}.

Waveforms of Read Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{LZ} is referenced to the later of $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ low transition.

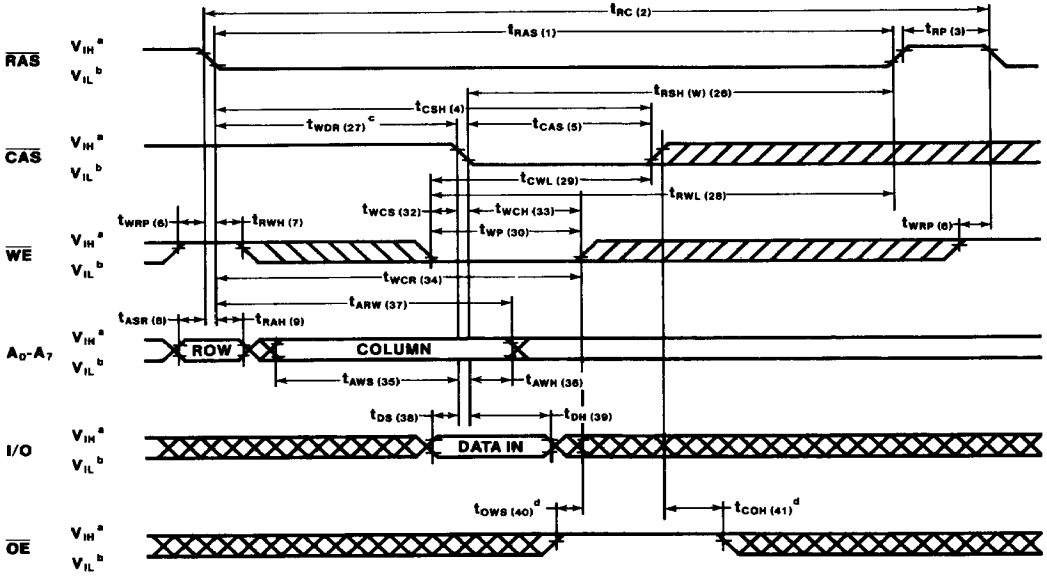
f. t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ or $\overline{OE}$ high transition.

g. Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

h. Either t_{RCH} or t_{RRH} must be satisfied.

i. If $t_{RRH} \geq t_{ARH}$ (min), then data from the last address will be latched on D_{OUT} by a $\overline{RAS}$ high transition, until either a $\overline{CAS}$ or $\overline{OE}$ high transition releases the data.

Waveforms of Write Cycle ($\overline{CAS}$ Controlled) [e]



NOTES:

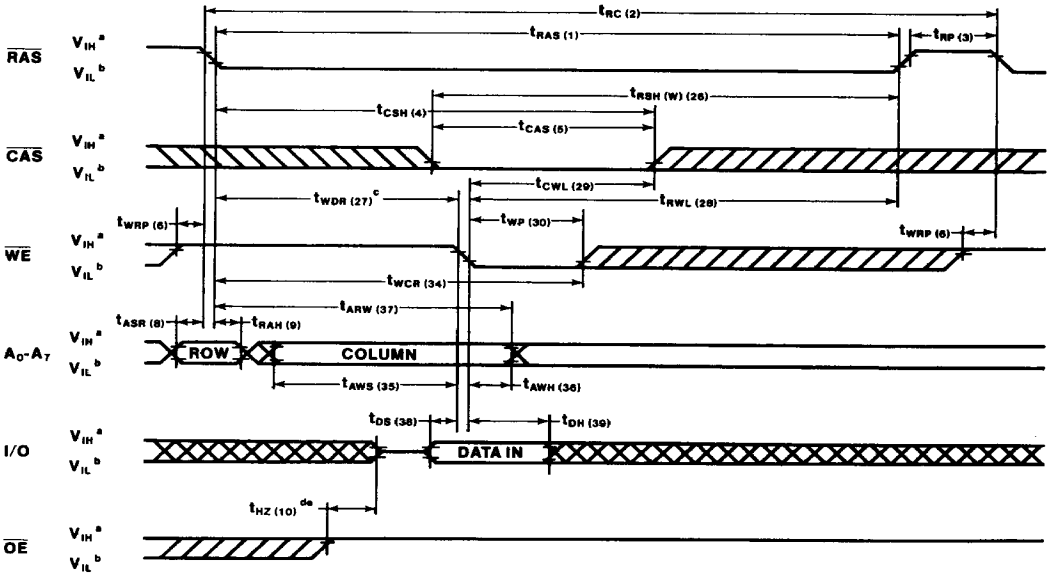
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c. t_{WDR} is reference to the later of the $\overline{CAS}$ or $\overline{WE}$ low transition.

d. If the low transition of $\overline{WE}$ occurs before or simultaneously with the low transition of $\overline{CAS}$ and the high transition of $\overline{CAS}$ or $\overline{RAS}$ occurs before the high transition of $\overline{WE}$, then the outputs remain in a high impedance state (i.e., $\overline{OE}$ is a don't care).

e. $\overline{WE}$ is low prior to or simultaneously with $\overline{CAS}$ low transition. $\overline{CAS}$ is high prior to $\overline{RAS}$ low transition.

Waveforms of Write Cycle ($\overline{WE}$ Controlled)[f]



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

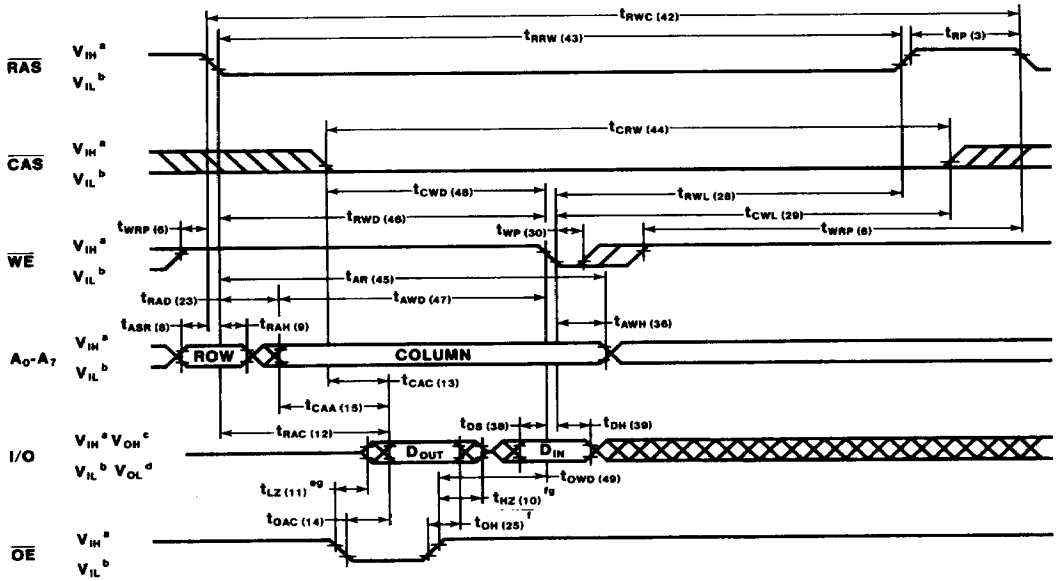
c. t_{WDR} is reference to the later of the $\overline{CAS}$ or $\overline{WE}$ low transition.

d. t_{HZ} is referenced to the earlier of the $\overline{CAS}$ or $\overline{OE}$ high transition or $\overline{WE}$ low transition.

e. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

f. $\overline{CAS}$ is low prior to the $\overline{WE}$ low transition.

Waveforms of Read/Modify/Write Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

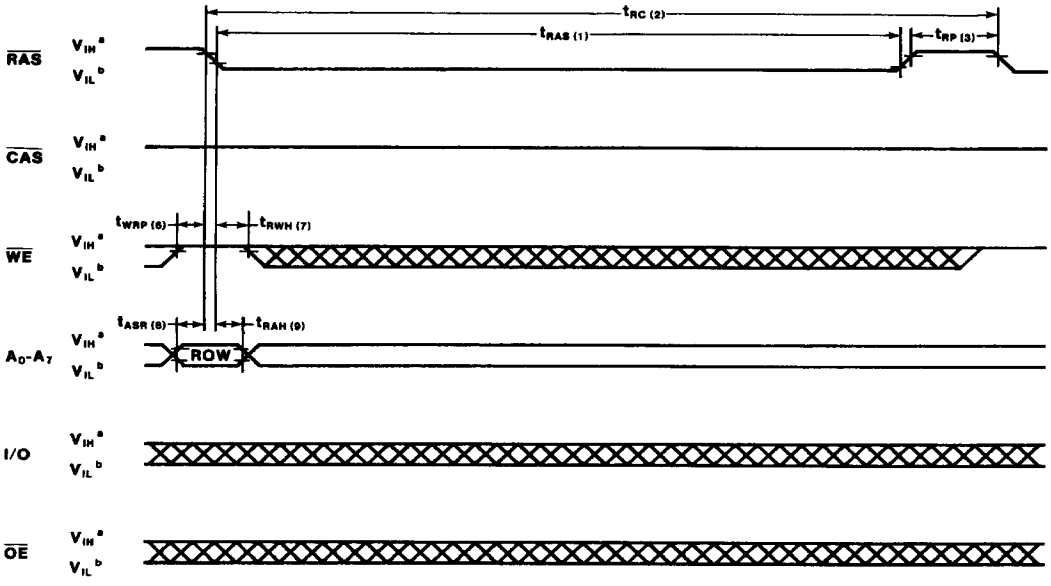
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{LZ} is referenced to the later of $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ low transition.

f. t_{HZ} and t_{OH} are referenced to the earlier of the $\overline{CAS}$ or $\overline{OE}$ high transition.

g. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

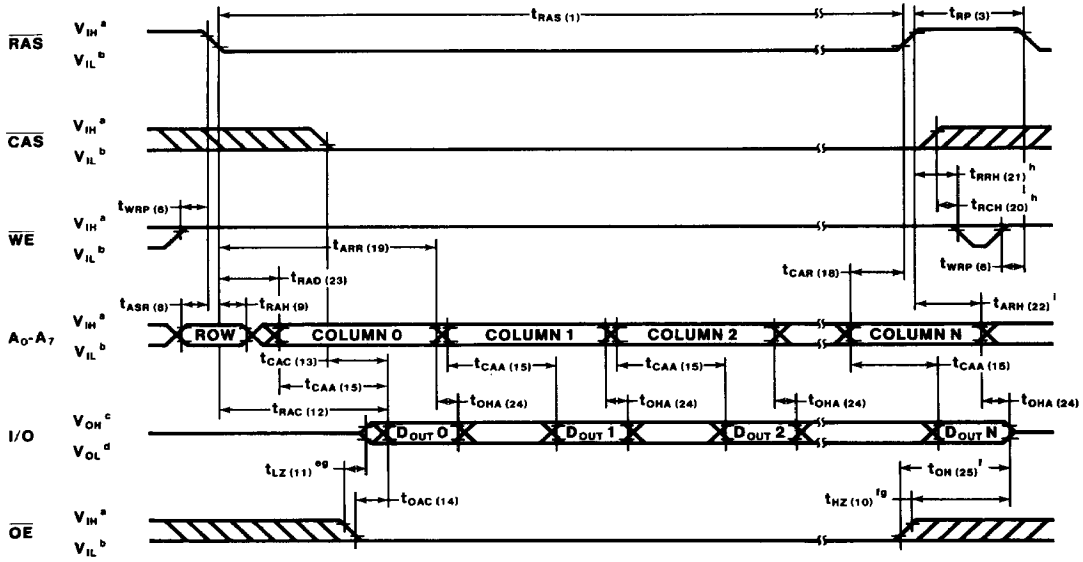
Waveforms of $\overline{RAS}$-Only Refresh Cycle



NOTE:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

Waveforms of Static Column Mode Read Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{LZ} is referenced to the later of $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ low transition.

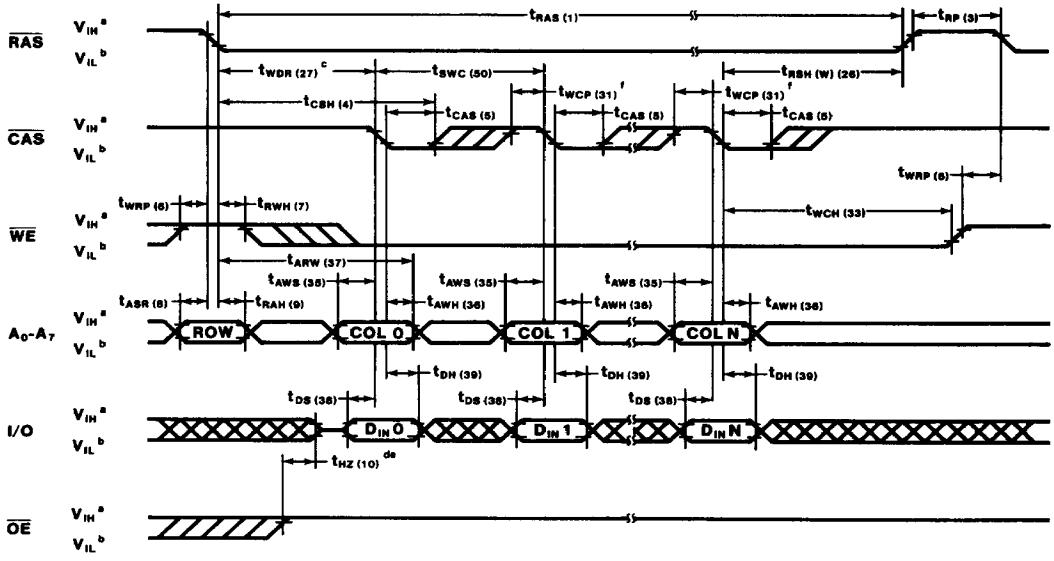
f. t_{HZ} and t_{OH} are referenced to the earlier of the $\overline{CAS}$ or $\overline{OE}$ high transition.

g. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

h. Either t_{RCH} or t_{RRH} must be satisfied.

i. If $t_{ARH} \geq t_{ARH}$ (min), then data from the last address will be latched on D_{OUT} by a $\overline{RAS}$ high transition, until either a $\overline{CAS}$ or $\overline{OE}$ high transition releases the data.

Waveforms of Static Column Mode Write Cycle ($\overline{CAS}$ Controlled) g



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c. t_{WDR} is reference to the later of the $\overline{CAS}$ or $\overline{WE}$ low transition.

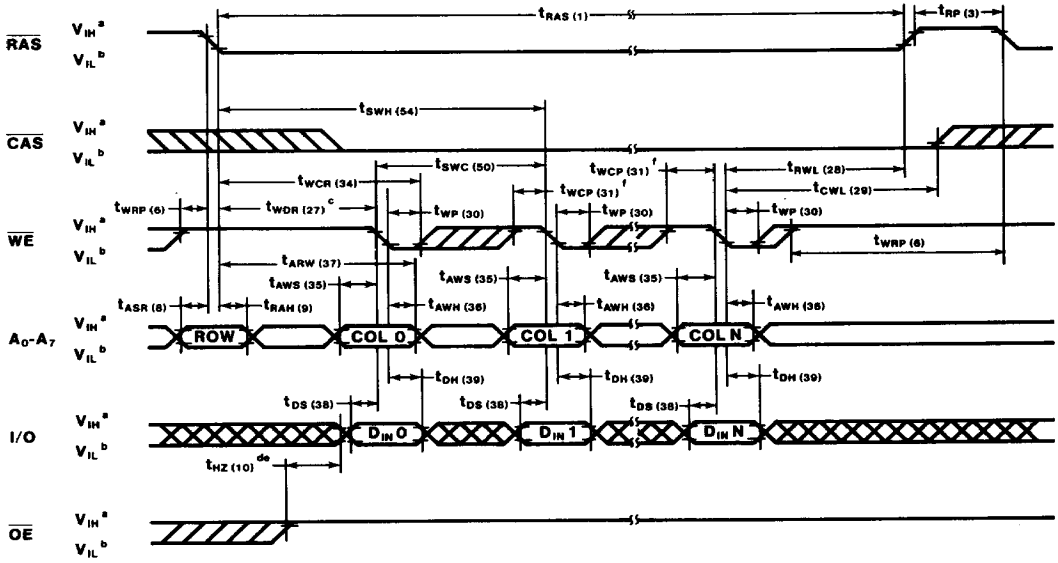
d. t_{HZ} is referenced to the earlier of the $\overline{CAS}$ or $\overline{OE}$ high transition or $\overline{WE}$ low transition.

e. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

f. t_{WCP} is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

g. $\overline{WE}$ is low prior to or simultaneously with a $\overline{CAS}$ low transition. $\overline{CAS}$ is high prior to a $\overline{RAS}$ low transition.

Waveforms of Static Column Mode Write Cycle ($\overline{WE}$ Controlled) [g]



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c. t_{WDR} is reference to the later of the $\overline{CAS}$ or $\overline{WE}$ low transition.

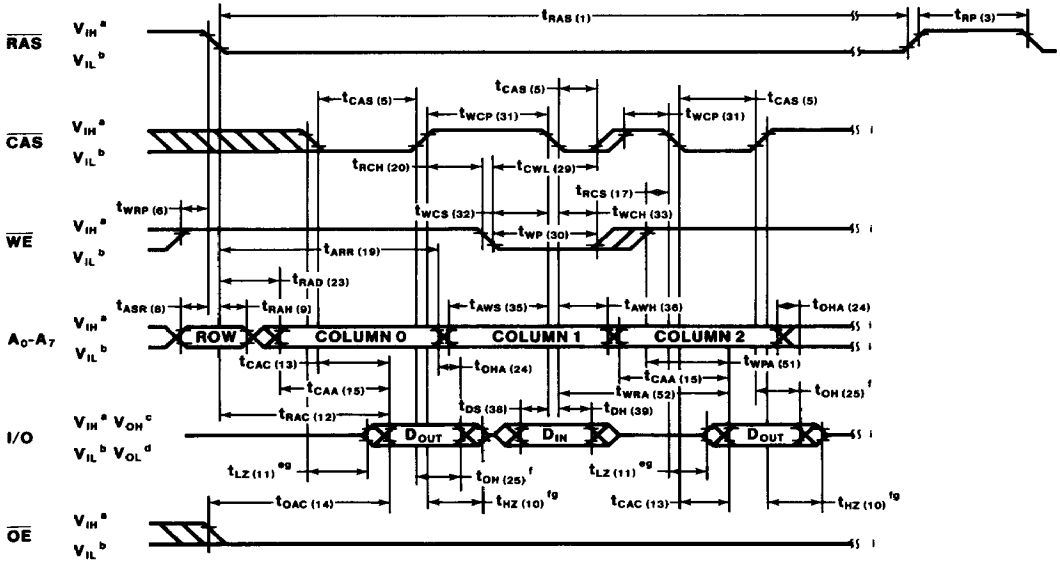
d. t_{HZ} is referenced to the earlier of the $\overline{RAS}$ or $\overline{CAS}$ or $\overline{OE}$ high transition.

e. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

f. t_{WCP} is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

g. $\overline{CAS}$ is low prior to a $\overline{WE}$ low transition.

Waveforms of Static Column Mode Read/Write/Read. . .Cycle ($\overline{CAS}$ Controlled) [h]



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{LZ} is referenced to the later $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$ are low transition.

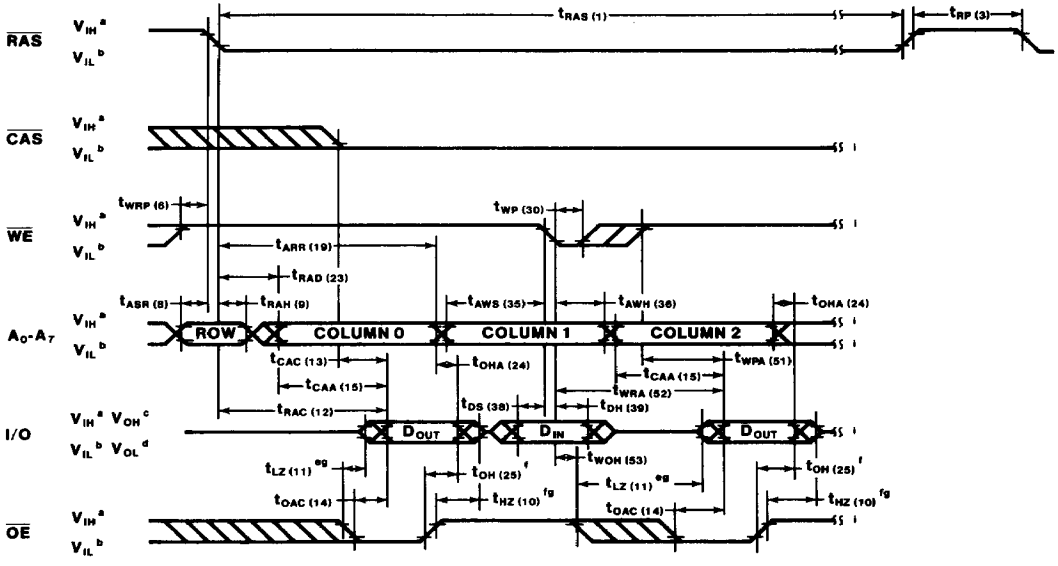
f. t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ or $\overline{OE}$ high transition.

g. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

h. $\overline{WE}$ is low prior to or simultaneously with a $\overline{CAS}$ low transition.

i. The cycle can be terminated by either a read or a write operation followed by a $\overline{RAS}$ high transition. See pages 36 or 37 for timings.

Waveforms of Static Column Mode Read/Write/Read. . .Cycle ($\overline{WE}$ Controlled) [h]



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{LZ} is referenced to the later of $\overline{RAS}$ $\overline{CAS}$, and $\overline{OE}$ high transition.

f. t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ or $\overline{OE}$ high transition if $\overline{RAS}$ and $\overline{CAS}$ and $\overline{OE}$ are low.

g. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

h. $\overline{CAS}$ is low prior to a $\overline{WE}$ low transition.

i. The cycle can be terminated by either a read or a write operation followed by a $\overline{RAS}$ high transition. See pages 36 or 38 for timings.

Functional Description

The V51C259HL is a CMOS dynamic RAM optimized for the high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The V51C259HL reads and writes 4 bits of data at a time by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, is only latched during a write cycle by the later of either Column Address Strobe ($\overline{CAS}$) or Write Enable ($\overline{WE}$). During the read cycle, the column address is not latched and continuously flows through the internal input latches. Access time is primarily dependent on a valid column address. $\overline{CAS}$ acts as chip select signal and may remain low during the entire memory operation.

Memory Cycle

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, has elapsed.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{ARR}. $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation. Data out is controlled by the Output Enable ($\overline{OE}$) and $\overline{CAS}$ which is discussed in the Data Out Operation.

For applications where $\overline{CAS}$ is held low, the data out becomes valid when t_{RAC}, t_{CAA}, and t_{OAC} are all satisfied.

For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. Data out becomes valid only when t_{RAC}, t_{CAA}, t_{OAC}, and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{CAA}, t_{OAC}, and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{OAC}, and t_{CAC} are all satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation. To simplify the system design, the column address is latched in by the later of $\overline{WE}$ or $\overline{CAS}$. As in the read cycle, $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation. For applications where $\overline{CAS}$ is held low, the input data must be valid at or before the falling edge of $\overline{WE}$. For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Consequently, the write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the later of $\overline{WE}$ or $\overline{CAS}$ low transition. In a $\overline{CAS}$ controlled write cycle, (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ will maintain the I/O in the high impedance state; terminating with $\overline{WE}$ allows the output to go active, and the $\overline{OE}$ must be brought high to allow for inputs on the I/O.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. Any read, write, read-modify write, or $\overline{RAS}$-Only cycle will perform refresh.

Extended Refresh Cycle

The V51C259HL extends the refresh cycle period to 32 milliseconds for $\overline{RAS}$-Only refresh cycles. This feature reduces the total current consumption to a maximum of 230 μA, and typically 90 μA, for data retention. The low standby current can significantly extended battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{((t_{RC})\,(I_{Active}) + (t_{RI} - t_{RC})\,(I_{Standby}))}{t_{RI}}$$

where t_{RC} = refresh cycle time, and t_{RI} = refresh interval time or $t_{REF}/256$

Static Column Mode Operation

Static column mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Read, write and read-write-read cycles can be performed during static column mode operation. The row address is internally retained by maintaining $\overline{RAS}$ active. Following the entry cycle into static column mode operation, the data are accessed simply by changing the column address. Because the column address buffer acts as a transparent or flow-through latch, access begins from a valid column address. Thus, the V51C259HL operates like a static RAM for multiple accesses within the same row. $\overline{CAS}$ acts as an output enable.

Data Out Operation

The V51C259HL Input/Output (I/O) is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or a $\overline{CAS}$ low level enables the internal I/O data path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path, nor on the output driver. An $\overline{OE}$ low transition or an $\overline{OE}$ low level enables the output driver when the I/O data path is enabled. An $\overline{OE}$ high level disables the output driver, but does not disable the data latch when it has been enabled. A $\overline{WE}$ low level disables the output driver when a $\overline{CAS}$ low level occurs. If the $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enabled prior to the $\overline{WE}$ low transition, it is necessary to use $\overline{OE}$ to disable the output driver prior to the $\overline{WE}$ low transition to allow data in set-up time (t_{DS}). A $\overline{WE}$ high transition passes control of the output drive to $\overline{OE}$.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 32 ms).

The V_{DD} current (I_{DD}) requirement of the V51C259HL during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ = V_{SS} during power on, the device will go into an active cycle and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.