MATRA
DESIGN SEMICONDUCTOR

WRITE BUFFER SLICE™

December 1991

WB 416 AND WB 418

FEATURES

- **4 Deep Write Buffer Slice™**

  WB 416 - 16-bit Wide, 52-pin PQFP package
  WB 418 - 18-bit Wide, 64-pin PQFP package
  Available in 20-, 33- and 50-MHz

- **Can provide significant performance advantage by eliminating wait-states on writes**

  Performance gain dependent on write characteristics of software and CPU

- **Simple Universal CPU Interface:**

  CPUs Supported: 80486SX/DX, 386SX/DX, MIPS, SPARC, i860, 29K, 68040/030

- **Each Write Buffer Slice™ configurable for Data Mode or Address Mode**

  Address Mode parts used to buffer address
  Data Mode parts used to buffer data bytes and byte enables

- **WB416 - 16-bits of address or 16-bits data plus 2 byte enables**
  WB418 - 18-bits of address or 18-bits data plus 2 byte enables

- **Supports Byte-gathering and Word-gathering**

  Important for DOS/Windows - Most of the Code is 8- or 16- bit

1. OVERVIEW

The MDS WB 416/418 Write Buffer Slice™ is a four deep, 16/18-bit wide FIFO that is ideal for use as a posted write buffer. Some simple external logic implemented in a single PAL is used to interface this device to any CPU. The device supports two modes: an address mode and a data mode.

In the Address Mode it supports a 16/18-bit address which can be strobed into the device on the rising edge of **CLK**. The address is stored in the four deep FIFO and provided on the system bus upon assertion of **NEXT#**.

In the Data Mode the WB 416/418 provides 16/18-bits of data and two bits for byte enables. The data is strobed into the FIFO on the rising edge of **CLK**. The data is provided on the system bus upon assertion of **NEXT#**. In the data mode the part can also perform byte- or word-gathering when the **MF#** input is asserted.

2. DEVICE OPERATION

The Write Buffer Slice™ is essentially a four deep FIFO in the A-bus to B-bus direction and a buffer in the B-bus to A-bus direction. Address or data information is strobed into the Write Buffer Slice™ FIFO on the rising edge of **CLK** when qualified by **EN#**. In many systems **CLK** may be connected to the processor **CLK** signal. Two flags indicate FIFO status in an address mode part: **EF#** is low when the FIFO is empty, and **FF#** is low when the FIFO is full. A full FIFO should indicate to the control logic that a write cannot be buffered and thus **EN#** should not be driven. The empty flag, **EF#**, signals to the control logic that the FIFO is empty; either a DMA or a pending CPU read may occur, or the system bus should be idle. Complete flexibility is allowed in the architecture to support posted I/O writes, non-posted memory regions, copy-back and write-through cache configurations and different processor types.

In most systems the **SHLDA/DIR** pin must be driven by the control logic for the data mode parts. It must not change during a system write operation or data to the system will change from registered to real-time. In most systems **SHLDA/DIR** may be tied to the system W/R# signal driven by the Write Buffer Slice™ control logic. For address mode parts the **SHLDA/DIR** pin can be tied to the system HLDA signal, again driven by the control logic.

The **NEXT#** input may be tied to the system ADS# (SADS#) signal for all WB41x parts in the system. SADS# is generated by the Write Buffer Slice™ control logic for CPU reads and writes to the system. The Write Buffer Slice™ will ignore any **NEXT#** pulses if it is empty. **BP/BE1** input to address mode parts are driven by the control logic. This signal allows the address mode part to bypass the Write Buffer Slice™ internal FIFO so that addresses may be presented to the system on a read operation without the delay of having to pass through the registers.

Table 1: Typical Write Buffer Slice™ Combinations for selected CPUs

CPU	Address	Data	Control
386 SX	2	1	1 PAL
386 DX	2	2	1 PAL
80486	2	2	1 PAL
i860	2	4	1 PAL
68040/030	2	2	1 PAL

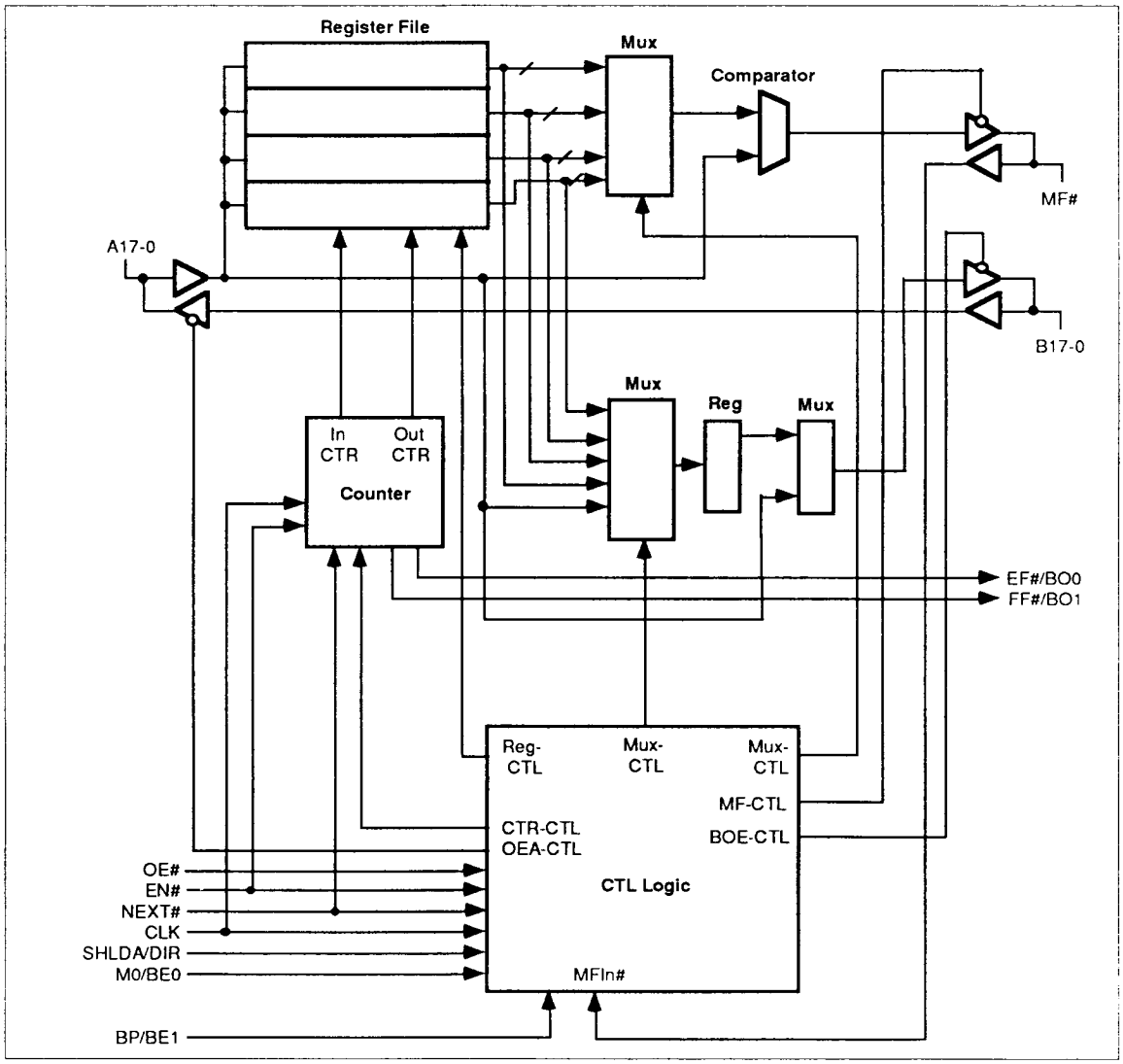


Figure 2.1: Write Buffer Slice™ Block Diagram

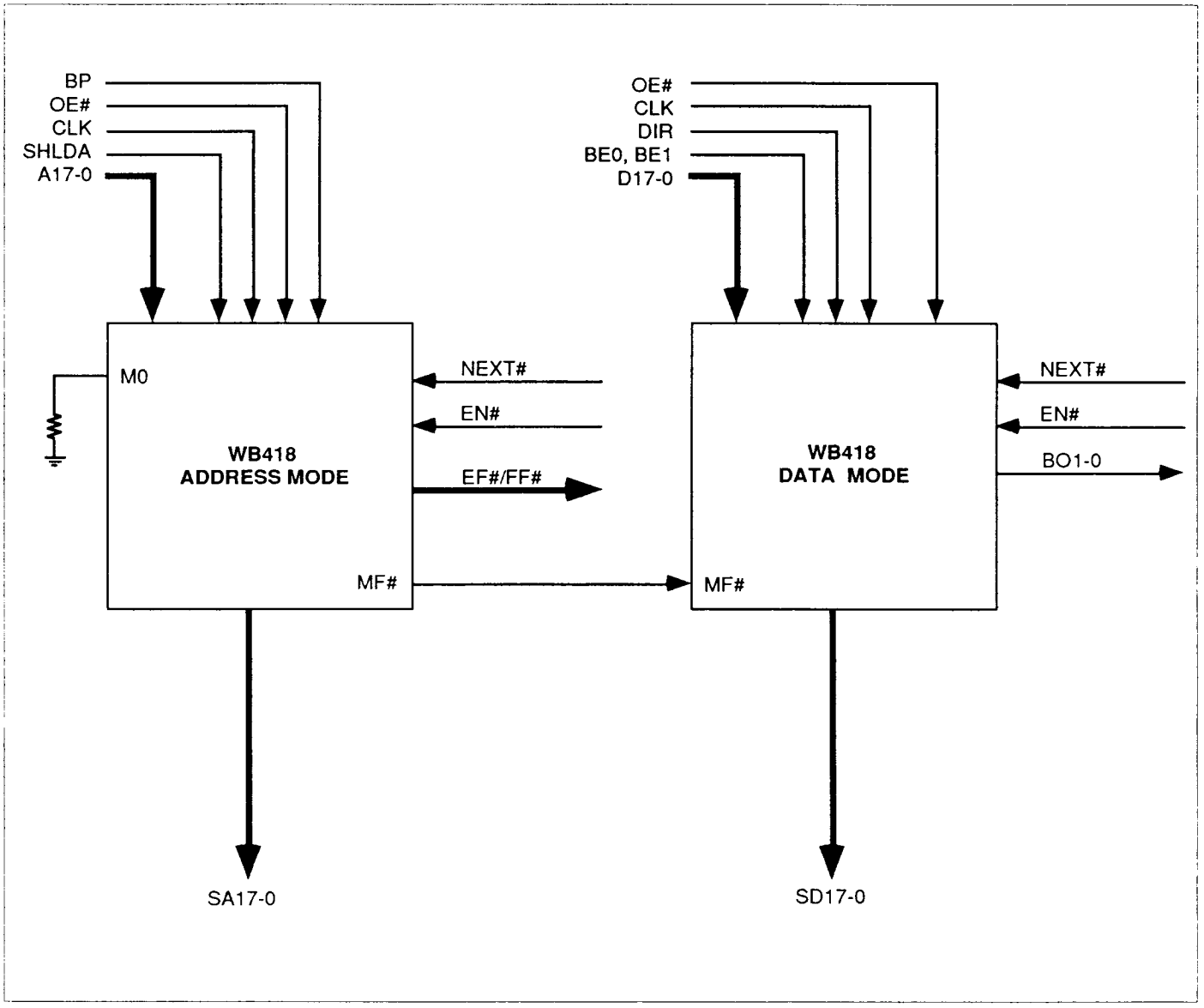


Figure 2.2: Address and Data Mode Pin Out

3. CPU INTERFACE

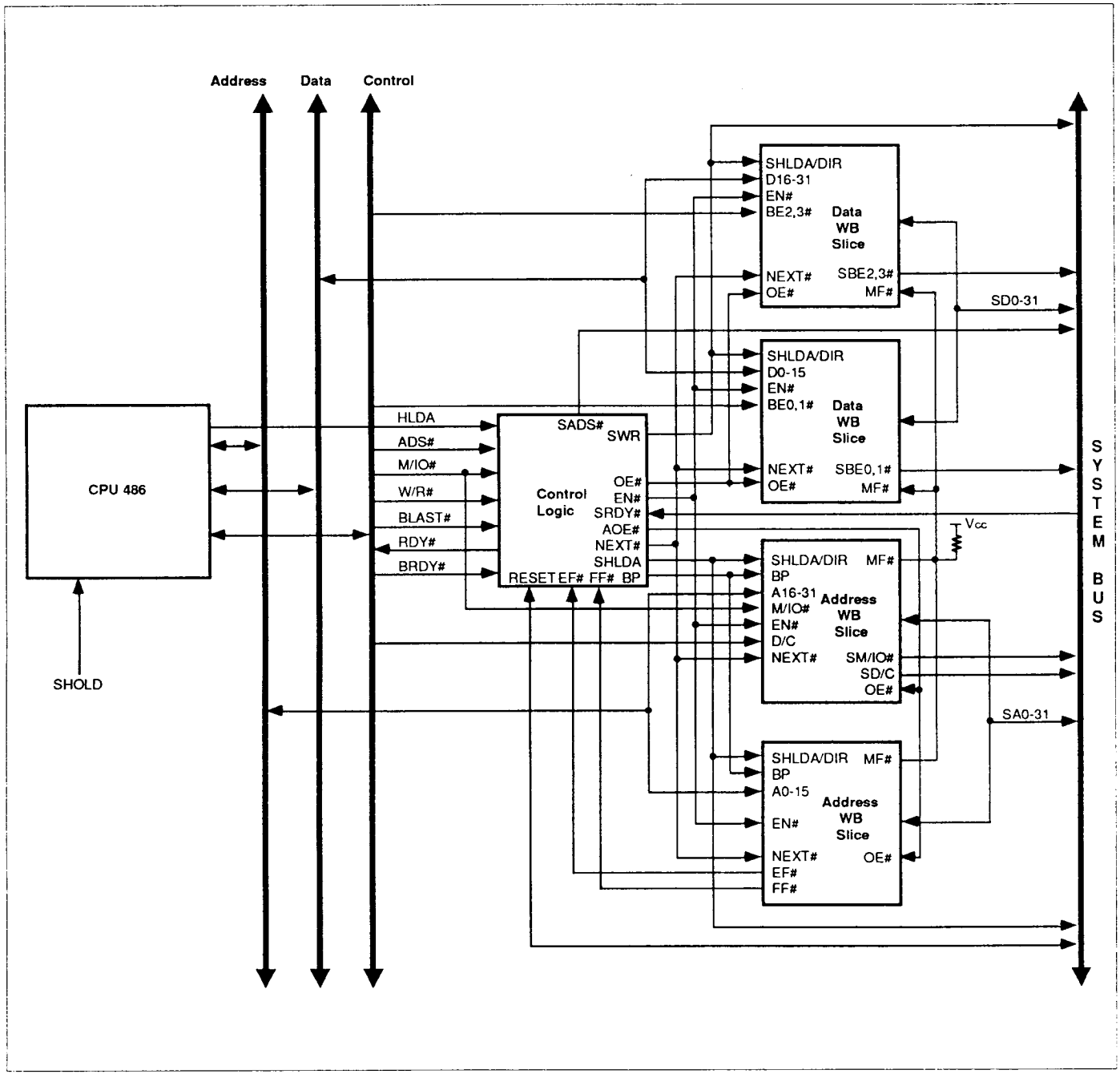


Figure 3.1: Write Buffer Slice™ CPU Interface

4. PIN DESCRIPTION

4.1 WB 416 - PQFP52

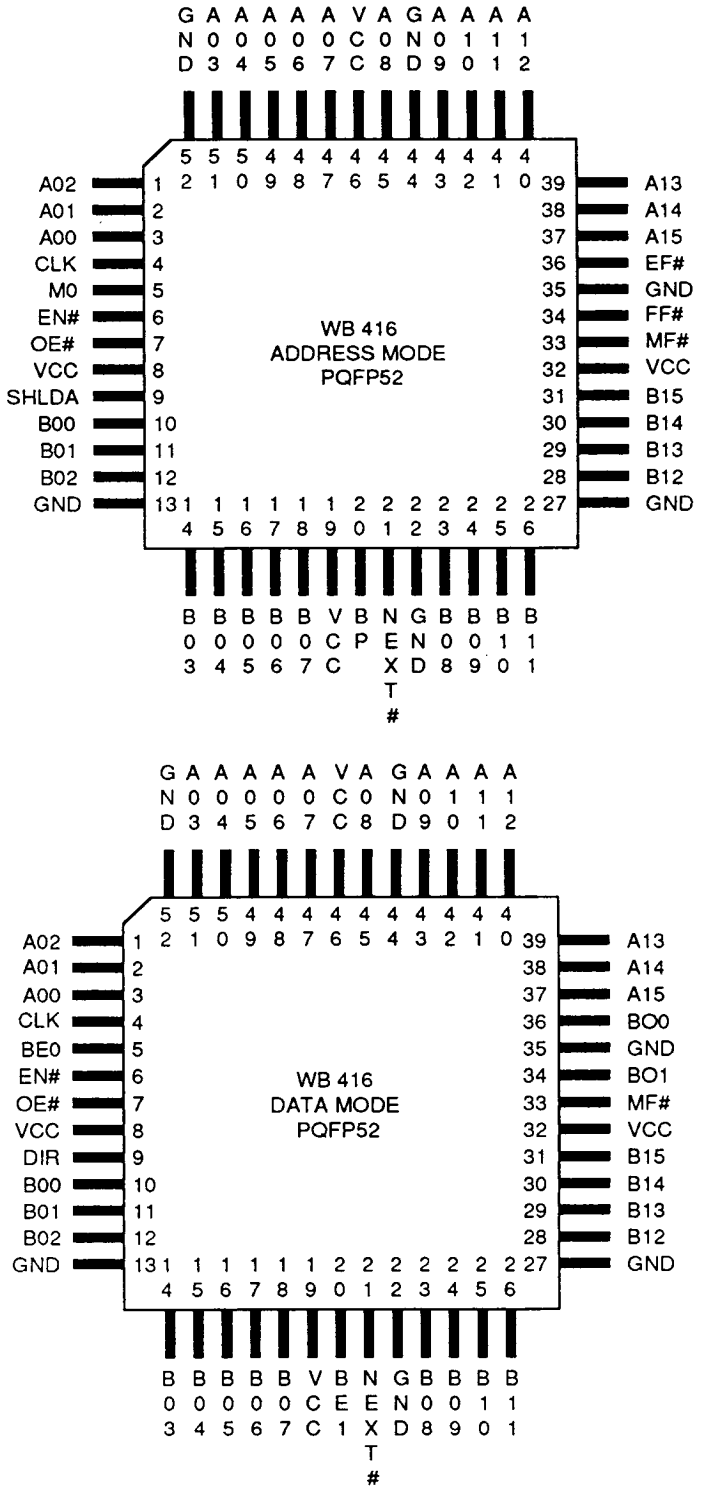


Figure 4.1: Write Buffer Slice™ 16-Bit Pin Out

4.2 WB 418 - PQFP64

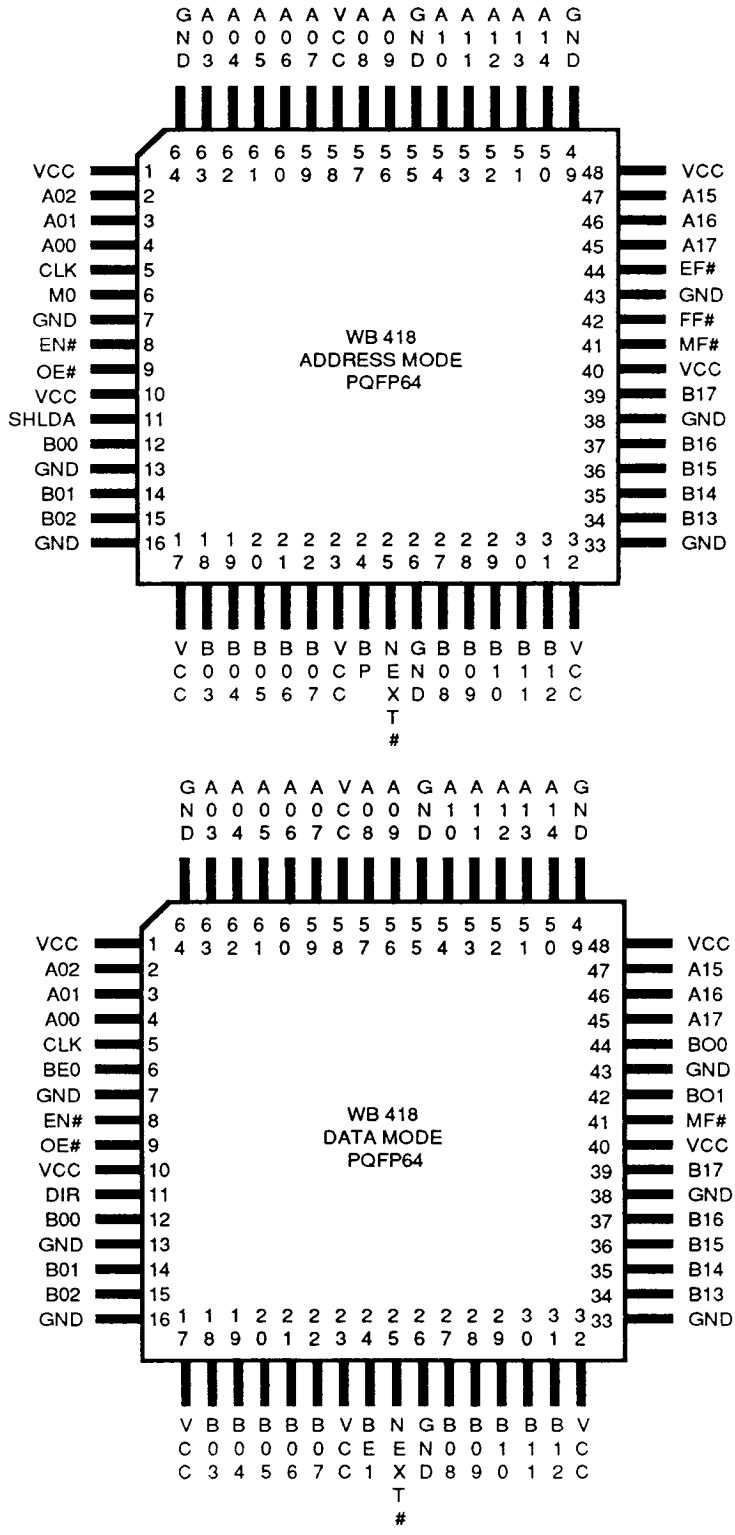


Figure 4.2: Write Buffer Slice™ 18-Bit Pin Out

4.3 Pin Description - Address Mode

Signal	Type	Description
A00-A15 (WB 416) A00-A17 (WB 418)	Input/Output Input/Output	**CPU side input/output.** In Address mode these are connected to the CPU address lines. During CPU read and writes these lines are inputs. In hold state these lines should be outputs.
B00-B15 (WB 416) B00-B17 (WB 418)	Input/Output Input/Output	**System side input/output**. These are used as system address. They are driven with next address in FIFO when **NEXT#** is asserted. Real-time A-bus address is propagated to B-bus when **BP** is asserted.
M0	Input with Internal Pullup	**Mode Bit 0 during reset.** Must be tied low in Address mode.
BP	Input with Internal Pullup	**BP- Address bypass in Address mode.** **BP** when low, allow address from FIFO to be outputs on B-bus pins. When high provides real-time data from A-bus pins to B-bus outputs. When **BP** is asserted **NEXT#** is not required for addresses to become valid on the B-bus.
EF#	Tri-state Output	**Empty Flag**. The Empty flag is activated from the rising edge **CLK** when **NEXT#** is low. It is deasserted from the rising edge of **CLK** when **EN#** is active.
FF#	Tri-state Output	**Full Flag.** The full flag is activated from the rising edge of **CLK** when **EN#** is low. It is deasserted from the falling edge of **NEXT#**.
CLK	Input	**Write Buffer input strobe signal**. The address, data and control signals are strobed into the FIFO on the rising edge of this signal when **EN#** is asserted. If **BP** is asserted then the address is not strobed into the FIFO. In most systems this pin is driven by the CPU clock.
EN#	Input	**Qualification for CLK**. Normally this signal is driven by the control logic. This signal is active low. It should be asserted during CPU writes. It must be kept deasserted at all times in which the data is not required to be loaded in to the FIFO.

4.3 Pin Description - Address Mode (Continued)

Signal	Type	Description
NEXT#	Input	**Output FIFO address to system**. This signal is driven by the control logic. When driven active (low) the next data/ address in the write buffer FIFO is presented on the system side of the write buffer (B00-17). When NEXT# is asserted while OE# is deasserted the device is reset.
OE#	Input	**Enable outputs.** A high level on this pin forces all A-bus and B-bus outputs to a Tri-state mode. This is independent of all operating modes. When this pin is high and NEXT# is driven low the device is reset to the empty state and mode pins are sampled.
SHLDA	Input	**Direction control**. In Address mode a low level enables addresses from A-bus to B-bus while a high level enables addresses from B-bus to A-bus. In Address mode it is normally connected to SHLDA.
MF#	Open Collector (Drain) Match Fail output	**Output in Address mode.** Sampled by Data mode parts and driven by Output Address mode parts to determine if combining may be done. When the Write Buffer Slice™ is in Data mode a high level on this pin allows the data at the inputs to be combined with the last data written to the buffer into a single entry with the next CLK and EN# active signals. The byte enable inputs are used to determine the bytes or Words to be combined. When in Address mode this pin will be driven low if the address at the inputs does not match the previous address, indicating a match fail. In Data mode this pin is sampled with CLK and EN# to combine writes in the write buffer. All MF# pins of the Address and Data mode parts should be tied together with an appropriate pull-up resistor.

4.4 Pin Description - Data Mode

Signal	Type	Description
A00-A15 (WB 416) A00-A17 (WB 418)	Input/Output Input/Output	**CPU side data**. These are connected to the CPU data lines. During CPU writes these lines are inputs. During CPU reads these lines are outputs. In hold state these lines should be tri-state.
B00-B15 (WB 416) B00-B17 (WB 418)	Input/Output Input/Output	**System side data**. These are used as system data. They are driven when NEXT# is asserted.
BE0	Input with Internal Pullup	**Byte enable corresponding to A00-A07 data bits**. High during reset forces the part into the Data mode. Must be tied low in Address mode.
BE1	Input with Internal Pullup	**BE1 - Byte enable corresponding to data bits 8-15 on the A-bus.**
BO0,1	Tri-state Output	**Byte enable output**. The BO0,1 are propagated from A-bus to B-bus even when DIR indicates flow from B-bus to A-bus for instance in CPU reads. For CPU writes they are driven from the FIFO.
CLK	Input	**Write Buffer input strobe signal**. The address, data and control signals are strobed into the FIFO on the rising edge of this signal when EN# is asserted. In most systems this pin is driven by the CPU clock.
EN#	Input	**Qualification for CLK**. Normally this signal is driven by the control logic. This signal is active low. It should be asserted during CPU writes. It must be kept deasserted at all times in which the data is not required to be loaded in to the FIFO.
NEXT#	Input	**Enable Output of next write data and address to system**. This signal is driven by the control logic. When driven active (low) the next data/address in the write buffer FIFO is presented on the system side of the write buffer (B00-17). When NEXT# is asserted while OE# is deasserted the device is reset.
OE#	Input	**Enable outputs.** A high level on this pin forces all A-bus and B-bus outputs to a Tri-state mode. This is independent of all operating modes. When this pin is high and NEXT# is driven low the device is reset to the empty state and mode pins are sampled.
DIR	Input	**Direction control**. A high level on this pin enables data flow from A-bus to B-bus. A low enables data flow from B-bus to A-bus when DIR is low. The BO0,1 direction is not changed, the CPU BE# is propagated from A-bus to B-bus. It is normally connected to SW/R#.

4.4 Pin Description - Data Mode (Continued)

Signal	Type	Description
MF#	**Match Fail Input**	**Input in Data mode.** Sampled by Data mode parts and driven by Output Address mode parts to determine if combining may be when the Write Buffer Slice™ is in Data mode a high level on this pin allows the data at the inputs to be combined with the last data written to the buffer into a single entry with the next **CLK** and **EN#** active signals. The byte enable inputs are used to determine the bytes or Words to be combined. In Data mode this pin is sampled with **CLK** and **EN#** to combine writes in the write buffer. All **MF#** pins of the Address and Data mode parts should be tied together with an appropriate pull-up resistor.

4.5 Control Signals Operation

Table 4.5 Control Signals Operation

Signals	EN#	CLK	NEXT#	BP	SHLDA /DIR	OE#	OPERATION
ADDRESS Mode	L	↑	H	L	L	L	Address from A-B strobed into FIFO.
	H	↑	H	L	L	L	B-bus driven with previous address.
	H	X	↓	L	L	L	Output next address in FIFO onto B-bus.
	H	X	H	H	L	L	Output real-time address from A-bus to B-bus
	H	X	H	L	H	L	Output real-time B-bus to A-bus.
	L	↑	↓	NA	L	L	Address on A-bus strobed into FIFO. Next address on FIFO output on B-bus.
	H	X	L	L	X	H	Reset part.
DATA Mode	L	↑	H	NA	H	L	Data on A-bus strobed into FIFO.
	H	X	↓	NA	H	L	Next data in FIFO output onto the B-bus.
	H	X	H	NA	L	L	Real-time B-bus data to A-bus.
	H	X	H	NA	X	H	Outputs on A- and B-bus tri-stated.
	H	X	L	L	X	H	Reset part.
	L	↑	↓	NA	L	L	BE#/Data on A-bus strobed into FIFO. Next Data/BE# onto FIFO output on B-bus.
BEx#	L	↑	H	NA	L	L	BE# on A-bus strobed into FIFO.
	H	X	↓	NA	L	L	Next BE# in FIFO output on B-bus.
	H	X	H	NA	H	L	Real-time BE# on A-bus propagated to B-bus.
	L	↑	↓	NA	L	L	BE#/Data on A-bus strobed into FIFO. Next Data/BE# onto FIFO output on B-bus.

5. FUNCTIONAL DESCRIPTION

5.1 Byte Gathering

The Byte Gathering capability of the Write Buffer Slice™ allows consecutive bytes written by the CPU to be combined into a single word. If four consecutive bytes are written by the CPU then they are combined into a Dword (32-bit word).

The Byte Gathering functions of the part require certain implementation restrictions. The processor must be in non-pipelined mode and the data and byte enables must be connected in the proper order. In the 80386DX and 80486 systems there will be a total of four Write Buffer Slices™, two in Address mode and two in Data mode.
One Data mode part should be connected to data byte 0 and 1 with **BE0** and **BE1** with the second Data mode part connected to bytes 2 and 3 with **BE2** and **BE3**.

If the Byte Gathering function is not to be used, the **MF#** pins of all devices should be grounded.

The Write Buffer Slice™ architecture supports the gathering of byte and word writes into a single double word or word write. In order to perform this function the address of the words must be the same. Each Address mode part continuously compares the last written address still in the buffer with the address on its A-bus input pins. If the comparison is not identical the Match Fail output is asserted.

Table 5.1 Examples: (**BE3#-BE0#** shown, address is identical)

First	Second	Result	Notes
1110	1101	1100	
1100	0011	0000	
1110	1001	1000	
1000	0111	0000	
1000	1011	1000	Intentional overwrite of Byte 2
0011	1100	0000	
0011	1110	0010	
1011	1110	1010	Non-continguous bytes in same Dword
1011	0110	0010	
1011	0111	0011	
1101	1011	1001	

Note that intentional data overwrites can occur which replace one or more bytes of previously written data. If there are regions of the memory address space which cannot tolerate this (i.e. some peripheral device is memory mapped) the **MF#** signal should be driven low on these addresses. The same addresses generally cannot be cached as well.

The table below summarizes normal system operation.

Table 5.2: Normal System Operation

CPU Function	Operation
Memory Write	Data and Address are strobed into the Write Buffer Slice™ on **CLK** if **EN#** is asserted.
Memory Read	Data is propagated from the system side inputs (B-bus) to the CPU side outputs (A-bus). Address is propagated from A-bus to B-bus (**BP** is asserted). Control logic should wait for the Write Buffer Slice™ to empty before initiating the read operation on the system bus.
I/O Write	Data and Address are strobed into the Write Buffer Slice™ on **CLK** as qualified by **EN#**. The control logic should wait for the Write Buffer Slice™ to empty before strobing this write.
I/O Read	Data is propagated from the system side inputs (B-bus) to the CPU side outputs (A-bus). Control logic should wait for the Write Buffer Slice™ to empty before initiating the read operation on the system bus.
INTA/Special	Data is propagated from the system side inputs (B-bus) to the CPU side outputs (A-bus). Control logic should wait for the Write Buffer Slice™ to empty before initiating the INTA operation on the system bus.
DMA	Data is Tri-stated (data **OE#** High). Address is propagated from B-bus to A-bus to allow for snoops (**SHLDA/DIR=1**). Write Buffer must always be emptied before a system bus is given up to another master.

5.2 System Coherency Considerations

In most systems using the Write Buffer Slice™ there will be some type of cache associated with the CPU. In the case of the 80486 this may be the internal cache or a secondary cache such as the Matra MDS415/395e. In the case of the 80386DX there will be an external cache such as the MDS395e. These cache controllers will be required to "snoop" the bus operation to allow another master (i.e. DMA) to invalidate a cache line, or in the case of a copy-back cache, to provide modified data to the bus master. The **SHLDA/DIR** pin allows addresses to flow from the B-bus side of the Write Buffer Slice™ to the A-bus side and the cache controller. Note that the Write Buffer Slice™ must always be emptied before the system or bus master is given a hold acknowledge in order to maintain coherency of data.

DMA Function	Operation
DMA Write	Direct address to cache controller for line invalidation. Support copy-back if required.
DMA Read	Direct address to cache controller if copy-back supported. Provide read data if cache snoop hit in copy-back system.

6. DC SPECIFICATIONS (T_A=0°C to +70°C; V_{DD}=5V± 5%; V_{SS}=0)

V_{DD} level with reference to V_{SS}	-1V to +6.5V
Minimum voltage on any other pin	-1V
Maximum voltage on any other pin	V_{DD}+1V
Storage temperature	-65°C to +150°C
Case Temperature under bias	-65°C to +110°C

6.1 DC Specifications (Continued)

Symbol	Description	Min	Max	Unit	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	-	V	I_{OH}=-12mA
V_{OL}	Output LOW Voltage	-	0.5	V	I_{OL}=12mA
V_{IH}	Input HIGH Voltage	2.0	-	V	-
V_{IL}	Input LOW Voltage	-	0.8	V	-
I_{ILP}	Input PullUp Leakage Current	+50	+350	uA	V_{IN}=V_{SS}
I_{IL}	Input Leakage Current	-10	+10	uA	V_{IN}=V_{SS}
I_{OZ}	Output Leakage Current	-10	+10	uA	V_{SS}<V_{OUT}<V_{DD}
I_{CSB}	Standby Current	-	15	mA	V_{DD}=Max; V_{IN}=GND Outputs Open
I_{DD}	Power Supply Current	-	20	mA	V_{DD}=Max; V_{IN}=GND Outputs Open f_{OP}=1MHz
C_{IN}	Input Capacitance	-	5	pF	Note 1
C_{IO}	Output Capacitance	-	5	pF	Note 1

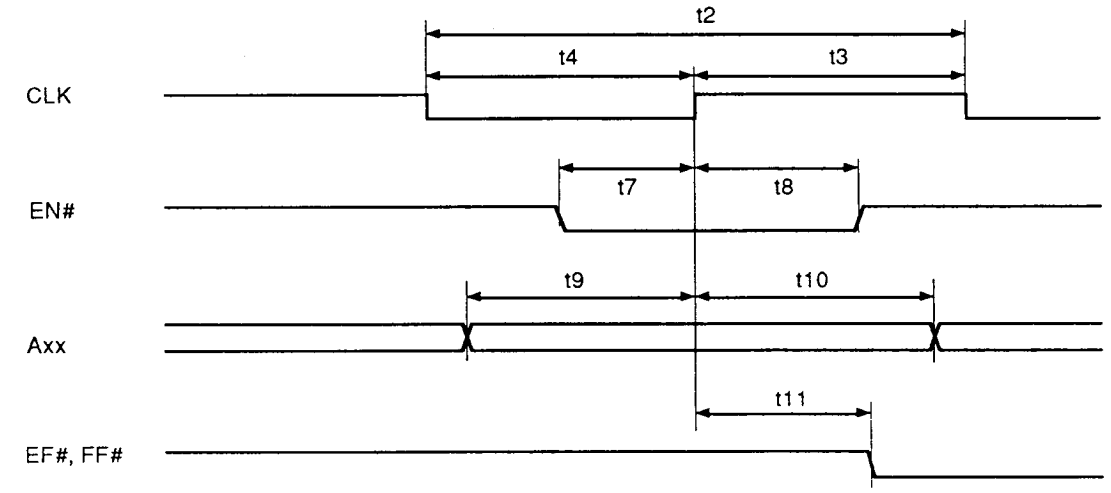
Note 1: Guaranteed by design and verified by characterization. Not tested in production.

7. AC SPECIFICATIONS (T_A=0°C to +70°C; V_{DD}=5V±5%; V_{SS}=0)

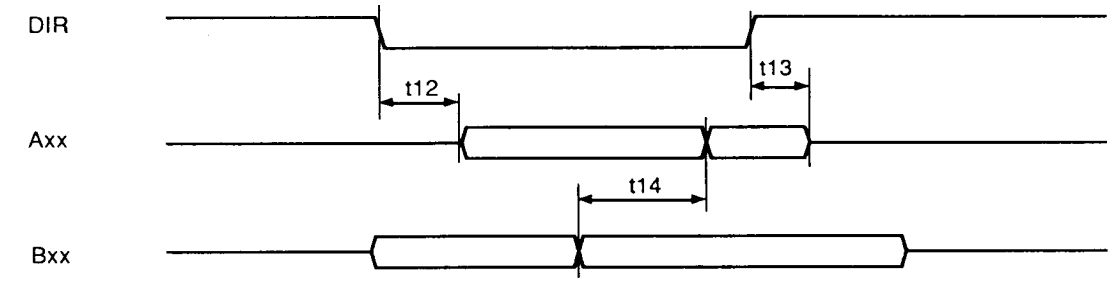
Symbol	Description	20 MHz		33 MHz		50 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
t1	Clock Frequency		20		33.33		50	MHz	
t2	Clock Period	50		30		20		ns	
t3	Clock High Time	16		11		7		ns	
t4	Clock Low Time	16		11		7		ns	
t5	Clock Rise Time		6		3		2	ns	.8V to 2V
t6	Clock Fall Time		6		3		2	ns	2V to .8V
t7	EN# Setup to CLK	32		19		11.50		ns	
t8	EN# Hold Time	3		3		2		ns	
t9	A-Bus Setup to CLK	17		11		5		ns	
t10	A-Bus Hold Time	3		3		2		ns	Would Always Change After T2
t11	Flag Delay from CLK		27		15		11	ns	
t12	Output Enable Time from DIR Data Mode		26		14		7.5	ns	
t13	Output Disable Time from DIR Data Mode		35		20		14.5	ns	
t14	B-Bus to A-Bus Prop. Delay Data Mode		14		10		7	ns	
t15	BP high to B-bus Valid Address Mode		26		14		7.50	ns	
t16	A-bus to B-bus Prop. Delay Address Mode		14		10		6	ns	
t17	MF# Input Setup to CLK		22		12		10	ns	
t18	MF# Input Hold from CLK	3		3		2		ns	
t19	MF# Output Valid Delay from A-Bus		20		18		15	ns	
t20	NEXT# Pulse Width	25		15		10		ns	
t21	B-Bus Output Valid from NEXT# Fall	4	16	3	13	2	10	ns	
t22	Flag Delay from CLK Rise		25		15		11	ns	

7.1 CPU Interface Timings

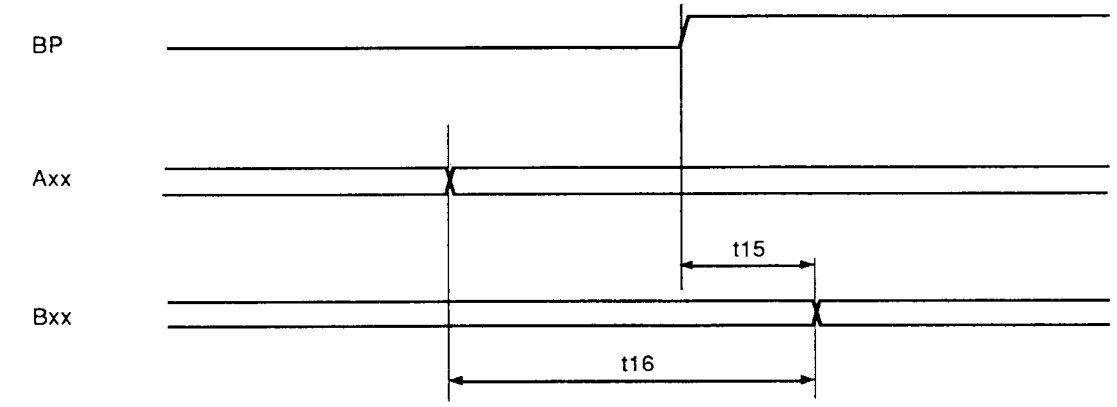
CPU WRITE TIMINGS



CPU READ TIMINGS (DATA MODE)

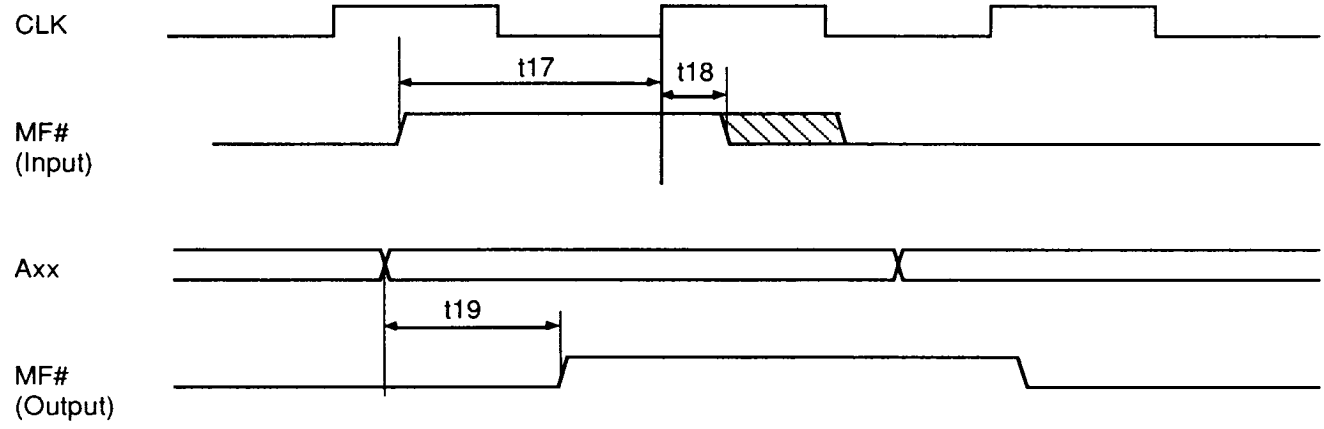


CPU READ TIMINGS (ADDRESS MODE)

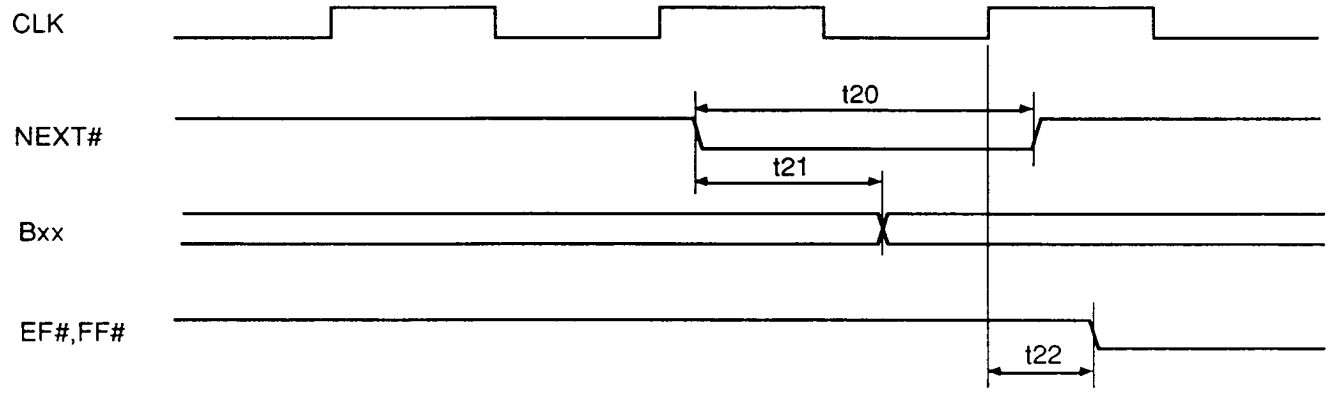


7.2 System Interface Timings

MF# INPUT/OUTPUT TIMING



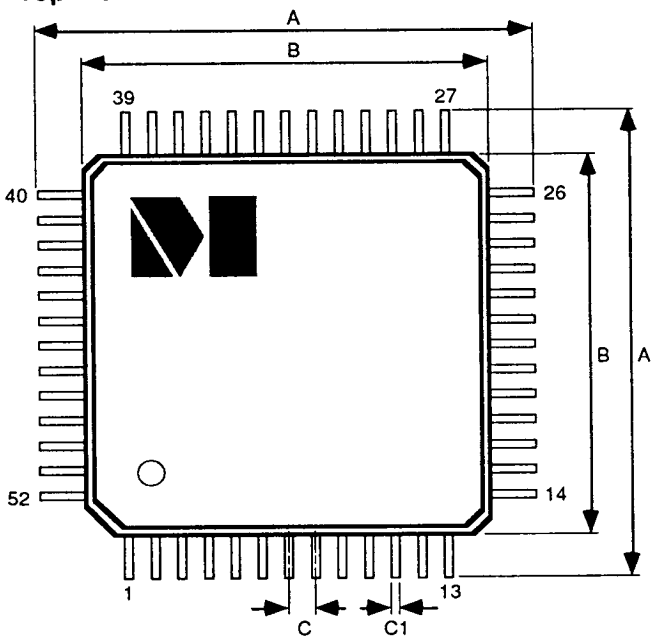
SYSTEM SIDE TIMING



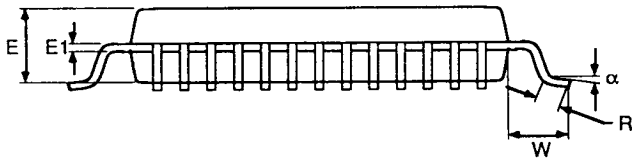
8. PACKAGE

8.1 52-Pin WB 416

Top View

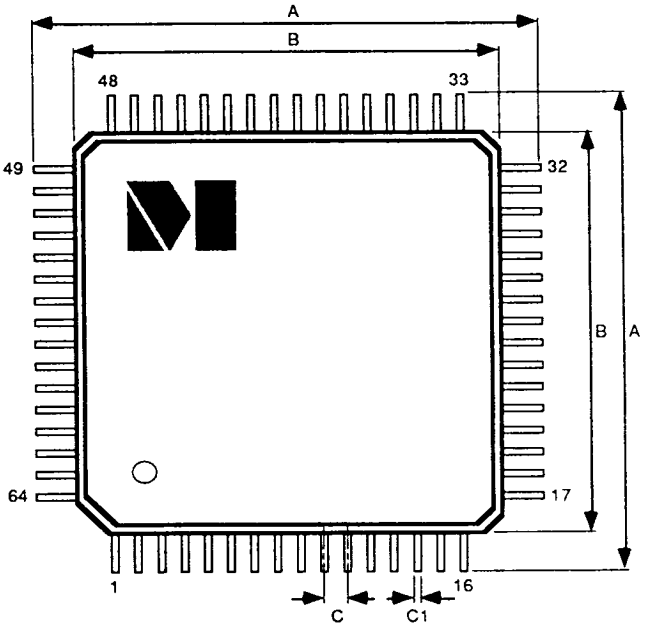


Front View

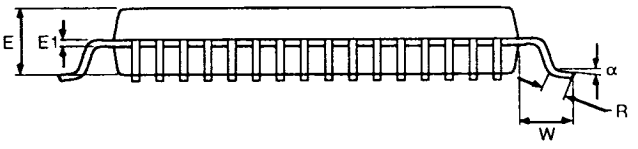


8.2 64-Pin WB 418

Top View



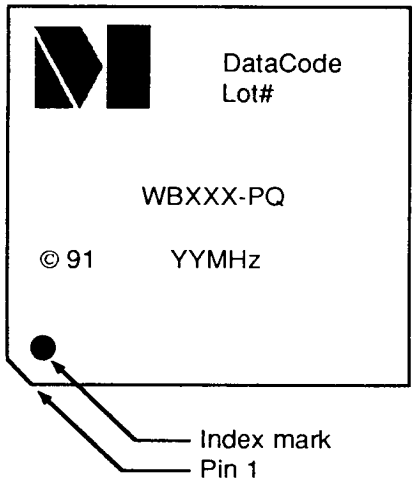
Front View



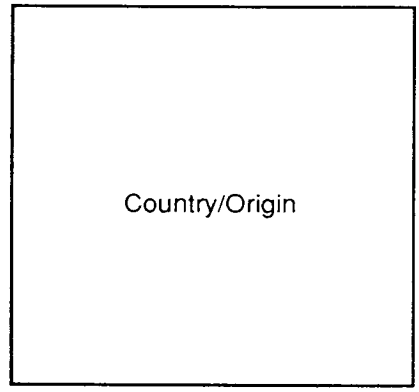
Symbol	WB 416				WB 418			
	Inches		Millimeters		Inches		Millimeters	
	Min	Max	Min	Max	Min	Max	Min	Max
A	0.677	0.709	17.2	18.0	0.645	0.677	16.4	17.2
B	0.543	0.559	13.8	14.2	0.543	0.056	13.8	14.2
C	0.035	0.043	0.90	1.10	0.027	0.035	0.69	0.89
C1	0.008	0.02	0.20	0.50	0.008	0.02	0.20	0.50
E	0.102	0.110	2.60	2.80	0.102	0.110	2.60	2.80
E1	0.004	0.008	0.10	0.20	0.004	0.008	0.10	0.20
R	0.019	0.043	0.50	1.10	0.012	0.036	0.30	0.90
α	0°	12°	0°	12°	0°	12°	0°	12°
W	- - -	0.71	- - -	1.80	- - -	0.055	- - -	1.40

9. MARKING INFORMATIONS

Top View



Bottom View



Notes:
1. XXX = 416 or 418.
2. YY = 20, 33, or 50 MHz.

10. ORDERING INFORMATIONS

Package	Speed	P/N
52-pin PQFP Package	20 MHz	WB 416-PQ-20
52-pin PQFP Package	33 MHz	WB 416-PQ-33
52-pin PQFP Package	50 MHz	WB 416-PQ-50
64-pin PQFP Package	20 MHz	WB 418-PQ-20
64-pin PQFP Package	33 MHz	WB 418-PQ-33
64-pin PQFP Package	50 MHz	WB 418-PQ-50

11. REVISION HISTORY

The following table reflects key modifications in successive versions of Write Buffer Slice™ data sheet.

Document	Date	Description of Change
WB/r1.0/1291	December 1991	Original Document.

NOTES