WD1100-05 Parallel/Serial Converter

DESCRIPTION

The WD1100-05 Parallel/Serial Converter allows the user to convert a byte of data to a serial stream when writing to a disk or any serial device. Parallel data is entered via the D0-D7 lines on the rising edge of $\overline{DCLK}$. A synchronous BYTE counter is used to signify that 8-bits of data have been shifted out and that the 8-bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.

The WD1100-05 is implemented in NMOS silicon gate technology and is available in a 20-pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5 M BITS/SEC SHIFT RATE
- TRI-STATE OUTPUT CONTROL
- PARALLEL IN/SERIAL OUT
- 20 PIN DIP PACKAGE

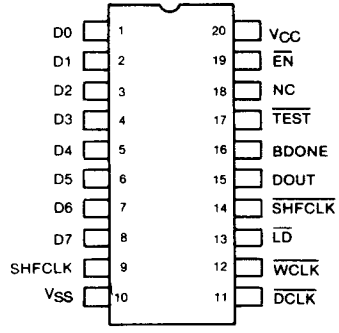

Figure 1.
WD1100-05 Pin Connections

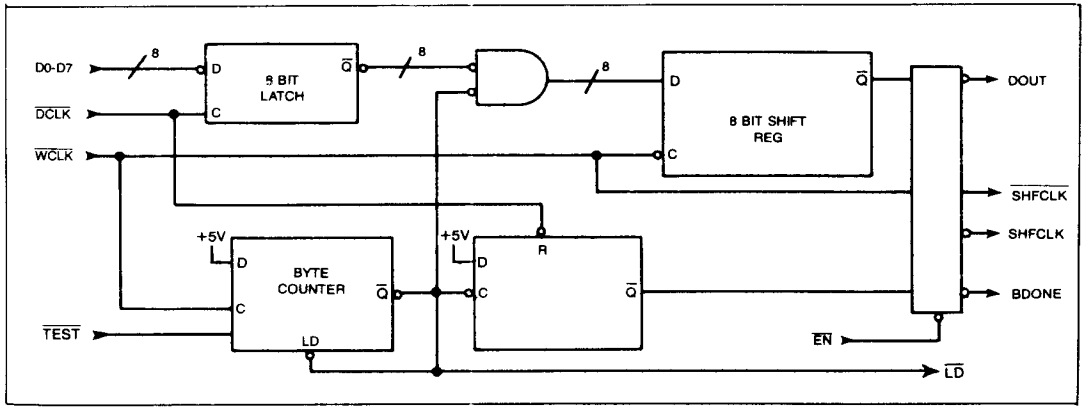

Figure 2.
WD1100-05 Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1-8	D0-D7	DATA 0-DATA 7	8-bit parallel data inputs (bit 7 = MSB).
9	SHFCLK	SHIFT CLOCK	Inverted copy of $\overline{\text{WCLK}}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0.
10	V_{SS}	GROUND	GROUND.
11	$\overline{\text{DCLK}}$	$\overline{\text{DATA CLOCK}}$	Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8-bit latch.
12	$\overline{\text{WCLK}}$	$\overline{\text{WRITE CLOCK}}$	The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (module 8).
13	$\overline{\text{LD}}$	$\overline{\text{LOAD}}$	This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user.
14	$\overline{\text{SHFCLK}}$	$\overline{\text{SHIFT CLOCK}}$	Delayed copy of $\overline{\text{WCLK}}$ (pin 12) which is active when EN (pin 19) is at a logic 0.
15	DOUT	DATA OUT	Serial data output enabled by EN (pin 19).
16	BDONE	BYTE DONE	This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data.
17	$\overline{\text{TEST}}$	$\overline{\text{TEST INPUT}}$	This pin must be left open by the user.
18	NC	No Connection	
19	$\overline{\text{EN}}$	$\overline{\text{ENABLE}}$	This active low signal enables DOUT, $\overline{\text{SHFCLK}}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state.
20	V_{CC}	V_{CC}	+5 ± 10% power supply input.

DEVICE DESCRIPTION

Prior to loading the WD1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. EN (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of DCLK (pin 11). DCLK also resets BDONE (pin 16). The first BDONE that comes up simply means that the WD1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th WRITE CLOCK pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the WD1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low (↓) transition of the WCLK (pin 12). The low-to-high (↑) transition of WCLK increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 WCLK cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, $\overline{\text{SHFCLK}}$, and SHFCLK, can be placed in a high impedance state by setting EN (pin 19) to a logic 1. Likewise, EN must be at a logic 0 in order for these signals to drive any external device.

The $\overline{\text{TEST}}$ pin is internally OR'ed with the counter output to produce the LD (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{\text{TEST}}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias . . . . . 0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS} . . . . . -0.2V to +7.0V
Power Dissipation . . . . . 1 Watt
STORAGE TEMPERATURE
PLASTIC . . . . . -55°C (-67°F) to + 125°C (257°F)
CERAMICS . . . . . -55°C (-67°F) to + 150°C (302°F)

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics: T_A = 0°C (32°F) to 50°C (122°F), V_{CC} = ±5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 200 μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Ouputs Open
I_{IH}	Current Input High			<10	μA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	μA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics: T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = + 5 ± 10% V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
^tWC	WCLK frequency			5.25	MHZ	50% duty cycle
^tDW	DCLK pulse width	50			nsec	
^tDS	Data set-up w.r.t. ↑ DCLK	30			nsec	
^tDH	Data hold time w.r.t. ↑ DCLK	50			nsec	
^tDB	↓ DCLK to ↓ BDONE			160	nsec	EN = 0
^tDO	↓ WCLK to DOUT			130	nsec	EN = 0
^tSH	↓ WCLK to ↓ SHFCLK			75	nsec	EN = 0
^tHS	↑ WCLK to ↑ SHFCLK			70	nsec	EN = 0
^tWB	↑ $\overline{WCLK}$ to ↑ BDONE			180	nsec	EN = 0
^tES	↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE			90	nsec	
^tCL	↑ $\overline{WCLK}$ to ↓ $\overline{LD}$			150	nsec	

NOTES: 1. Typical Values are for T_A = 25°C (77°F) and V_{CC} = + 5.0V

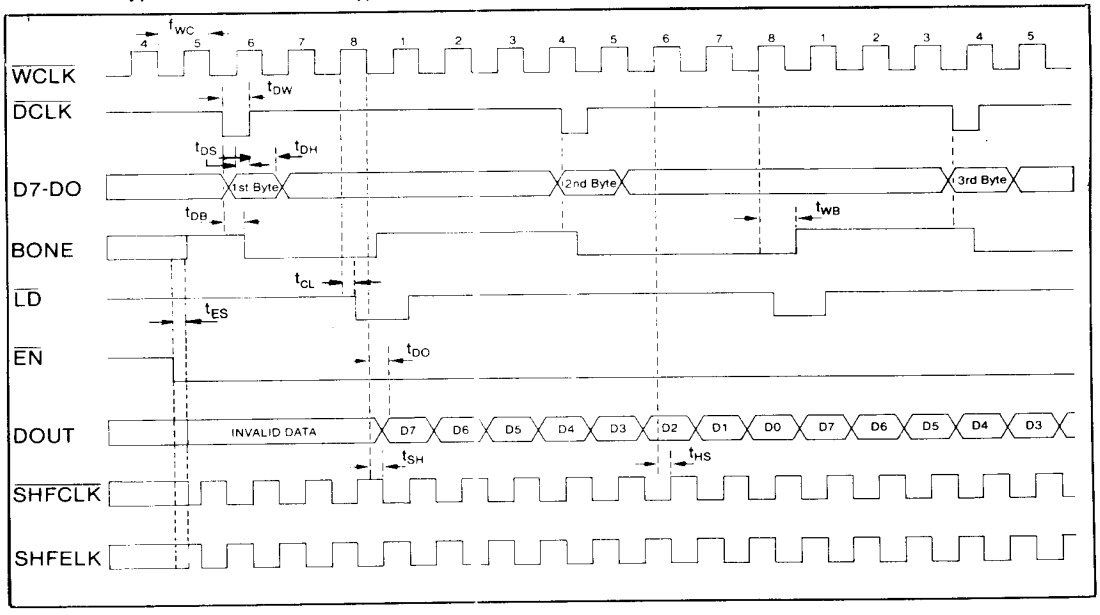

Figure 3.
WD1100-05 Functional Timing Diagram