WD1100-01 Serial/Parallel Converter

DESCRIPTION

The WD1100-01 Serial/Parallel Converter allows the user to convert NRZ (non-return to zero) data from a Winchester disk drive into 8-bit parallel form. Additional inputs are provided to signal the start of the parallel process, as well as Byte Strobes to signify the end of the conversion. The device contains two sets of 8-bit registers; one register may be read (in parallel), while data is being shifted into the other register. This double-buffering allows the Host to read data from the disk drive at one-eighth the actual data rate.

The WD1100-01 is implemented in NMOS silicon gate technology and is available in a 20 pin plastic or ceramic dual-in-line package.

FEATURES

- SINGLE +5V SUPPLY
- DOUBLE BUFFERING
- BYTE STROBE OUTPUTS
- 5MBITS/SEC SHIFT RATE
- SERIAL IN/SERIAL-PARALLEL OUT
- 20 PIN DIP PACKAGE

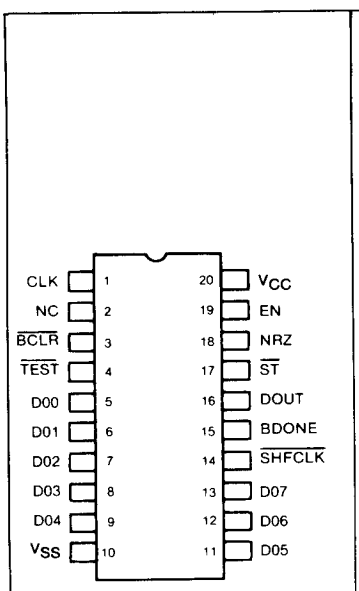

Figure 1.
WD1100-01 Pin Connections

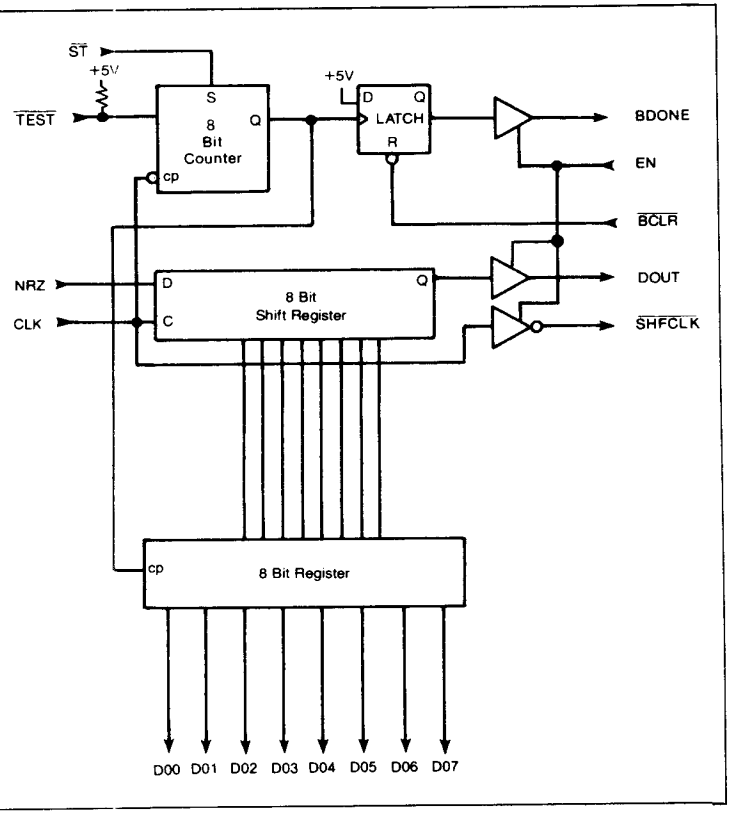

Figure 2.
WD1100-01 Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	CLK	CLOCK	NRZ data is entered into the 8-bit shift register on the low-to-high transition of clock.
2	NC	NO CONNECTION	No connection. This pin is to be left open by the user.
3	$\overline{BCLR}$	$\overline{BYTE\ CLEAR}$	When this line is at a logic 0, the BDONE (Pin 15) line is held reset.
4	$\overline{TEST}$	$\overline{TEST\ INPUT}$	This pin must be left open by the user.
5-9 11-13	D00-D07	DATA0-DATA 7	8 bit parallel data outputs.
10	V_{SS}	GROUND	Ground.
14	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	Inverted copy of CLOCK (pin 1) which is active when EN (pin 19) is at a logic 1.
15	BDONE	BYTE DONE	This signal is forced to a logic 1 signifying 8 bits of data have been assembled. BDONE remains in a logic 1 state until reset by a logic 0 on the BCLR (pin 3) line.
16	DOUT	DATA OUT	Serial Data Output from the 8th stage of the internal shift register. DOUT is in a high impedance state whenever EN (pin 19) is at a logic 0.
17	$\overline{ST}$	$\overline{START}$	This line enables the byte counter and is used for synchronization. It must be held to a logic 1 prior to first data bit on the NRZ (pin 18) line.
18	NRZ	NRZ DATA	NRZ serial data is entered on this pin and clocked by the low to high transition of CLK (pin 1).
19	EN	ENABLE	When this signal is at a logic 0, DOUT, $\overline{SHFCLK}$, and BDONE outputs are in a high impedance state.
20	V_{CC}	V_{CC}	$+5V \pm 10\%$ power supply input.

DEVICE DESCRIPTION

Prior to shifting data through the device, the WD1100-01 must be synchronized to the data stream. The $\overline{ST}$ line (Pin 17 high) is used to hold the internal bit counter in a cleared state until valid data (NRZ) and clocks (CLK) are entered. The $\overline{ST}$ line is a synchronous input and therefore requires one full cycle of the CLK line (Pin 1) to occur in order to accept a $\overline{ST}$ condition. After this happens, the device is ready to perform serial to parallel conversions.

Data is entered on the NRZ line and clocked into the 8-bit shift register on the low-to-high transition of CLK. The $\overline{ST}$ line must be set low during the low time of CLK. Data is accepted on low-to-high transition of the clock while the high-to-low transition of CLK increments the bit counter. After 8 data bits have been entered the final high-to-low transition of CLK sets an internal latch tied to the BDONE line (Pin 15). At the same time, the contents of the shift register are parallel loaded into an 8 bit register making the parallel data available on the D00-D07 outputs. BDONE will remain in a latched state until the BCLR is set to a logic 0, clearing off the BDONE signal. $\overline{BCLR}$ is a level triggered input and must be set back to a logic 1 before the next 8 bits are shifted through the register. BCLR has no effect on the serial shifting process. When the next 8 bits are received, BDONE will again be set and the operation continues.

When interfacing to a microprocessor, BDONE is used to indicate a parallel byte is ready to be read. As the processor reads the data out of the D00-D07 lines, the $\overline{BCLR}$ line should be strobed to clear of BDONE in anticipation of the next assembled byte. An address decode signal generated at the host may be used for this purpose. During a power-up condition, the state of BDONE is indeterminant. It is recommended that $\overline{BCLR}$ be strobed low after power-up to insure that BDONE is cleared.

The serial output line from the last stage of the shift register is available on the DOUT pin. An inverted copy of CLK is available on the $\overline{SHFCLK}$ pin. Both DOUT (Pin 16) and $\overline{SHFCLK}$ (Pin 14) can be used to drive another shift register external to the device.

The three signals BDONE, DOUT, and $\overline{SHFCLK}$ can be placed in a high impedance state by setting EN (Pin 19) to a logic 0. Likewise, EN must be at a logic 1 in order for these signals to be active.

The $\overline{TEST}$ pin is internally OR'ed with the $\overline{ST}$ line to inhibit the bit counter. It is recommended that $\overline{TEST}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required internally for proper device operation.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias .....0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS} .....−0.2V to +7.0V
Power Dissipation.....1 Watt
STORAGE TEMPERATURE
PLASTIC ...−55°C (−67°F) to +125°C (257°F)
CERAMIC ..−55°C (−67°F) to +150°C (302°F)

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = + 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_O	Output Low Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Outputs Open
I_{IH}	Input High			<10	μA	V_{IN} = .4 to V_{CC}
I_{IL}	Input Low			<10	μA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F), V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
f_{CL}	CLK FREQUENCY	0		5.25	MHZ	
t_{LS}	↓CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{HS}	↑CLK to $\overline{ST}$	0			nsec	$\overline{ST}$ = 1 (min 200nsec)
t_{DS}	Data set-up to ↑ CLK	15			nsec	
t_{VB}	BDONE valid from ↓ CLK	65		140	nsec	EN = 1
t_{RS}	BDONE reset from $\overline{BCLR}$			135	nsec	EN = 1
t_{BW}	$\overline{BCLR}$ Pulse Width	50			nsec	EN = 1
t_{SC}	↑ CLK to ↓ $\overline{SHFCLK}$			90	nsec	EN = 1
t_{CS}	↓ CLK to ↑ $\overline{SHFCLK}$			90	nsec	EN = 1
t_{SD}	Data delay from ↑ $\overline{SHFCLK}$			55	nsec	EN = 1
t_{FO}	Enable to DOUT ACTIVE			90	nsec	
t_{DH}	Data Hold w.r.t. ↑ CLK	45			nsec	
t_{CD}	↑ CLK to DOUT ACTIVE			145	nsec	
t_{OF}	Enable to DOUT disable			90	nsec	

NOTE: 1. Typical Values are for T_A = 25°C (77°F) and V_{CC} = +5V ± 10%

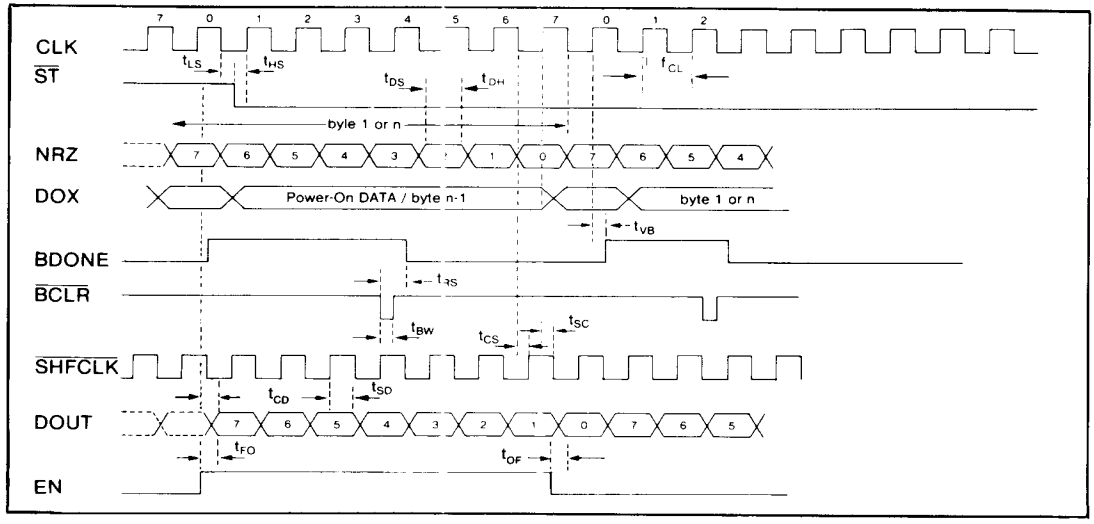

FIGURE 3. WD1100-01 FUNCTIONAL TIMING