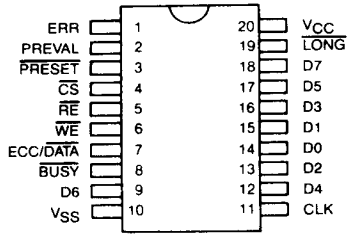
WD11C00-13 ECC Support Device

FEATURES

- 32-BIT COMPUTER SELECTED POLYNOMIAL
- PARALLEL INPUT AND OUTPUT
- DATA TRANSFER RATES UP TO 5 MBITS/SEC
- RECORD LENGTH UP TO 1038 BYTES INCLUDING CHECK BYTES
- TTL, MOS COMPATIBLE
- 20 PIN DIP PACKAGE
- CMOS TECHNOLOGY
- SINGLE + 5 VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD11C00-13 ECC Support Device is designed to provide ECC capabilities for Winchester Disk Controllers and accommodates data transfer rates up to 5 Mbits/sec. Data is transferred into and out of the WD11C00-13 via an 8-bit, bi- directional parallel data port.

The WD11C00-13 performs several operations including ECC byte generation, error detection, and error syndrome generation. Additionally, the WD11C00-13 supports user diagnostics by allowing transparent ECC byte transfers between the Host and disk medium.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	ERR	ERROR	O	This signal is valid only when the Byte Counter reaches the end of the syndrome bytes. Asserted indicates a non-zero syndrome, or the syndrome has not yet been generated. In the Long mode, ERR will be de-asserted at the completion of each ECC byte, but is of no meaning.
2	PREVAL	PRESET VALUE	I	PREVAL asserted presets the ECC accumulator to FFFFFFFF, and when de-asserted, presets the accumulator to B517894A. It is an asynchronous signal and enabled when $\overline{\text{PRESET}}$ is asserted and $\overline{\text{LONG}}$ de-asserted.
3	$\overline{\text{PRESET}}$	$\overline{\text{PRESET}}$	I	$\overline{\text{PRESET}}$ asserted and $\overline{\text{LONG}}$ de-asserted enables PREVAL.
4	$\overline{\text{CS}}$	$\overline{\text{CHIP SELECT}}$	I	$\overline{\text{CS}}$ asserted enables $\overline{\text{WE}}$ or $\overline{\text{RE}}$.
5	$\overline{\text{RE}}$	$\overline{\text{READ ENABLE}}$	I	When asserted, data is written to or ECC and Syndrome bytes read from the accumulator.
6	$\overline{\text{WE}}$	$\overline{\text{WRITE ENABLE}}$	I	When asserted, data and ECC bytes are written to the accumulator.
7	ECC/$\overline{\text{D}}$	ECC/$\overline{\text{DATA}}$	I	When $\overline{\text{DATA}}$ is asserted, data is written to the accumulator and ECC bytes are generated. When ECC is asserted, polynomial control logic is inhibited. ECC and syndrome bytes are transferred to or from the accumulator.
8	$\overline{\text{BUSY}}$	$\overline{\text{BUSY}}$	O	WD11C00-13 asserts $\overline{\text{BUSY}}$ while performing any function other than $\overline{\text{PRESET}}$.
9	D6	DATA BIT 6	I/O	This signal is bit 6 of an 8-bit, bi-directional, data bus.
10	V_{SS}	GROUND		Ground.
11	CLK	CLOCK	I	5 MHZ clock used for internal timing (see text for additional explanation).
12	D4	DATA BIT 4	I/O	This signal is bit 4 of an 8-bit, bi-directional data bus.
13	D2	DATA BIT 2	I/O	This signal is bit 2 of an 8-bit, bi-directional data bus.
14	D0	DATA BIT 0	I/O	This signal is bit 0 (LSB) of an 8-bit, bi-directional data bus.
15	D1	DATA BIT 1	I/O	This signal is bit 1 of an 8-bit, bi-directional data bus.
16	D3	DATA BIT 3	I/O	This signal is bit 3 of an 8-bit, bi-directional data bus.
17	D5	DATA BIT 5	I/O	This signal is bit 5 of an 8-bit, bi-directional data bus.
18	D7	DATA BIT 7	I/O	This signal is bit 7 (MSB) of an 8-bit, bi-directional data bus.
19	$\overline{\text{LONG}}$	$\overline{\text{LONG}}$	I	$\overline{\text{LONG}}$ is asserted when Long Mode is selected. This signal inhibits $\overline{\text{PRESET}}$, as well as ECC and Syndrome byte generation.
20	V_{CC}	POWER SUPPLY		+5V Power Supply

ARCHITECTURE

The WD11C00-13 is composed of an accumulator and necessary timing and control logic, to generate four ECC or Syndrome bytes. The generation process can be inhibited, allowing the WD11C00-13 to appear transparent to the four additional bytes that follow the end of data written to or read from the disk during READLONG or WRITELONG operations. The major blocks of the WD11C00-13 are shown in Figure 1.

Accumulator

The accumulator consists of a 32-bit serial, ring shift register. Access to this register is byte serial via the most significant byte. Due to the configuration of the register, an 8-bit byte requires only four clocks to shift to the next byte position.

The WD11C00-13 operates as a destructive read out. As each ECC or Syndrome byte is read out, it is replaced with zeros. Hence, as the last ECC or Syndrome byte is read, the accumulator is reset.

The content of the WD11C00-13 is altered by any of the following events:

1. Presetting to FFFFFFFF or B517894A with the $\overline{\text{PRESET}}$ and PREVAL input signals.
2. Passing data through the device to produce four ECC bytes (i.e. writing data to the disk).
3. Passing data and ECC bytes through the device to produce and hold a syndrome (i.e. reading data from the disk).
4. Writing only the ECC bytes into the device with no data (i.e. WRITELONG to, or READLONG from the disk, create a transparent effect on the ECC character).

Polynomial Control

The polynomial $X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$ is the same as that used in other Western Digital devices. ECC and Syndrome generation is initiated during data transfer by asserting $\overline{\text{DATA}}$ (ECC/$\overline{\text{DATA}}$). Polynomial logic is inhibited as the ECC and Syndrome bytes are read by asserting ECC (ECC/$\overline{\text{DATA}}$).

Preset Generator

$\overline{\text{PRESET}}$ and PREVAL are asynchronous inputs which do not require $\overline{\text{CS}}$ or Clock asserted. They provide a means of presetting the ECC register to FFFFFFFF or B517894A. When $\overline{\text{WE}}$ is asserted before the address mark (A 1F8) is read. $\overline{\text{PRESET}}$ and PREVAL are asserted prior to the device being selected. This presets the ECC register to FFFFFFFF. As the first data byte is reached, the polynomial control logic will have generated ECC bytes B517894A.

When an application calls for not passing the address mark (A 1F8) through the WD11C00-13, $\overline{\text{PRESET}}$ is asserted and PREVAL de-asserted before the device is selected. This presets the ECC register to B517894A, the same configuration that is reached when the address mark is read. In this manner, compatibility between drives is maintained.

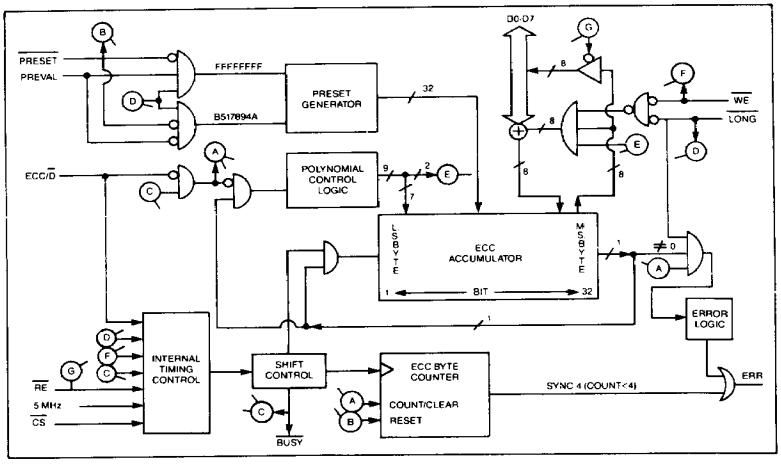


FIGURE 1. WD11C00-13 FUNCTIONAL BLOCK DIAGRAM

Byte Counter

As the ECC or Syndrome bytes are written into or read out of the accumulator, ECC (ECC/DATA) is asserted. This initiates the Byte Counter. The counter is incremented once for each byte and used internally to indicate when all 4 bytes (Sync 4) have been written or read. It is also used to control ERR timing and WE. The counter is reset synchronously during data transfer or asynchronously by asserting PRESET.

Error Logic

ERR is de-asserted only when the Byte Counter has reached the count of four (SYNC 4) and the Syndrome is equal to zero, or the device is in the long mode.

Internal Timing

With the exception of PRESET and PREVAL functions all operations are performed under control of the external 5 MHz clock. The internal timing is initiated by the following signals:

$\overline{CS}$ $\overline{BUSY}$ $\overline{RE}$ $\overline{WE}$ ECC/$\overline{DATA}$ $\overline{LONG}$ SYNC 4

When the device is selected for either a Read or Write function in the normal mode, the clocks function throughout the entire data transfer. When the WD11C00-13 is selected during WRITELONG mode, the clocks do not start until the ECC bytes from the Host or disk is reached (indicated by ECC/DATA). The clocks stop when the fourth byte has been counted.

When the WD11C00-13 is selected during READLONG mode, the clocks do not start until the ECC bytes previously loaded are sent to the Host or disk. The clocks continue as long as Read functions are requested, even if more than four ECC bytes have been called for.

LONG MODE COMMANDS

When in the Long Mode, PRESET can not be asserted, thus protecting the contents of the Accumulator from being altered by anything other than ECC bytes.

For diagnostic purposes, it is not desirable to generate ECC or Syndrome bytes on the data being passed between the Host and disk. Instead, the WD11C00-13 allows the ECC bytes to pass through unaltered. To accomplish this, READLONG and WRITELONG commands are provided. The three significant inputs used to accomplish this are LONG, WE and ECC/DATA, with LONG being the primary control.

While in the Long Mode with data on the bus, no internal clocks can be generated. Therefore, no data can be written into the Accumulator or ECC bytes produced. The content on the Accumulator remains unchanged from its Preset Value.

When the first of the ECC bytes is placed on the data bus, ECC (ECC/DATA) is asserted. With LONG inhibiting the polynomial control logic from functioning, the clocks are initiated and this byte, along with the next three, are written into the Accumulator unchanged. As stated in the clock description, after the fourth byte is written into the WD11C00-13 the clocks stop, preventing the destruction of the ECC bytes by additional Write functions.

Reading the ECC bytes from the WD11C00-13 is much the same as in WRITELONG, with the following exception. as each byte is read out, its location is reset to zero and the clock continues to run as long as RE is asserted.

SUMMARY

When writing to the WD11C00-13 during Long Mode, the polynomial and preset functions are inhibited and the clocks cannot run after the fourth byte. This protects the ECC bytes, making the device appear transparent.

When reading from the WD11C00-13 during Long Mode, ECC generation and preset functions are inhibited. The clocks can continue to run after the fourth byte, making it possible to supply the Host or disk with as many zeros as needed to fill the allotted space. This decision is controlled by the Host.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATING

V_{CC} with respect to V_{SS} (ground) . . . . . + 7V

Voltage on any pin with respect to V_{SS} . . . . . -0.3 to V_{CC} + 0.3 volts

Operating temperature . . 0°C (32°F) to 70°C (185°F)

Storage Temperature . . . . -65°C (-85°F) to 150°C (302°F)

NOTE:

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

TABLE 1. DC OPERATING CHARACTERISTICS

T_A = 0°C (32°F) to 70°C (158°F); V_{SS} = OV, V_{CC} = +5V ± .25V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100uA
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
I_{CC}	Supply Current			10	mA	In active state
				100	μA	In rest state

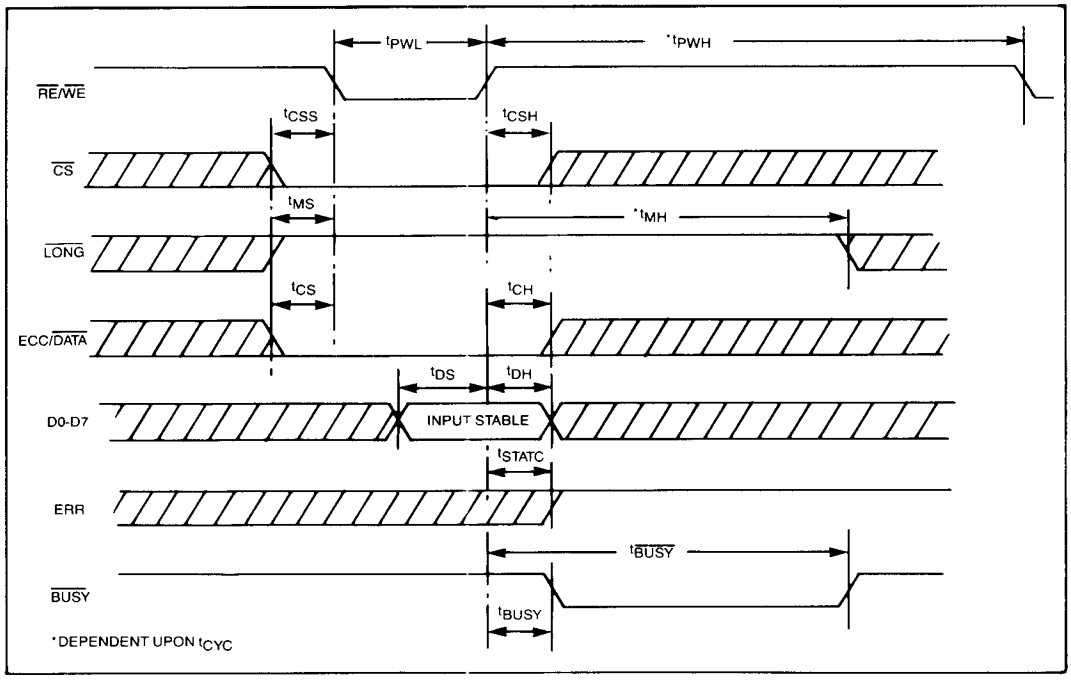


FIGURE 2. DATA INPUT TIMING

TABLE 2. DATA INPUT TIMING

All Units in nsec.

SYMBOL	CHARACTERISTIC	MIN	MAX	TYP
t_{PWL}	$\overline{RE}/\overline{WE}$ Pulse Width Low	124		
t_{PWH}	$\overline{RE}/\overline{WE}$ Pulse Width High	4T + 235*		
t_{CSS}	$\overline{CS}$ Setup to Leading Edge of $\overline{RE}/\overline{WE}$	10		
t_{CSH}	$\overline{CS}$ Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	0		
t_{MS}	Mode Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	14		
t_{MH}	Mode Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	4T + 115*		
t_{CS}	Control Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	33		
t_{CH}	Control Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	37		
t_{DS}	Data Input Setup to Trailing Edge of $\overline{RE}/\overline{WE}$	40		
t_{DH}	Data Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	20		
t_{STATC}	Accumulator ≠ 0 to High Level After Trailing Edge of $\overline{RE}/\overline{WE}$		40	
$t_{\overline{BUSY}}$	$\overline{BUSY}$ Output to High Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
t_{BUSY}	$\overline{BUSY}$ to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		85	
t_{CYC}	Clock Cycle Period	180		

*T = t_{CYC}

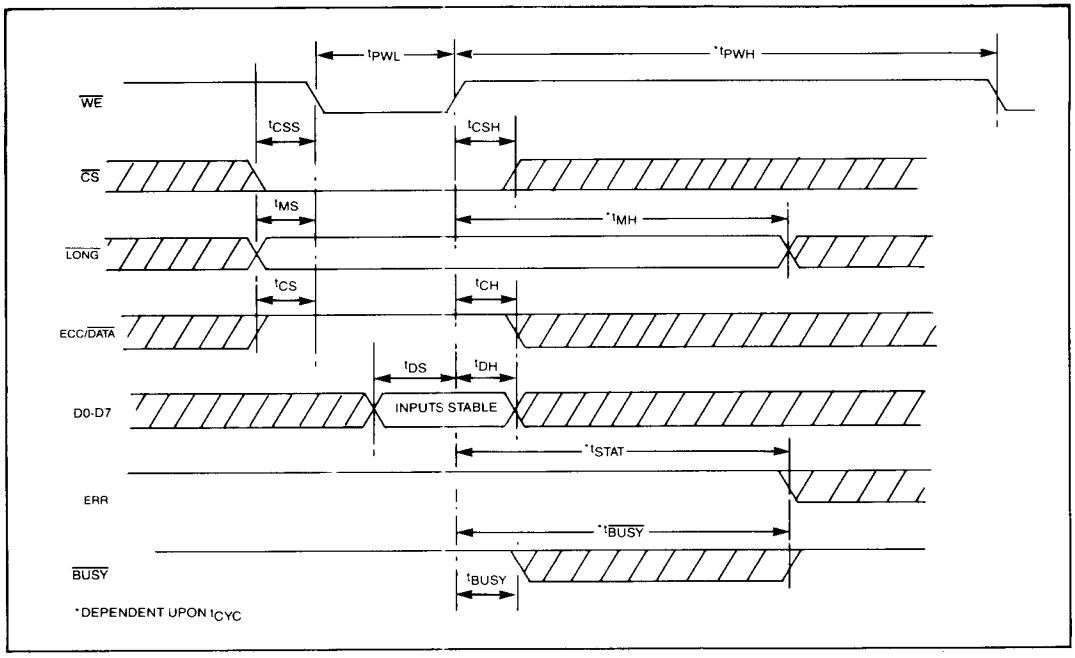


FIGURE 3. ECC BYTE INPUT TIMING

TABLE 3. ECC INPUT TIMING All Units in nsec.

SYMBOL	CHARACTERISTIC	MIN	MAX	TYP
^tPWL	$\overline{RE}/\overline{WE}$ Pulse Width Low	124		
^tPWH	$\overline{RE}/\overline{WE}$ Pulse Width High	4T + 235*		
^tCSS	$\overline{CS}$ Setup to Leading Edge of $\overline{RE}/\overline{WE}$	10		
^tCSH	$\overline{CS}$ Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	0		
^tMS	Mode Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	14		
^tMH	Mode Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	4T + 115*		
^tCS	Control Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	33		
^tCH	Control Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	37		
^tDS	Data Input Setup to Trailing Edge of $\overline{RE}/\overline{WE}$	40		
^tDH	Data Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	20		
^tSTAT	Accumulator ≠ 0 to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
$^t\overline{BUSY}$	$\overline{BUSY}$ Output to High Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
^tBUSY	$\overline{BUSY}$ to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		50	
^tCYC	Clock Cycle Period	180		

*T = ^tCYC

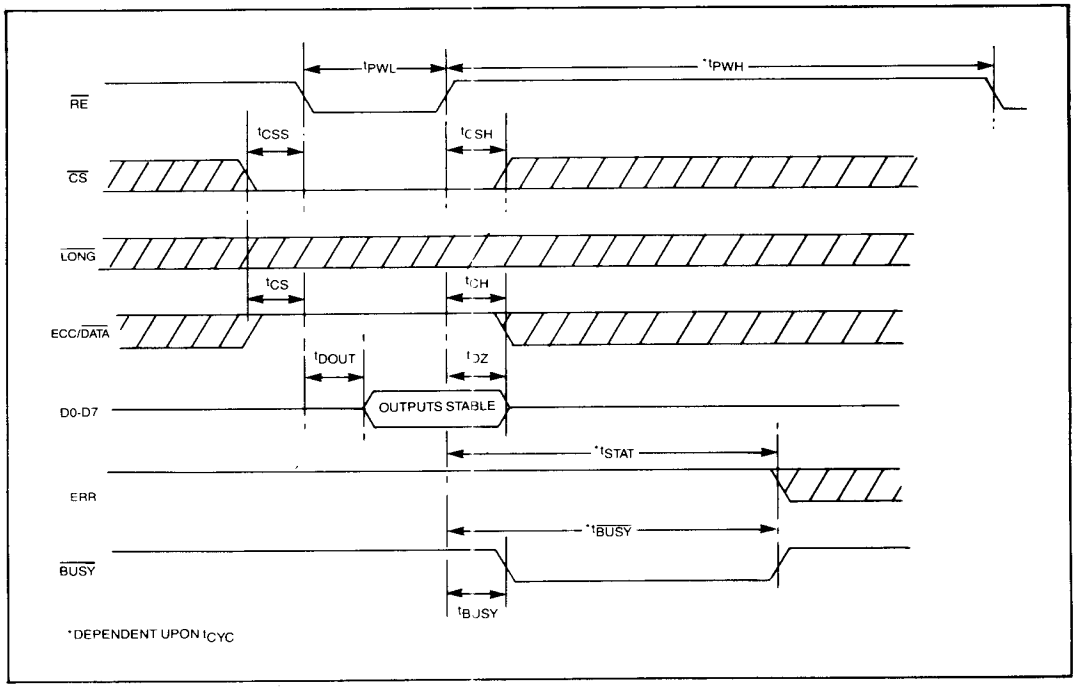


FIGURE 4. DEVICE OUTPUT TIMING

TABLE 4. DEVICE OUTPUT TIMING All Units in nsec.

SYMBOL	CHARACTERISTICS	MIN	MAX	TYP
t_{PWL}	$\overline{RE}/\overline{WE}$ Pulse Width Low	124		
t_{PWH}	$\overline{RE}/\overline{WE}$ Pulse Width High	4T + 235*		
t_{CSS}	$\overline{CS}$ Setup to Leading Edge of $\overline{RE}/\overline{WE}$	10		
t_{CSH}	$\overline{CS}$ Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	0		
t_{CS}	Control Input Setup to Leading Edge of $\overline{RE}/\overline{WE}$	33		
t_{CH}	Control Input Hold After Trailing Edge of $\overline{RE}/\overline{WE}$	37		
t_{DOUT}	Data Output Valid After Leading Edge of $\overline{RE}$		50	
t_{DZ}	Data Bus Float After Trailing Edge of $\overline{RE}$		60	
t_{STAT}	Accumulator ≠ 0 to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
$t_{\overline{BUSY}}$	$\overline{BUSY}$ Output to High Level After Trailing Edge of $\overline{RE}/\overline{WE}$		4T + 165*	
t_{BUSY}	$\overline{BUSY}$ to Low Level After Trailing Edge of $\overline{RE}/\overline{WE}$		50	
t_{CYC}	Clock Cycle Period	180		

*T = t_{CYC}

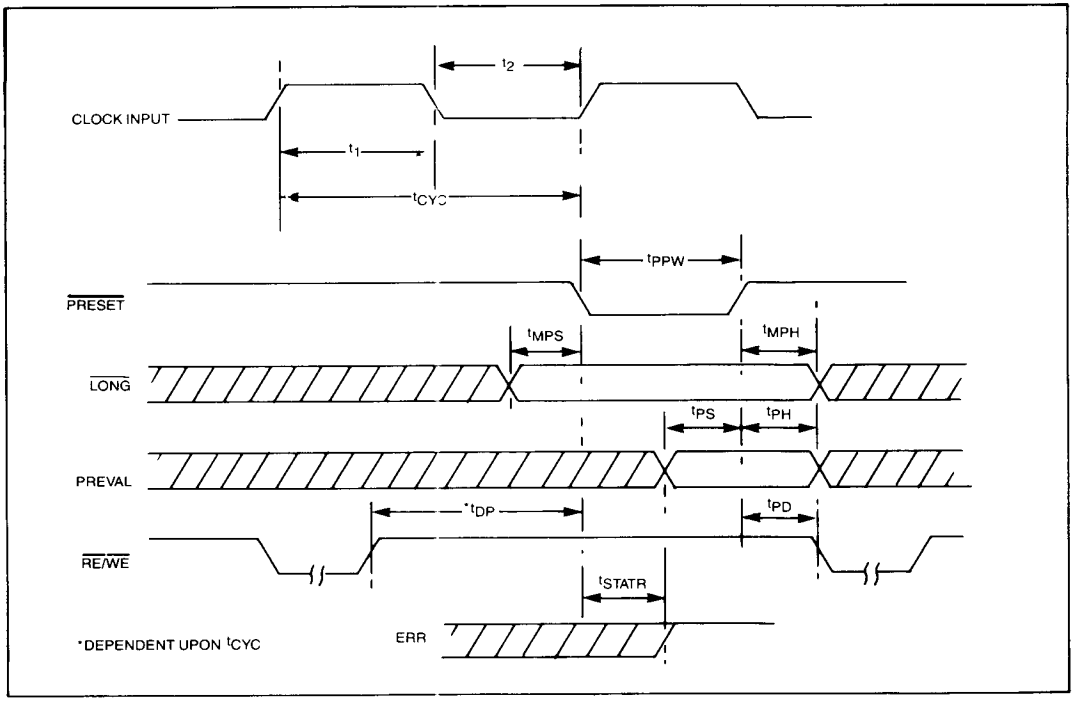


FIGURE 5. MISCELLANEOUS TIMING

TABLE 5. MISCELLANEOUS TIMING All Units in nsec.

SYMBOL	CHARACTERISTICS	MIN	MAX	TYP
t_1	Clock High Period	90		
t_2	Clock Low Period	90		
t_{CYC}	Clock Cycle Period	180		
t_{PPW}	$\overline{\text{PRESET}}$ Input Pulse Width Low	109		
t_{MPS}	Mode Setup to Leading Edge of $\overline{\text{PRESET}}$	23		
t_{MPH}	Mode Hold After Trailing Edge of $\overline{\text{PRESET}}$	0		
t_{PS}	SSC Input Setup to Trailing Edge of $\overline{\text{PRESET}}$	103		
t_{PH}	SSC Input Hold After Trailing Edge of $\overline{\text{PRESET}}$	9		
t_{DP}	Delay from Trailing Edge of $\overline{\text{RE/WE}}$ to Trailing Edge of $\overline{\text{PRESET}}$	4T + 375*		
t_{PD}	Delay from Trailing Edge of $\overline{\text{PRESET}}$ to Leading Edge of $\overline{\text{RE/WE}}$	0		
t_{STATR}	Accumulator ≠ 0 to High Level After Leading Edge of $\overline{\text{PRESET}}$	91		

*T = t_{CYC}