VITELIC

V53C258A FAMILY
HIGH PERFORMANCE, LOW POWER
256K X 1 BIT STATIC COLUMN
CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C258A	60/60L	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	45 ns
Min. Static Column Cycle Time, (t_{SWC}, t_{SRC})	40 ns	45 ns	50 ns	55 ns
Min. Read/Write Cycle Time, (t_{RC})	115 ns	130 ns	145 ns	175 ns

LOW POWER V53C258AL	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	1.2 mA	1.2 mA	1.2 mA	1.2 mA

2

Features

- Low power dissipation for V53C258A-10
  - Operating Current—60 mA max.
  - TTL Standby Current—4.0 mA max.
- Low CMOS Standby Current
  - V53C258A—3.0 mA max.
  - V53C258AL—1.2 mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Static Column Operation – continuous data rate greater that 24 MHz
- Common I/O capability
- 256 Refresh cycles/4 ms
- Standard packages are 16-pin Plastic DIP and 18 pin PLCC

Description

The Vitelic V53C258A is a high-speed 262,144 x 1 bit CMOS dynamic random access memory. Fabricated with Vitelic's VICMOS III technology, the V53C258A offers a combination of size and features unattainable with NMOS technology: Static Column decode for high data bandwidth and clock-free page operation, fast usable speed, CMOS standby current and, for the V53C258AL, reduced CMOS standby mode supply current (I_{DD6}).

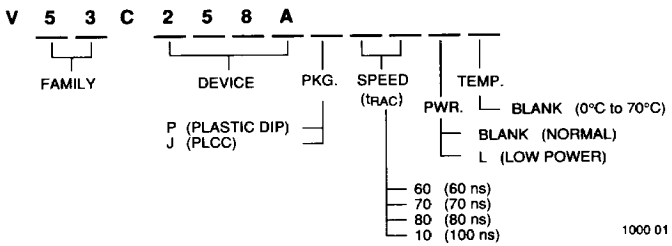
All inputs and outputs are TTL-compatible. Input and output capacitances are significantly lowered to allow increased system performance. Static Column operation allows random access of up to 512 bits within a row with cycle times as short as 40 ns. Because of static circuitry, $\overline{CAS}$ is not required either to clock or to gate column addresses. Since $\overline{CAS}$ is not in the critical access time path, system design is easier, and inherent device speed is more usable. These unique features make the V53C258A ideally suited for computer peripherals, control systems and graphics systems.

The V53C258AL (-10) offers a maximum data retention power of 10 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. For selected V53C258AL devices with Refresh Interval longer than 4 ms, consult the factory.

Device Usage Chart

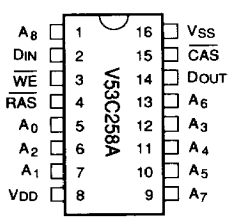
Operating Temperature Range	Package Outline		Access Time (ns)				Power		Temperature Mark
	P	J	60	70	80	100	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	•	Blank

V53C258A Rev. 00 June 1990

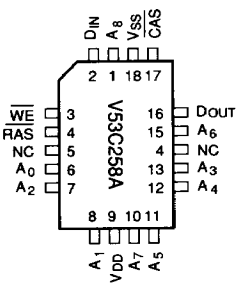


Description	Pkg.	Pin Count
Plastic DIP	P	16
PLCC	J	18

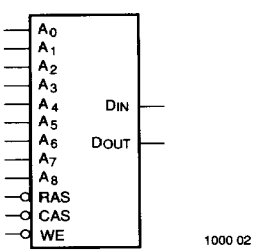
16 Lead Plastic DIP PIN CONFIGURATION
Top View



18 Lead PLCC Package PIN CONFIGURATION
Top View



LOGIC SYMBOL



Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... −1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... −1.0 V to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

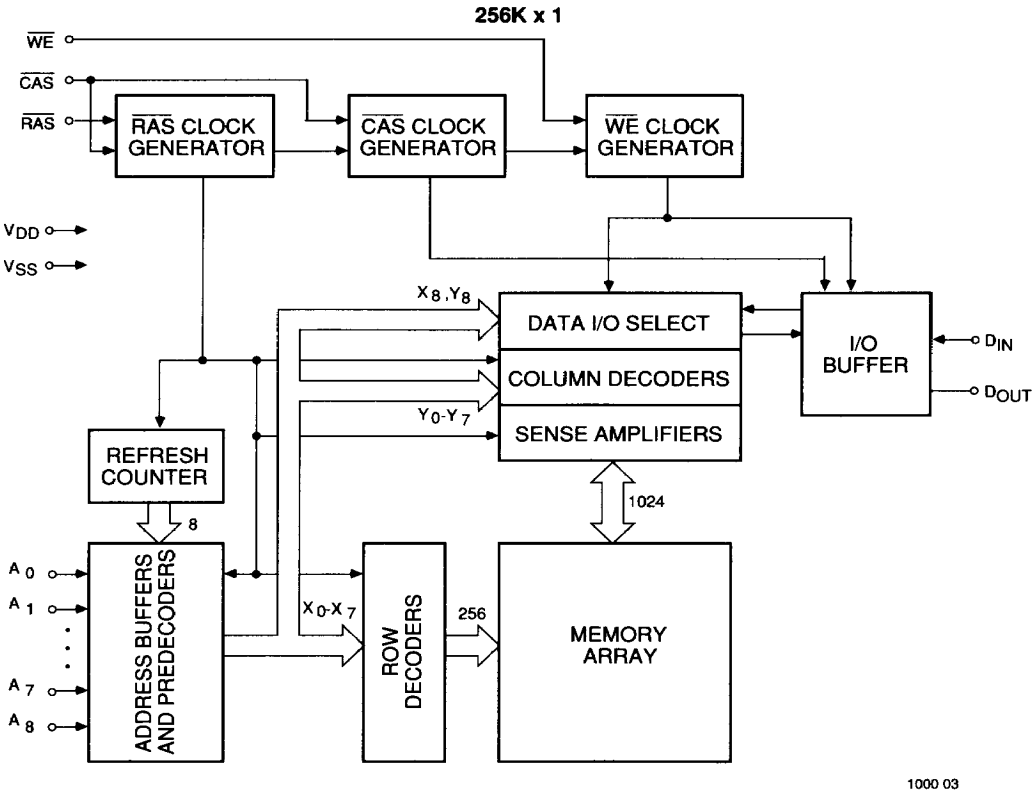
Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C258A			V53C258AL			Unit	Test Conditions	Notes
			Min.	Typ.	Max.	Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10		10	−10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10		10	−10		10	µA	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60			80			80	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		70			70			70			
		80			65			65			
		100			60			60			
I_{DD2}	V_{DD} Supply Current, TTL Standby				3.5			2.0	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60			80			80	mA	$t_{RC} = t_{RC}$ (min.)	2
		70			70			70			
		80			60			60			
		100			50			50			
I_{DD4}	V_{DD} Supply Current, Static Column Mode	60			50			50	mA	Minimum Cycle	1,2
		70			45			45			
		80			40			40			
		100			35			35			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				4			2.5	mA	$\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				3			1.2	mA	$\overline{RAS} \ge V_{DD}$ −0.2 V, $\overline{CAS} = V_{IH}$, other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		−1		0.8	−1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{DD} +1	2.4		V_{DD} +1	V		3
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL}	t_{RC}	Read or Write Cycle Time	115		130		145		175		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	45		50		55		65		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		15		15		15		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		45		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	20	35	20	40	20	55	ns	4
8	t_{RH2AX}	t_{ARH}	Column Address Hold Time from $\overline{RAS}$	5		5		5		5		ns	
9	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	25	55	25	60	25	75	ns	5
10	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	6,7,8
11	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40		45	ns	8,9,16
12	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		15		20		25	ns	8
13	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	15		15		20		25		ns	
14	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		15		20		25		ns	
15	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
16	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		5		ns	10
17	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15		15		15		15		ns	
18	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	10	0	15	0	20	0	25	ns	11
19	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		0		ns	11
20	t_{AVWL2}	t_{AWS}	Column Address to Write Command Setup Time	0		0		0		0		ns	

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{WL1AX}	t_{AWH}	Column Address to Write Command Hold Time	10		15		15		205		ns	
22	t_{RL1AX}	t_{ARW}	Column Address Hold Time from $\overline{RAS}$ (Write)	50		55		60		70		ns	
23	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width (Write)	15		20		25		30		ns	
24	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write)	15		25		25		30		ns	
25	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		70		ns	
26	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12,13
27	t_{CH2WH1}	t_{WHC}	Write Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	12,14
28	t_{RH2WH1}	t_{WHR}	Write Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	12,14
29	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		0		ns	15
30	t_{WH1DX}	t_{DH}	Data In Hold Time	10		15		15		20		ns	15
31	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	50		55		60		70		ns	
32	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	135		155		175		210		ns	
33	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	80		95		110		135		ns	
34	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time Read-Modify-Write Cycle	60		70		80		100		ns	12
35	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	15		15		20		25		ns	12
36	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	30		35		40		45		ns	12
37	t_{RL1AX}	t_{ARR}	Column Address Hold Time from $\overline{RAS}$ (Read)	60		70		80		100		ns	
38	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		5		ns	10

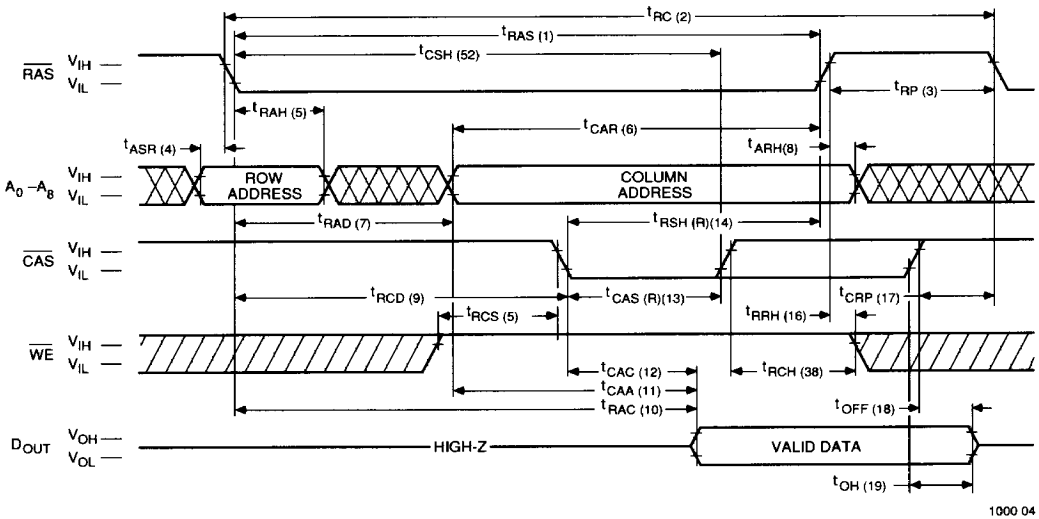
AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{AVAV}	t_{SRC}	Static Column Mode Read Cycle	40		45		50		55		ns	
40	t_{AXQX}	t_{OHA}	Output Hold Time from Address Change	0		0		0		0		ns	
41	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		15		20		25		ns	
42	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ LeadTime	15		20		25		30		ns	
43	t_{WL2WL2}	t_{SWC}	Static Column Mode Write Cycle Time	40		45		50		55		ns	
44	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		20		25		ns	
45	t_{WL1QV}	t_{WRA}	Write-Read Access Time		70		80		90		100	ns	8
46	t_{WH2QV}	t_{WPA}	Write Precharge Access Time		15		15		20		25	ns	8,16
47	t_{WH1QX}	t_{WOH}	Output Hold Time from $\overline{WE}$	0		0		0		0		ns	
48	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		10		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	15		20		25		30		ns	
50	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
51	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		25		30		ns	
52	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
53	t_{WH2WL2}	t_{WCP}	Write Command Precharge Time	10		15		20		25		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	17,18
		t_{RI}	Refresh Interval (256 Cycles)		4		4		4		4	ms	19

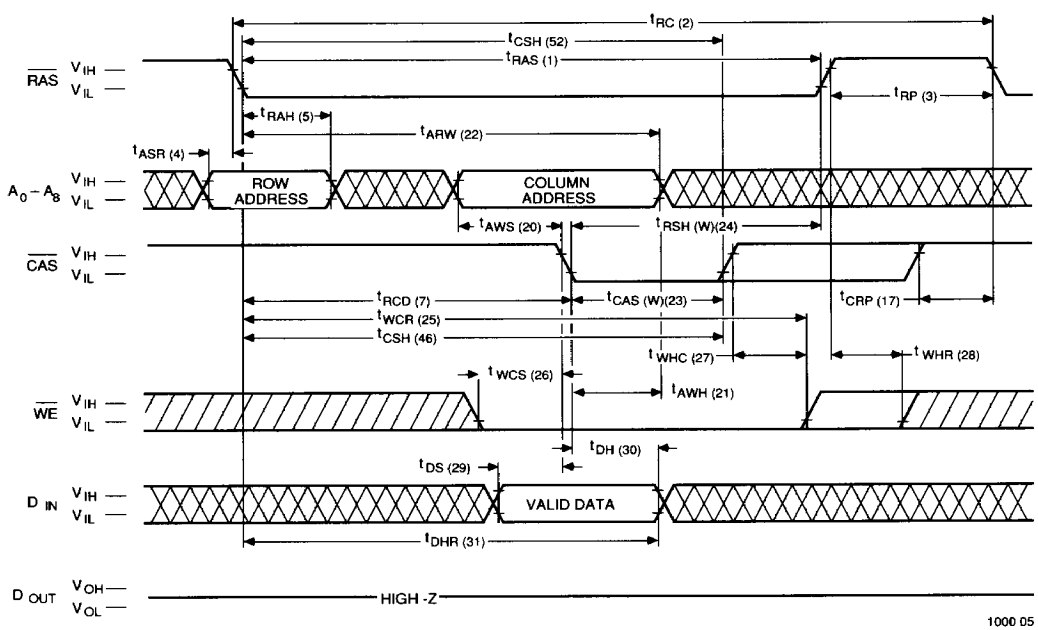
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Static Column Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to −1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
10. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
11. t_{OFF} and t_{OH} define the time when the output reaches an open circuit condition and are not referenced to the output voltage levels.
12. t_{WCS}, t_{WHC}, t_{WHR}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. Either t_{WHC} (min.) or t_{WHR} (min.) must be satisified in an Early Write and Read-Modify-Write cycles.
15. t_{DS} and t_{DH} are referenced to the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
16. Access time is determined by the longer of t_{CAA}, or t_{WPA}.
17. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
18. AC measurements assume t_T = 5 ns.
19. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

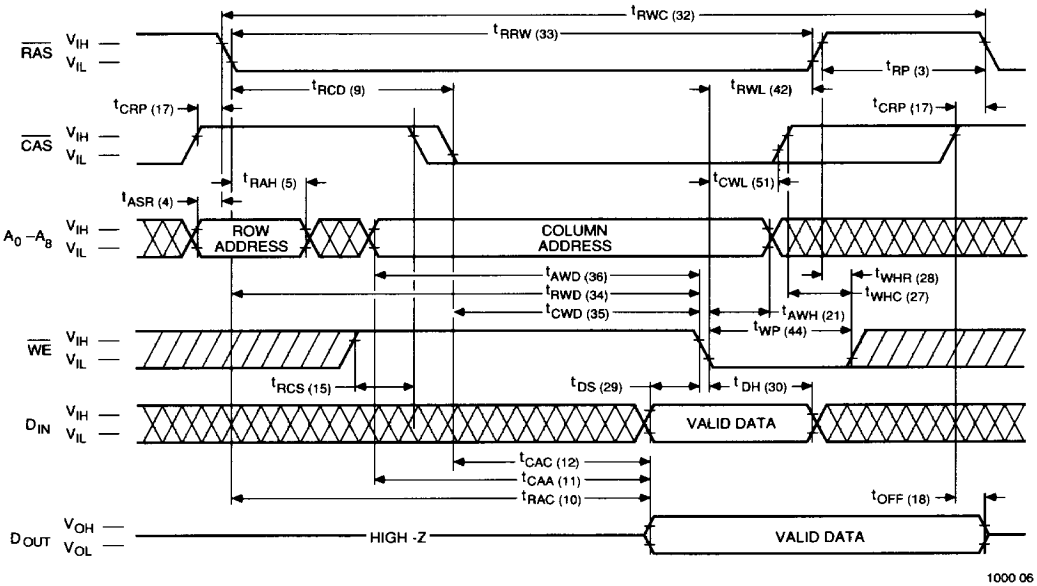
Waveforms of Read Cycle



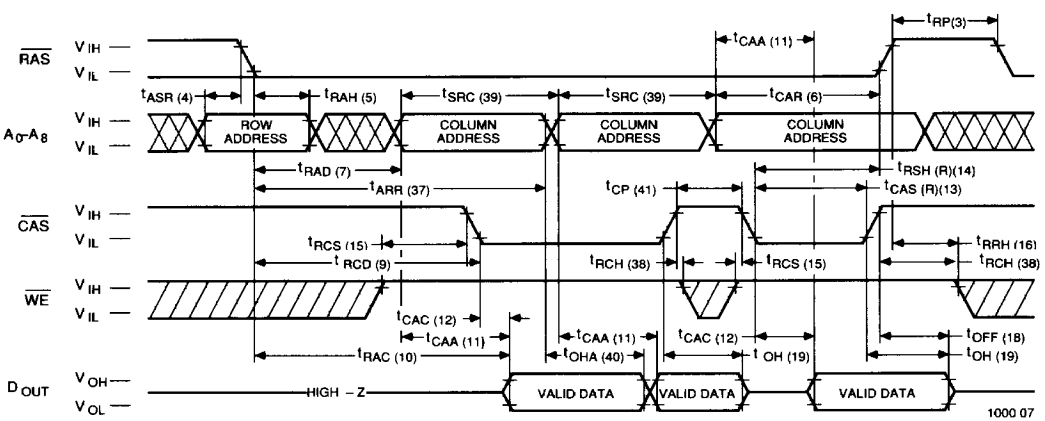
Waveforms of Early Write Cycle



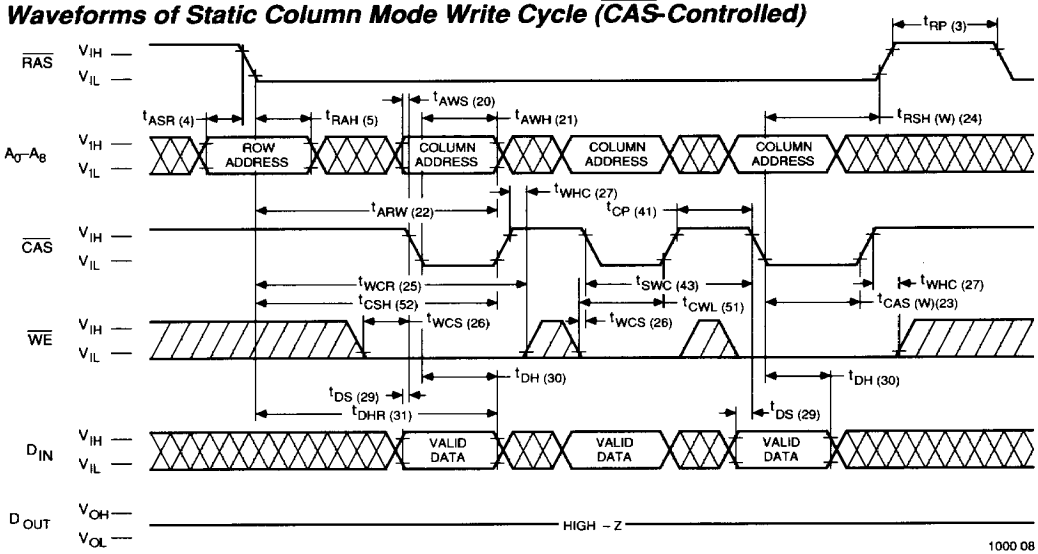
Waveforms of Read-Modify-Write Cycle



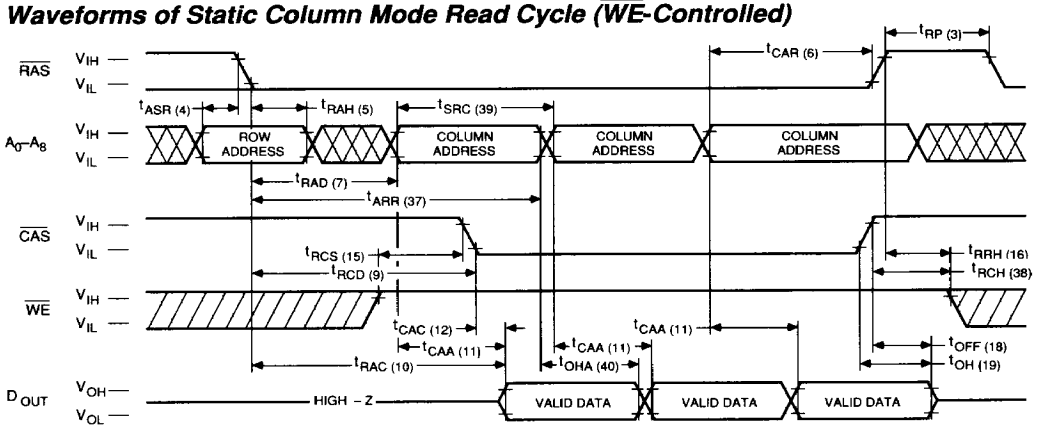
Waveforms of Static Column Mode Read Cycle ($\overline{CAS}$-Controlled)



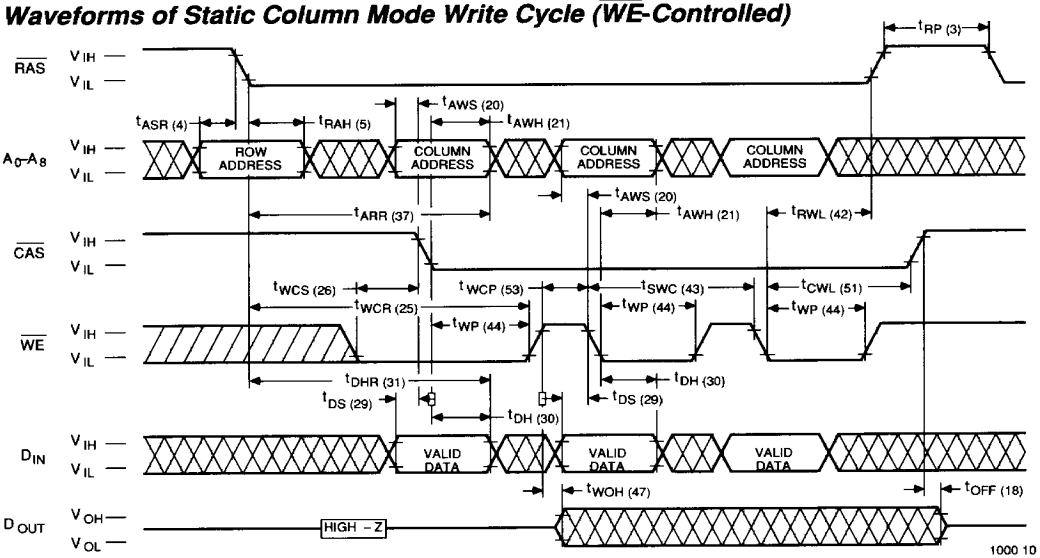
Waveforms of Static Column Mode Write Cycle ($\overline{CAS}$-Controlled)



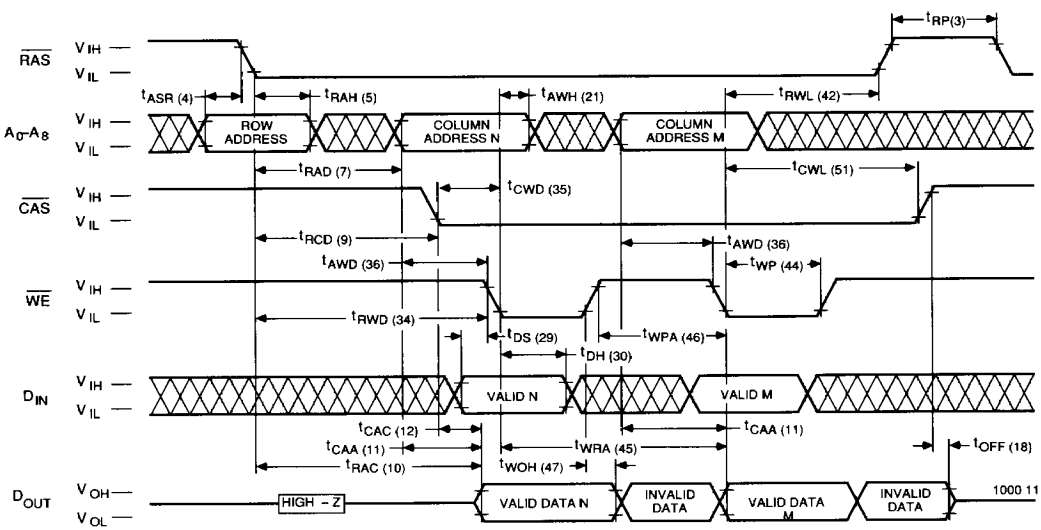
Waveforms of Static Column Mode Read Cycle ($\overline{WE}$-Controlled)



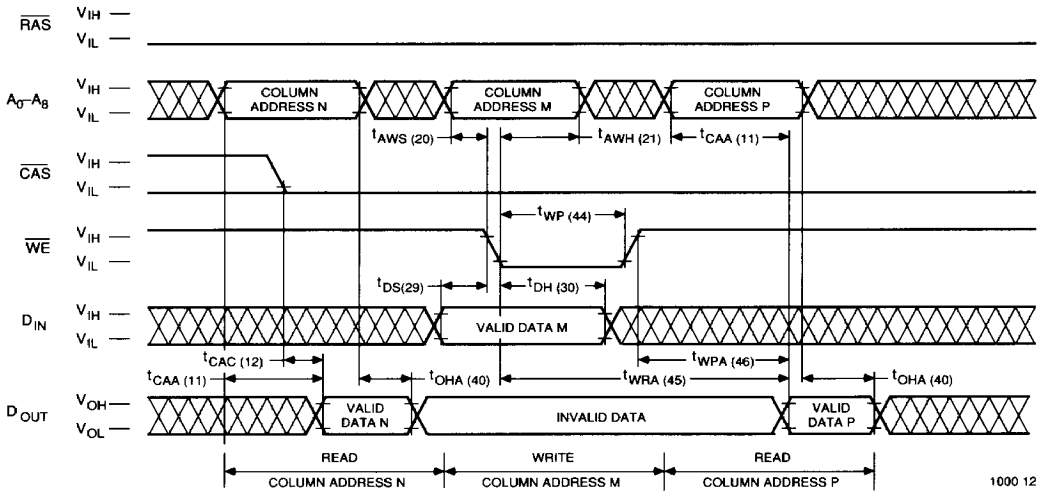
Waveforms of Static Column Mode Write Cycle ($\overline{WE}$-Controlled)



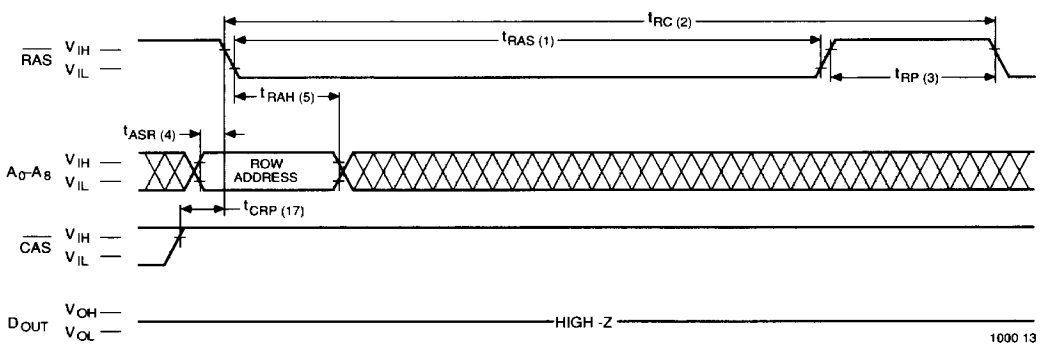
Waveforms of Static Column Mode Read-Write Cycle



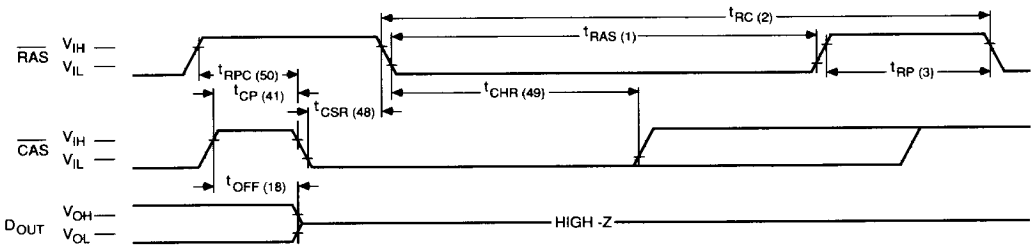
Waveforms of Static Column Mode Read-Write Mixed Cycle



Waveforms of RAS-Only Refresh Cycle



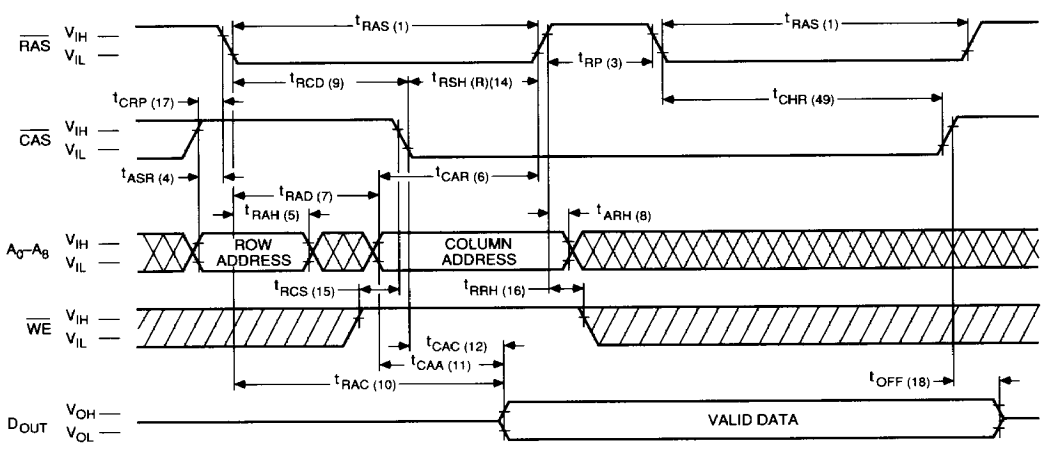
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



1000 14

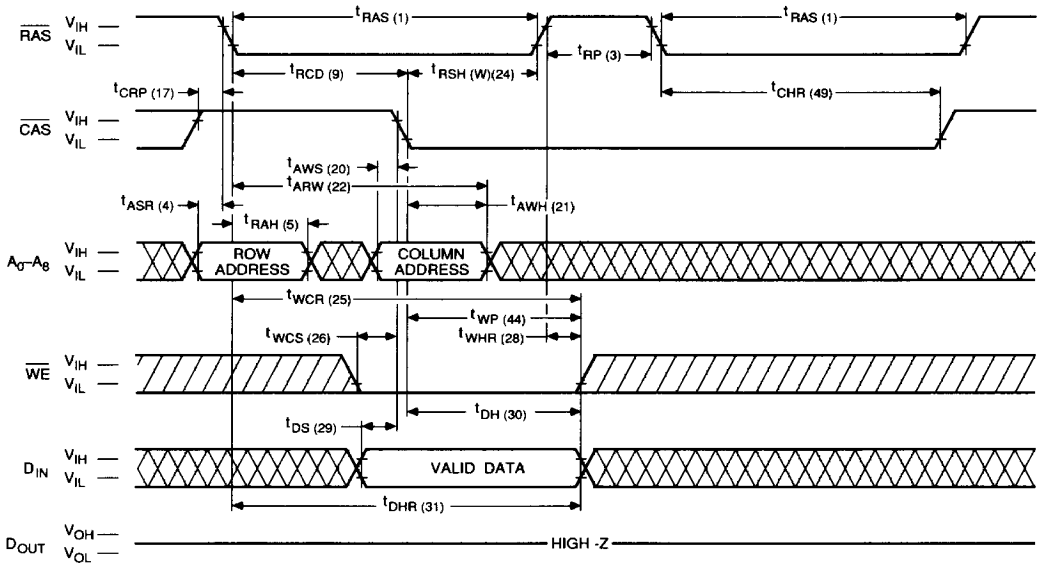
NOTE: $\overline{WE}$ = Don't Care
D_{IN} = Don't Care
A_0–A_8 = Don't Care

Waveforms of Hidden Refresh Cycle (Read)

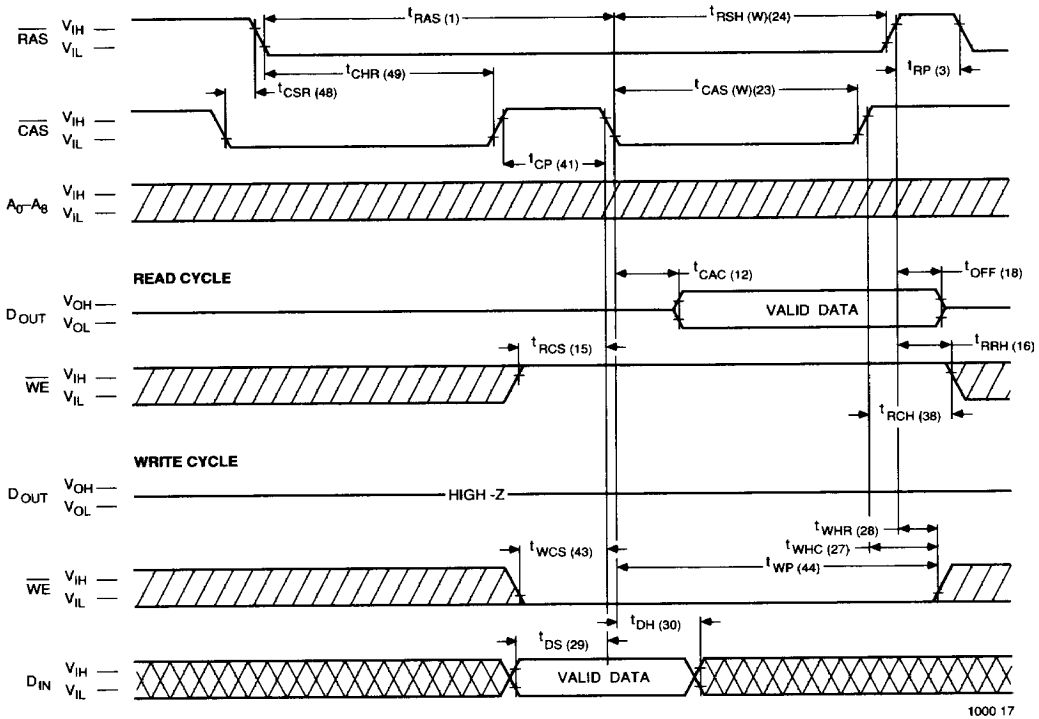


1000 15

Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C258A is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to other dynamic RAMs. The V53C258A reads and writes one data bit at a time by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address, however, is only latched during a Write cycle by either Column Address Strobe ($\overline{CAS}$) or Write Enable ($\overline{WE}$), whichever occurs last. During a Read cycle, the column address is not latched and continuously "flows through" the internal input latches. Access time is primarily dependent on a valid column address. $\overline{CAS}$ acts as an output enable signal in the access path.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle initiated must not be ended or aborted before the minimum t_{RAS} time specification. This ensures proper device operation and data integrity. Also, a new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address is not latched and must be held valid until the output becomes valid. This occurs after t_{RAC}, t_{CAA} and t_{CAA} are all satisfied. Consequently, the access time is dependent on the timing relationships among t_{RAC}, t_{CAC} and t_{CAA}. For example, the access time is limited by t_{CAA} when t_{RAC} (min.) and t_{CAC} (min.) are both satisfied.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by the later of either $\overline{WE}$ or $\overline{CAS}$ going low. The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Consequently, the Write cycle can be $\overline{WE}$-controlled or $\overline{CAS}$-controlled. In a $\overline{CAS}$-controlled Write cycle where the leading edge of $\overline{WE}$ occurs prior to or coincident with $\overline{CAS}$ low transition, the output pin will be in the High-Z state at the beginning of the Write cycle. Terminating the Write cycle with $\overline{CAS}$ going high will maintain the output in the High-Z state. Terminating the Write cycle with $\overline{WE}$ going high allows the output to go active and starts a Read (Read after Write).

The V53C258A incorporates a self-timed write feature that simplifies the system interface and optimizes data bandwidth. After the Write has been initiated, the V53C258A internally completes the write action and unlatches the address and data latches to be ready for the next input/output cycle. This eliminates the need for long address and data hold times during write operations and allows a subsequent column address to be applied earlier. The write pulse width, write precharge and hold time are minimized, providing maximum flexibility in system design.

Refresh Cycle

To retain data, 256 Refresh Cycles are required in each 4 ms period. Refresh can be performed in two ways:

1. By selecting each of the 256 row addresses determined by A0 through A7 at least once every 4 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ is low during the falling edge of $\overline{RAS}$, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C258A will use the output of an internal eight-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a refresh-only mode and no data access or device selection is allowed. Therefore, the state of the output will remain at High-Z.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to execute 256 consecutive Write cycles and then verify the written data by applying 256 consecutive Read cycles. In this mode, the V53C258A ignores external row/column addresses and takes the output from the internal counter instead.

Data Retention Mode

The V53C258A offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C258A power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 256

Static Column Mode Operation

Static Column Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Read, Write and Read-Write-Read cycles can be performed during Static Column operation. The row address is internally retained by maintaining $\overline{RAS}$ active. Following the entry cycle into Static Column mode, data are accessed by simply changing the column address. Because the column address buffer acts as transparent or flow-through latches, access begins from a valid column address.

Thus, the V53C258A behaves like a Static RAM for multiple column accesses within a row. $\overline{CAS}$ acts as an output enable. Static Column mode allows mixed Read and Write cycles. Terminating a Write cycle by taking $\overline{WE}$ high causes the Data Output lines to assume the Low-Z condition. The user has total control of Read and Write cycles by using different $\overline{WE}$ timings.

Static Column Mode provides a sustained data rate of over 24 MHz for applications that require high data rates. The following equation can be used to calculate the data rate achievable:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{SRC}}$$

Data Output Operation

The V53C258A data output pin has three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\overline{CAS}$ at V_{IH}), the output is in the High-Z state. Table 1 summarizes the output state possible for various memory cycles.

Power-On

After application of the V_{DD}, an initial pause of 200 µs is required, followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C258A is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle, and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid I_{DD} surges.

Table 1. Vitelic V53C258A Data Output
Operation for Various Cycle Types

Cycle Type	D_{OUT} State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	Active, not valid
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Static Column Mode Read Cycle	Data from Addressed Memory Cell
Static Column Mode Write Cycle (Early Write)	High-Z
Static Column Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z