WD33C92 And WD33C93 SCSI-Bus Interface Controller

T-52-33-27

DOCUMENT SCOPE

This document describes both the WD33C92-SBIC and WD33C93-SBIC. The Register File and Commands are identical for both devices. For those areas in which the devices differ, the WD33C92 is referred to first followed by the WD33C93.

FEATURES

- Implements full SCSI features:
  Arbitration, Disconnect
  Reconnect, Parity,
  Synchronous data transfers up to 4 Mbytes/Sec with an offset programmable from one to five
- Can be used as host adapter or peripheral adapter
- Selectable for programmed-I/O DMA transfers, or direct buffer access (DBA)
- "Combination" commands greatly reduce interrupt-handling responsibilities
- The WD33C92 is available in 48-pin DIP or 44-pin QSM package
- The WD33C93 is available in 40-pin DIP or 44-pin QSM package
- Full compliance with ANSI SCSI X3T9.2 specifications
- Compatible with most microprocessors through an 8-bit data bus, supports both multiplexed and non-multiplexed address/data bus systems
- The WD33C92 includes 48-MA drivers for direct connection to the SCSI bus
- Programmable timeouts for selection and reselection
- Special "translate address" command performs the logical-to-physical address translation
- 24-bit transfer counter
- Single +5V supply
- Low power CMOS design

Table of Contents

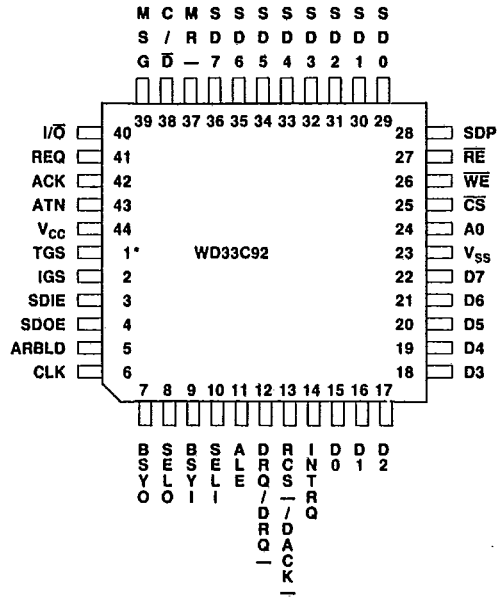
T-52-33-27

List of Illustrations

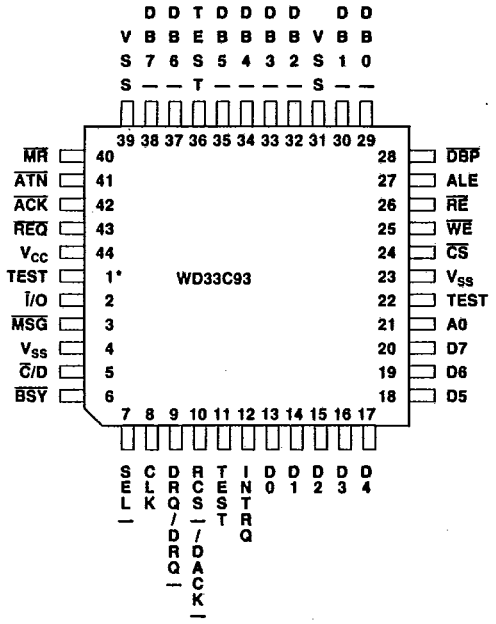
T-52-33-27

List of Tables

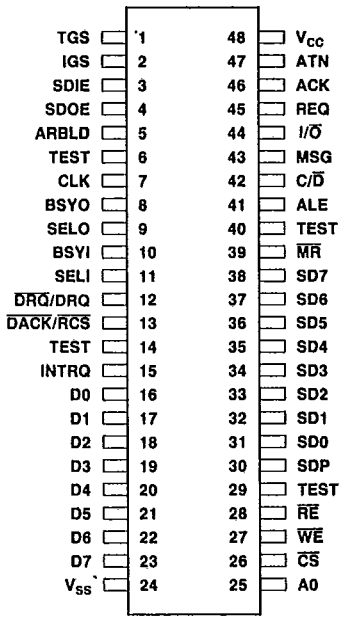
T-52-33-27



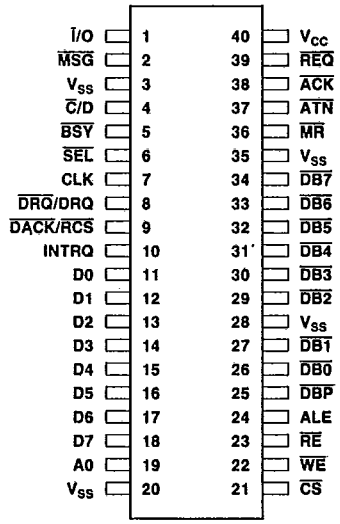
WD33C92-SBIC QSM Diagram



WD33C93-SBIC QSM Diagram



WD33C92-SBIC DIP Diagram



WD33C93-SBIC DIP DIAGRAM

T-52-33-27

DESCRIPTION

The WD33C92/3 SCSI Bus Interface Controllers are designed to adapt either a Host (Initiator) system or a peripheral controller (Target) system to the SCSI bus. In either environment, the WD33C92/3 operates in any one of three possible states: Disconnected, connected as a Target or connected as an Initiator.

The WD33C92 is used in conjunction with external drivers for the differential driver option. The WD33C93-SBIC includes 48 MA drivers, allowing direct connection to the SCSI bus for the single-ended interfacing option.

Following is a brief summary of the SCSI protocol between a Host/Initiator and a Target/Controller.

- The Host selects a SCSI controller.
- The controller requests a command from the Host specifying the task to be performed, eg. disk read.
- The controller interprets the command and executes it by reading data from the disk and then requesting that the Host accept the data.
- When all data has been transferred, the controller requests that the Host accept the Status Byte.
- After the Host accepts the status from the controller, the controller disconnects from the bus, leaving it free for the next operation.

When used in an initiator system, the WD33C92/3-SBIC connects to both the Host (8086/8088 type) bus and the SCSI bus, waits for a command from the Host to select a specific Target, arbitrates for the SCSI bus if necessary, and selects the designated Target. When the bus is busy serving a higher priority Initiator, the WD33C92/3-SBIC waits for the bus to become available, then attempts to select the Target. When successful, the WD33C92/3-SBIC generates an interrupt to the Host to indicate that the selection process has been completed. After the Target device requests a command byte, the WD33C92/3-SBIC interrupts the Host and passes on the request. The Host responds by giving a "Transfer Info" command to the WD33C92/3-SBIC, along with the command byte requested by the Target, and then the command byte is passed on to the Target. This process continues until all command, data, and status bytes have been transferred. During a data transfer phase, the data can be transferred between the WD33C92/3-SBIC and Host memory via DMA. To relieve the Host of some of the interrupt-handling responsibilities, the Select and Transfer Information commands may be chained together by using the special SELECT-AND-TRANSFER commands.

When the WD33C92/3-SBIC is used in a peripheral controller system, it communicates with the local processor and SCSI bus in the same way as when used in an initiator system. It is also capable of operating as a busmaster on the controller's local data bus. Therefore, during a data transfer phase, the WD33C92/3-SBIC can issue read and write enables to access an external buffer without requiring DMA or programmed I/O transfers.

The WD33C92/3 implements arbitration, parity, and synchronous transfers as well as the full standard SCSI physical path definition for use with either the differential or single-ended interfacing option.

The WD33C92/3-SBICs are MOS/VLSI devices implemented in 3 micron high-speed CMOS, operating from a single +5 volt supply. The WD33C92/3-SBIC is available in a 48-pin DIP, while the WD33C93-SBIC is available in a 40-pin DIP. Both devices are available in 44-pin QSM packages. All input and output pins are TTL compatible.

T-52-33-27

WD33C92-SBIC SIGNAL DESCRIPTION

The following table describes the function of the signals serviced by the WD33C92/3-SBIC. The signals that deal with the SCSI bus are presented first, followed by the signals that communicate with the Host/DMA interface.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
DIP/QSM		**SCSI INTERFACE**		
1/1	TGS	TARGET GROUP SELECT	O	The WD33C92 asserts TGS when operating as a Target. This enables the SCSI drivers for REQ, MSG C/$\overline{D}$, and I/$\overline{O}$ as output signals. When in the Idle or Initiator state, TGS is de-asserted and REQ, MSG, C/$\overline{D}$, and I/$\overline{O}$ are enabled for input.
2/2	IGS	INITIATOR GROUP SELECT	O	The WD33C92 asserts IGS when operating as an Initiator. This enables SCSI drivers for ATN and ACK as output signals. When in the Idle or Target state, IGS is de-asserted and ATN and ACK are enabled for input.
3/3	SDIE	SCSI DATA IN ENABLE	O	Enables SCSI data bus receivers.
4/4	SDOE	SCSI DATA OUT ENABLE	O	Enables SCSI data bus drivers.
5/5	ARBLD	ARBITRATION LOAD	O	Latches the decoded port number into an external register just prior to the SCSI bus arbitration process.
8/7	BSYO	BUSY OUT	O	The WD33C92 asserts BSYO to drive the SCSI $\overline{BSY}$ signal.
10/9	BSYI	BUSY IN	I	BSYI signals the WD33C92 that the SCSI $\overline{BSY}$ signal is asserted.
9/8	SELO	SELECT OUT	O	The WD33C92 asserts SELO to drive the SCSI $\overline{SEL}$ signal.
11/10	SELI	SELECT IN	I	When asserted, SELI signals the WD33C92 that the SCSI $\overline{SEL}$ signal is asserted.
30/28	SDP	SCSI DATA PARITY	I/O	SCSI bus data parity
31/29 thru 38/36	SD0 thru SD7	SCSI DATA 0 thru SCSI DATA 7	I/O	SCSI bus data bit 0 thru SCSI bus data bit 7
42/38	C/$\overline{D}$	CONTROL/$\overline{DATA}$	I/O	C/$\overline{D}$ is asserted when there is Control information on the SCSI data bus and de-asserted for data. C/$\overline{D}$ is an input when the WD33C92 is operating as an Initiator (TGS de-asserted) and an output when operating as a Target (TGS asserted).
43/39	MSG	MESSAGE	I/O	MSG is asserted during a message phase. MSG is an input when the WD33C92 is operating as an Initiator (TGS de-asserted) and an output when operating as a Target (TGS asserted).
44/40	I/$\overline{O}$	INPUT/$\overline{OUTPUT}$	I/O	I/$\overline{O}$ controls the direction of data movement on the SCSI bus with respect to the Initiator. When asserted, data is input to the Initiator. When de-asserted, data is output from the Initiator. I/$\overline{O}$ is an input signal when the WD33C92 is operating as an Initiator (TGS de-asserted) and an output signal when operating as a Target (TGS asserted).

PIN NUMBER DIP/QSM	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
SCSI INTERFACE (cont.)				
45/41	REQ	REQUEST	I/O	REQ requests an REQ/ACK data transfer. REQ is an input signal when the WD33C92 is operating as an Initiator (TGS de-asserted), and an output signal when operating as a Target (TGS asserted).
46/42	ACK	ACKNOWLEDGE	I/O	ACK acknowledges a REQ/ACK data transfer handshake. ACK is an output signal when the WD33C92 is operating as an Initiator (IGS asserted), and an input when operating as a Target (IGS de-asserted).
47/34	ATN	ATTENTION	I/O	ATN signals that the Initiator has a message to transfer. ATN is an output signal when the WD33C92 is operating as an Initiator (IGS asserted) and an input signal when connected as a Target (IGS de-asserted).
PROCESSOR/DMA INTERFACE				
7/6	CLK	CLOCK	I	10 MHz square wave clock
12/12	$\overline{DRQ}$/DRQ	$\overline{DATA\ REQUEST}$	O	DRQ interfaces with an external DMA controller (eg. 8237) and forms the $\overline{DRQ}$/$\overline{DACK}$ handshake for data byte transfers.
		DATA REQUEST	I	DRQ interfaces with an external buffer. When asserted, data burst transfers are enabled using Direct Buffer Access (DBA). This signal is open drain. DRQ should be pulled up to +5v with a 1K resistor.
13/13	$\overline{DACK}$/$\overline{RCS}$	$\overline{DMA\ ACKNOWLEDGE}$	I	$\overline{DACK}$ interfaces with an external DMA controller (eg. 8237). When asserted, all bus transfers are to or from the Data Register regardless of the contents of the Address Register.
		$\overline{RAM\ CHIP\ SELECT}$	O	$\overline{RCS}$ interfaces with an external buffer. When asserted, $\overline{WE}$ and $\overline{RE}$ are enabled as output signals making it possible for the WD33C92 to access the buffer directly. ALE must be low (Ov) during DMA or DBA transfers. $\overline{CS}$ must be inactive (+5v) during $\overline{DACK}$ or $\overline{RCS}$ active (100ns margin). This signal is open drain.
15/14	INTRQ	INTERRUPT REQUEST	O	INTRQ signals a local microprocessor or Host that a WD33C92 command has terminated or the SCSI interface needs service.
16/15 thru 23/22	DO thru D7	DATA O thru DATA 7	I/O	Local data bus bit 0 thru Local Data bus bit 7
25/24	A0	ADDRESS O	I	A0 is used to access an internal register during indirect addressing mode of operation. During direct addressing A0 is ignored. A0 = 0. The address of the desired register is loaded into the Address Register during a write cycle ($\overline{WE}$ asserted). A0 = 1. The register selected by the Address REgister is accessed.
26/25	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	When $\overline{CS}$ is asserted, $\overline{WE}$ and $\overline{RE}$ are enabled as input signals for accessing registers within the WD33C92.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
DIP/QSM		**PROCESSOR/DMA INTERFACE (cont.)**		
27/26	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I/O	$\overline{WE}$ is an input signal and enables writing to an internal register when used with $\overline{CS}$. $\overline{WE}$ is a an output signal and enables writing to the external buffer when used with $\overline{RCS}$. $\overline{WE}$ is a tri-state signal.
28/27	$\overline{RE}$	$\overline{READ\ ENABLE}$	I/O	$\overline{RE}$ is an input signal and enables reading an internal register when used with $\overline{CS}$. $\overline{RE}$ is an output signal and enables reading the external buffer when used with $\overline{RCS}$. $\overline{RE}$ is a tri-state signal.
39/37	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	When asserted, $\overline{MR}$ places the WD33C92 into an idle state. All SCSI signals are placed in a passive state.
41/11	ALE	ADDRESS LATCH ENABLE	I	With the trailing edge of ALE, the address on the local Data Bus is latched into the Address Register. When indirect addressing is used, as in non-multiplexed busses, the ALE pin must be grounded.
		MISCELLANEOUS		
6/ 14/ 24/23 29/ 40/ 48/44	TEST TEST V_{SS} TEST TEST V_{CC}	FACTORY TEST FACTORY TEST GROUND FACTORY TEST FACTORY TEST +5 VOLTS		TEST pins are for factory use only and should not be connected.

WD33C93-SBIC SIGNAL DESCRIPTION

The following table describes the function of the signals serviced by the WD33C93-SBIC. The signals that deal with the SCSI bus are presented first, followed by the signals that communicate with the Host/DMA interface.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
DIP/QSM	SCSI INTERFACE — All SCSI pins have open-drain output drivers			
1/2	I/O	INPUT/OUTPUT	I/O	I/O controls the direction of data movement on the SCSI bus with respect to the Initiator. When asserted, data is input to the Initiator. When de-asserted, data is output from the Initiator. IO is an input signal when the WD33C93 is operating as an Initiator and an output signal when operating as a Target.
2/3	MSG	MESSAGE	I/O	MSG is asserted during a message phase. MSG is an input when the WD33C93 is operating as an Initiator and an output when operating as a Target.
4/5	C/D	CONTROL/DATA	I/O	C/D is asserted when there is Control information on the SCSI data bus and de-asserted for data. C/D is an input when the WD33C93 is operating as an Initiator and an output when operating as a Target.
5/6	BSY	BUSY	I/O	BSY is asserted by the WD33C93 as an output when attempting to arbitrate for the SCSI bus or when connected as a target. When the WD33C93 is connected as an Initiator, BSY operates as an input.
6/7	SEL	SELECT	I/O	The WD33C93 asserts SEL as an output when trying to select or reselect another SCSI device. The WD33C93 receives SEL as an input when it is being selected.
25/28	DBP	SCSI DATA PARITY	I/O	SCSI bus data parity
26/29	DB0	SCSI DATA 0	I/O	SCSI bus data bit 0
27/30	DB1	SCSI DATA 1	I/O	SCSI bus data bit 1
29/32 thru 32/35	DB2 thru DB5	SCSI DATA 2 thru 5	I/O	SCSI bus data bit 2 thru SCSI bus data 5
33/37	DB6	SCSI DATA 6	I/O	SCSI bus data bit 6
34/38	DB7	SCSI DATA 7	I/O	SCSI bus data bit 7
37/41	ATN	ATTENTION	I/O	ATN signals that the Initiator has a message to transfer. ATN is an output signal when the WD33C93-SBIC is operating as an Initiator and an input signal when connected as a Target.
38/42	ACK	ACKNOWLEDGE	I/O	ACK acknowledges a REQ/ACK data transfer handshake. ACK is an output signal when the WD33C93 is operating as an Initiator and an input when operating as a Target.
39/43	REQ	REQUEST	I/O	REQ requests an REQ/ACK data transfer. REQ is an input signal when the WD33C93 is operating as an Initiator and an output signal when operating as a Target.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
DIP/QSM		PROCESSOR/DMA INTERFACE		
7/8	CLK	CLOCK	I	10 MHz square wave clock
8/9	$\overline{DRQ}$/DRQ	$\overline{DATA\ REQUEST}$	O	DRQ interfaces with an external DMA controller (eg. 8237) and forms the $\overline{DRQ}$/$\overline{DACK}$ handshake for data byte transfers.
		DATA REQUEST	I	DRQ interfaces with an external buffer. When asserted, data burst transfers are enabled using Direct Buffer Access (DBA). This signal is open drain. DRQ should be pulled up to +5V with a 1K resistor.
9/10	$\overline{DACK}$/$\overline{RCS}$	$\overline{DMA\ ACKNOWLEDGE}$	I	$\overline{DACK}$ interfaces with an external DMA controller (eg. 8237). When asserted, all bus transfers are to or from the Data Register regardless of the contents of the Address Register.
		$\overline{RAM\ CHIP\ SELECT}$	O	$\overline{RCS}$ interfaces with an external buffer. When $\overline{RCS}$ is asserted, $\overline{WE}$ and $\overline{RE}$ are enabled as output signals making it possible for the WD33C93 to access the buffer directly. ALE must be low (Ov) during DMA or DBA transfers. $\overline{CS}$ must be inactive (+5V) during $\overline{DACK}$ or $\overline{RCS}$ active (100ns margin). This signal is open drain.
10/12	INTRQ	INTERRUPT REQUEST	O	INTRQ signals a local microprocessor or Host that a WD33C93 command has terminated or the SCSI interface needs service.
11/13 thru 18/20	D0 thru D7	DATA 0 thru DATA 7	I/O	Local data bus bit O thru Local Data bus bit 7
19/21	A0	ADDRESS O	I	A0 is used to access an internal register during the indirect addressing mode of operation. During direct addressing A0 is ignored. A0 = O. The address of the desired register is loaded into the Address Register during a write cycle ($\overline{WE}$ asserted). A0 = 1. The register selected by the Address Register is accessed.
21/24	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	When $\overline{CS}$ is asserted, $\overline{WE}$ and $\overline{RE}$ are enabled as input signals for accessing registers within the WD33C93.
22/25	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I/O	$\overline{WE}$ is an input signal and enables writing to an internal register when used with $\overline{CS}$. $\overline{WE}$ is an output signal and enables writing to the external buffer when used with $\overline{RCS}$. $\overline{WE}$ is a tri-state signal.
23/26	$\overline{RE}$	$\overline{READ\ ENABLE}$	I/O	$\overline{RE}$ is an input signal and enables reading an internal register when used with $\overline{CS}$. $\overline{RE}$ is an output signal and enables reading the external buffer when used with $\overline{RCS}$. $\overline{RE}$ is a tri-state signal.
24/27	ALE	ADDRESS	I	With the trailing edge of ALE, the address on the local data bus is latched into the Address Register. When indirect addressing is used, as in non-multiplexed busses the ALE pin must be grounded.
36/40	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	When asserted, $\overline{MR}$ places the WD33C93 into a disconnected state. All SCSI signals are placed in a passive state.

PIN NUMBER DIP/QSM	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
		MISCELLANEOUS		
/1	TEST	FACTORY TEST		TEST pins are for factory use only and should not be connected.
/11	TEST	FACTORY TEST		
3/4	V_{SS}	GROUND		
20/23	V_{SS}	GROUND		
28/31	V_{SS}	GROUND		
35/39	V_{SS}	GROUND		
/29	TEST	FACTORY TEST		
/36	TEST	FACTORY TEST		
40/44	V_{CC}	+ 5 VOLTS		

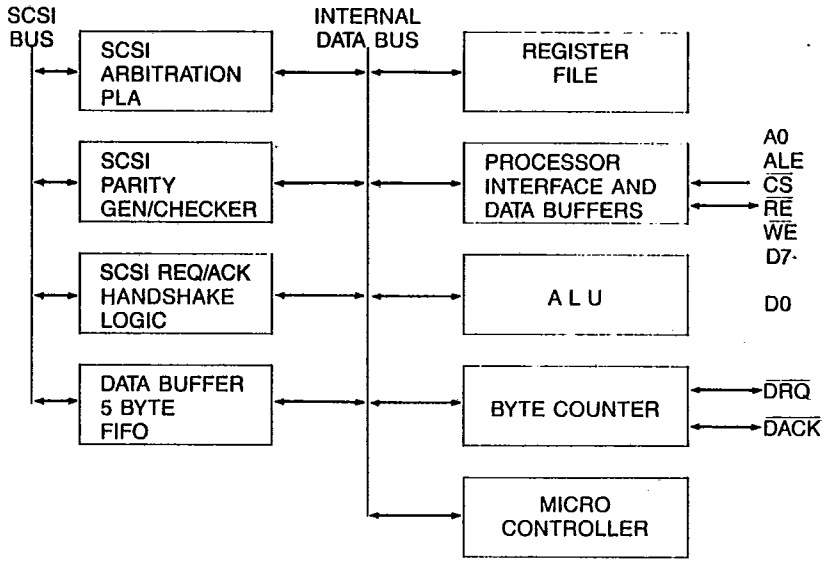


FIGURE 1. WD33C92/3-SBIC BLOCK DIAGRAM

ARCHITECTURE

As illustrated in Figure 1, the WD33C92/3-SBIC consists of nine major building blocks.

SCSI ARBITRATION PLA

The Programmable Logic Array (PLA) performs the SCSI arbitration process. When a Select or Reselect Command is issued, the PLA waits for the bus free condition ($\overline{BSY}$ and $\overline{SEL}$ both false), then outputs the chips's bus ID on the Bus and asserts $\overline{BSY}$.

PARITY GENERATOR AND CHECKER

This selection generates the parity for the data placed on the SCSI bus by the WD33C92/3-SBIC and checks the parity received from the SCSI bus. Even parity on a byte received from the SCSI bus indicates an error.

SCSI REQ AND ACK HANDSHAKE LOGIC

This logic performs the high-speed handshaking on the SCSI bus. This state machine operates from the 10 MHz input clock and performs either asynchronous or synchronous handshaking as described in the ANSI SCSI specifications.

DATA BUFFER

The Data Buffer is a five-byte FIFO which temporarily holds information until the SCSI bus is ready to accept a transmitted data byte, or the Host is ready to accept a received data byte.

REGISTER FILE

This file consists of 28 registers which hold various parameters and information needed by the WD33C92/3-SBIC to execute commands.

PROCESSOR INTERFACE

Multiplexed or non-multiplexed bus processors are supported by this interface. For non-multiplexed processors, the address of the register to be accessed is first written into the internal Address Register. For multiplexed processors, ALE is used to load the address from the local data bus.

ARITHMETIC LOGIC UNIT (ALU)

The ALU performs the division necessary for the logical-to-physical address translation. It is also used by the WD33C92/3-SBIC internal microcontroller to provide several logical and arithmetic functions.

BYTE COUNTER

This is a 24-bit counter used by the WD33C92/3-SBIC to keep track of how many data bytes are to be sent or received during a data transfer command.

MICROCONTROLLER

The internal microcontroller performs command interpretation and controls the PLA and handshaking logic.

REGISTER FILE

The Register File consists of 28 registers. They function as the logical and physical sector address registers, three ID registers (source device, destination device, and its own), and miscellaneous status and control registers.

For indirect addressing, when A0 = 0 and $\overline{WE}$ is asserted, the Address Register is loaded with the address of the desired register. When A0 = 0, and $\overline{RE}$ is asserted, the Auxiliary Status Register is read. See the Address Register and Auxiliary Register description for details. When A0 = 1, all other registers can be written to or read from, depending on the state of $\overline{WE}$, $\overline{RE}$ and and the contents of the Address Register. Table 1 is a map listing all the registers, their addresses, the state of A0, $\overline{RE}$ or $\overline{WE}$. In every instance $\overline{CS}$ is asserted, therefore it is not listed.

For direct addressing, the state of A0 is ignored and ALE is used to load the Address Register during each cycle prior to the assertion of $\overline{RE}$ or $\overline{WE}$. Therefore, this addressing mode requires only one I/O cycle to randomly access any register in the Register File.

All unused bits of a defined register are reserved and must be set to zero. Reading an undefined or unavailable register results in an output of all ones to the data bus.

ADDRESS REGISTER

The Address Register is a write-only register and counter, used to address a specific register in the Register File.

7	6	5	4	3	2	1	0
0	0	0	AR4				AR0

The address of the first register to be accessed, is written to this register by the local processor/Host data bus (D7 through D0). To write to this register during indirect addressing, A0 must be de-asserted and $\overline{CS}$ and $\overline{WE}$ asserted. During direct addressing, A0, $\overline{WE}$ and $\overline{RE}$ are ignored and the Address Register is written to by the trailing edge of ALE, prior to asserting $\overline{WE}$ or $\overline{RE}$.

The content of the Address Register is incremented by one each time a register in the Register File is accessed. Exceptions to this are the Address, Auxiliary Status, Data, and Command registers.

The Address Register is reset to zero by $\overline{MR}$ but is not affected by the Reset Command.

TABLE 1. REGISTER MAP T-52-33-27

A0	R/W	REGISTER ACCESSED		ADDR. HEX.
0	W	ADDRESS		• •
0	R	AUXILIARY STATUS		• •
1	R/W	OWN ID		0 0
1	R/W	CONTROL		0 1
1	R/W	TIMEOUT PERIOD		0 2
1	R/W	TOTAL SECTORS	/CDB 1	0 3
1	R/W	TOTAL HEADS	/CDB 2	0 4
1	R/W	TOTAL CYLINDERS (MSB)	/CDB 3	0 5
1	R/W	TOTAL CYLINDERS (LSB)	/CDB 4	0 6
1	R/W	LOGICAL ADDRESS (MSB)	/CDB 5	0 7
1	R/W	LOGICAL ADDRESS	/CDB 6	0 8
1	R/W	LOGICAL ADDRESS	/CDB 7	0 9
1	R/W	LOGICAL ADDRESS (LSB)	/CDB 8	0 A
1	R/W	SECTOR NUMBER	/CDB 9	0 B
1	R/W	HEAD NUMBER	/CDB 10	0 C
1	R/W	CYLINDER NUMBER (MSB)	/CDB 11	0 D
1	R/W	CYLINDER NUMBER (LSB)	/CDB 12	0 E
1	R/W	TARGET LUN		0 F
1	R/W	COMMAND PHASE		1 0
1	R/W	SYNCHRONOUS TRANSFER		1 1
1	R/W	TRANSFER COUNT (MSB)		1 2
1	R/W	TRANSFER COUNT		1 3
1	R/W	TRANSFER COUNT (LSB)		1 4
1	R/W	DESTINATION ID		1 5
1	R/W	SOURCE ID		1 6
1	R	SCSI STATUS		1 7
1	R/W	COMMAND		1 8
1	R/W	DATA		1 9

Registers in locations 03 Hex through 10 Hex are used exclusively by the Translate Address and/or Combination Commands, i.e.: Command Codes 08-0C (refer to Table 8). The function of each register is determined by the type of command.

When using direct addressing (Multiplexed Bus with ALE), the Auxiliary Status Register is mapped at 1F Hex.

AUXILIARY STATUS REGISTER

The Auxiliary Status Register is a read-only register containing general information not directly related to the interrupt condition.

When using a multiplexed address/data bus with ALE (direct addressing), this register is mapped at 1F Hex.

This register is reset to zero by the Reset Command.

The AUX STATUS register cannot be accessed during data phase when either $\overline{DACK}$ or $\overline{RCS}$ is active.

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	0	0	PE	DBR

Bit 7 - INT - Interrupt Pending

INT indicates that the INTRQ signal is asserted. The Host must read the SCSI Status Register before issuing any command.

Bit 6 - LCI - Last Command Ignored

LCI indicates that a command issued by the host, just prior to or concurrent with a pending interrupt, was ignored. In the case of a reselection interrupt occurring after a select command is issued, but before the selection process begins, the LCI bit will not be set.

Bit 5 - BSY - BUSY

BSY indicates a level II command is being performed. At this time, only the Command Register (whgen CIP = 0), Data Register, and Auxiliary Status Register are accessible by the Host.

Bit 4 - CIP - Command in Progress

CIP indicates that the WD33C92/3-SBIC is interpreting the command just entered into the Command Register. The Command Register is not accessible to the Host at this time.

Bit 3, 2 Not Used, will be zero

Bit 1 - PE - Parity Error

PE indicates that even parity was detected on the data byte received during a Receive or Transfer Info command. Detection of a parity error sets the PE Status regardless of the state of the Halt On Parity Error (HPE) in the Control Register. PE is reset to zero when a new command is issued.

Bit 0 - DBR - Data Buffer Ready

During Programmed I/O, DBR indicates to the Host that the Data Register is available for reading or writing.

During Send or Transfer Commands, data is transmitted over the SCSI bus from the Data Register. DBR = 1 indicates that the Data Register is in need of a data byte from the local processor/Host. DBR = 0 indicates there is a data byte in the Data Register ready for the SCSI bus.

During Receive or Transfer Commands, data is received over the SCSI bus into the Data Register. DBR = 1 indicates the Data Register has a Data Byte ready for the local processor/Host to read. DBR = 0 indicates the Data Register is empty and needs to be written to by the SCSI bus.

OWN ID REGISTER - Address 00 Hex - $\overline{RE}$ $\overline{WE}$

The encoded SCSI bus address of the WD33C92/3-SBIC is written to the Own ID Register. This register is sampled and becomes effective only after a Reset Command is issued to the WD33C92/3-SBIC. It is set to zero by the power-up reset ($\overline{MR}$) and if any bus ID other than zero is desired it must be loaded with the proper value and sampled with a Reset Command.

7	6	5	4	3	2	1	0
0	0	0	0	0	ID2	ID1	ID0

CONTROL REGISTER - Address 01 Hex - $\overline{RE}$/$\overline{WE}$

The Control Register is used to enable or disable certain halt and select functions. This register is reset to zero upon power-up or by a Reset Command.

7	6	5	4	3	2	1	0
DMA	WDB	0	0	EDI	IDI	HA	HPE

Bit 7 - DMA - DMA Select

DMA must be set when the WD33C92/3-SBIC is interfaced with a DMA controller. The DMA controller transfers data to or from the WD33C92/3-SBIC by asserting $\overline{DAC}$ and $\overline{WE}$ or $\overline{RE}$ in response to $\overline{DRQ}$ being asserted by the WD33C92/3-SBIC.

DMA is valid only during SCSI data transfer, ie: Message, Status, and Command Information require Programmed I/O.

Bit 6 - WDB - WD-Bus Select

WDB must be set when the WD33C92/3-SBIC is operating in the Direct Buffer Access (DBA) mode. This causes the $\overline{RCS}$ to function as an output signal for selecting an external buffer, enables $\overline{WE}$ and $\overline{RE}$ as output signals for the transfer of data, and causes DRQ to function as an input for temporarily halting data transfers.

WDB is valid only durng SCSI data transfer, ie: Message, Status, and Command Information require Programmed I/O.

Bits 4 and 5 are not used and should be set to zero.

Bit 3 - EDI - Ending Disconnect Interrupt

Under normal conditions, when the EDI bit is not set, a select and transfer command will complete with a 16th interrupt followed by an 85h interrupt once the target disconnects.

When the EDI bit is set, the SAT complete interrupt (16h) gets delayed until the target disconnects. The disconnect interrupt (85h) is assumed to be included in the 16h interrupt and will not occur.

Bit 2 - IDI - Intermediate Disconnect Interrupt

This bit is used to notify the SBIC microcontroller to generate an interrupt (85h) when the target disconnects temporarily. Normally the SBIC would remain busy and wait for the target to reselect. This feature allows overlapped SCSI transactions.

Bit 1 - HA - Halt On Attention

The HA bit causes the WD33C92/3-SBIC to terminate a Send or Receive Command when the ATN input is asserted. ATN indicates that the Initiator has a message for the WD33C92/3-SBIC. During synchronous data transfers the HA bit is ignored, therefore Send or Receive Commands are not terminated by the Attention condition.

The HA bit is valid only when the WD33C92/3-SBIC is connected as a Target.

Bit 0 - HPE - Halt On Parity Error

The HPE bit causes the WD33C92/3-SBIC to terminate a Receive or Transfer Command when a Parity Error is detected on an incoming data byte. As the Initiator, termination due to a Parity Error causes the ACK signal to remain in the active state, inhibiting any additional data transfers (REQ) by the Target.

During synchronous data transfers the HPE bit is ignored, therefore Receive and Transfer Commands are not terminated by Parity Errors.

TIMEOUT PERIOD REGISTER - Address 02 Hex - $\overline{RE}$/$\overline{WE}$

The contents of this 1-Byte register controls the timeout period required by the Select and Reselect Commands. The timeout values are in increments of 8 msec (with a 10MHz clock), therefore, a value of FF Hex provides a timeout period of 2.04 seconds. A value of 00 Hex written to this register disables the timeout period.

The timeout period specifies the length of time the WD33C92/3-SBIC waits for BSYI/$\overline{BSY}$ in, following its de-assertion of BSYO/$\overline{BSY}$ out, before terminating the command presently in progress.

This register is reset to zero by the Reset Command.

TOTAL SECTORS REGISTER or CDB BYTE 1 - Address 03 Hex - $\overline{RE}$/$\overline{WE}$

Prior to issuing a Translate Address Command, this register is to be loaded with the total number of sectors per track.

Prior to issuing a Select-And-Transfer Command, this register is to be loaded with the first byte of the Command Descriptor Block.

For the Wait-For-Select-And-Receive Command, the WD33C92/3-SBIC loads the first byte of the Command Descriptor Block in this register.

This register is set to zero by the Reset Command.

TOTAL HEADS REGISTER or CDB BYTE 2 - Address 04 Hex - $\overline{RE}/\overline{WE}$

Prior to issuing a Translate Address Command, this register is to be loaded with the total number of heads.

Prior to issuing a Select-And-Transfer Command, this register is to be loaded with the second byte of the Command Descriptor Block.

For the Wait-For-Select-And-Receive Command, the WD33C92/3-SBIC loads the second byte of the Command Descriptor Block in this register.

This register is set to zero by the Reset Command.

TOTAL CYLINDERS REGISTER or CDB BYTES 3, 4 - Addresses 05, 06 Hex - $\overline{RE}/\overline{WE}$

Prior to issuing a Translate Address Command, this register is to be loaded with the total number of cylinders. The MS Byte should be loaded in address 05 and the LS byte in address 06 Hex.

Prior to issuing a Select-And-Transfer Command, this register is to be loaded with the third byte of the Command Descriptor Block in address 05 and the fourth in address 06 Hex.

For the Wait-For-Select-And-Receive Command, the WD33C92/3-SBIC loads the third byte of the Command Descriptor Block into address 05 and the fourth byte into address 06 Hex.

This register is set to zero by the Reset Command.

LOGICAL ADDRESS REGISTER or CDB 5 thru 8 - Address 07 thru 0A Hex - $\overline{RE}/\overline{WE}$

Prior to issuing a Translate Address Command, this register is to be loaded with the 4-Byte logical sector address. The MS Byte should be loaded in address 07 and the LS byte in address 0A Hex.

SCSI commands requiring a 6-Byte Command Descriptor Block need only have the fifth byte written to address 07 and the sixth to address 08 Hex prior to issuing a Select-And-Transfer Command. It is not necessary to write to addresses 09 or 0A. However, SCSI commands requiring a 10 or 12 byte CDB must have the fifth through eighth bytes written to addresses 07 through 0A Hex.

For the Wait-For-Select-And-Receive Command, the WD33C92/3-SBIC loads the appropriate CDB bytes into addresses 07 through 0A Hex.

This register is set to zero by the Reset Command.

SECTOR NUMBER REGISTER or CDB 9 - Address 0B Hex - $\overline{RE}/\overline{WE}$

The Sector Number resulting from a Translate Address Command is written in this register.

SCSI commands requiring a 10 or 12 byte Command Descriptor Block must have CDM 9 written to address 0B Hex prior to issuing a Select-And-Transfer Command.

For the Wait-For-Select-And-Receive Command, the WD33C92/3-SBIC loads the ninth CDB byte into this register.

This register is set to zero by the Reset Command.

HEAD NUMBER REGISTER or CDB 10 - Address 0C Hex - $\overline{RE}/\overline{WE}$

When the WD33C92/3-SBIC is to perform automatic compensation for spare sectors, the number of spare sectors per cylinder must be written into this register before issuing a Translate Address Command. In this case, the maximum number of cylinders allowed is 4096 and the maximum number of heads is 15. These spare sectors may be reserved for use with Bad-Block-Mapping. Writing 00 Hex to this register indicates that automatic compensation for spare sectors is not to be performed.

The Translate Address Command writes the resulting Head Number to this register.

SCSI commands requiring a 10 or 12 byte Command Descriptor Block must have CDB 10 written to address 0C Hex prior to issuing a Select-And-Transfer Command.

For the Wait-For-Select-And-Receive Command, the WD33C92/3-SBIC loads the tenth CDB byte into this register.

This register is set to zero by the Reset Command.

CYLINDER NUMBER REGISTER or CDB 11, 12 - Address 0D, 0E Hex - $\overline{RE}/\overline{WE}$

A non-zero value in the Head Number Register indicates that automatic compensation is to be performed. The total number of available sectors per cylinder must then be written to this register prior to issuing a Translate Address Command. The total number of available sectors = (number of sectors per track) x (number of cylinders) – (number of spare sectors per cylinder).

The Translate Address Command writes the resulting Cylinder Number to this register.

SCSI commands requiring a 12 byte Command Descriptor Block must have CDB 11 and CDB 12 written to address 0D and 0E Hex prior to issuing a Select-And-Transfer Command.

For the Wait-For-Select-And-Receive Command, the WD33C92/3-SBIC loads the eleventh and twelfth CDB byte into address 0D and 0E Hex.

This register is set to zero by the Reset Command.

TARGET LUN REGISTER - Address OF Hex - $\overline{RE}/\overline{WE}$

7	6	5	4	3	2	1	0
0	0	0	0	0	TL2	TL1	TL0

The Target's Logical Unit Number must be written to this register before issuing a Select-And-Transfer or Reselect-And-Transfer command. These commands use this register during the Identify Message Phase. When the Select-And-Transfer Command completes the Receive Status Phase, the WD33C92/3-SBIC stores the Target Status byte in this register. The Host can read the Status upon completion of the command.

This register is set to zero when a Wait-For-Select-And-Receive Command is issued and is updated with the received message byte during a Message Phase.

This register is set to zero by the Reset Command.

COMMAND PHASE REGISTER - Address 10 Hex - RE/WE

7	6	5	4	3	2	1	0
0	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Bit 7 - Not used, will be zero.

Bit 6 thru 0 - Command Phase 6 thru Command Phase 0

In this register the Select-And-Transfer, Reselect-And-Transfer, and Wait-For-Select-And-Receive commands indicate which phase has been completed. If one of these multi-phase commands terminates abnormally, the Host can read this register and determine the cause of the termination and how to respond to it. Refer to the description of the specific commands for details regarding the command phases.

This register is set to zero by the Reset Command.

SYNCHRONOUS TRANSFER REGISTER - Address 11 Hex RE/WE

The Synchronous Transfer Register serves two functions. First, bits 6 thru 4 establish the minimum transfer cycle time (transfer period) for synchronous SCSI transfers and the pulse width of RE/WE strobes during DBA transfers. Although the selected transfer period determines the maximum rate at which the WD33C92/3 generates REQ/ACK pulses in synchronous mode, REQ/ACK can be input to the WD33C92/3 at any rate providing the specification in Tables 43-50 are satisfied. Second, bits 2 thru 0 (offset) establish the size of the "REQ Burst", ie: the maximum number of REQ's allowed out standing without an ACK in response.

Asynchronous transfers occur for information phases other than a data transfer phase, or when the offset is zero.

7	6	5	4	3	2	1	0
0	TP2	TP1	TP0	0	OF2	OF1	OF0

Bit 7 **Not used, must be 0**

Bit 6 - 4 **TP2, TP1, TP0 - Transfer Period 2, 1, 0**

TP2, 1, and 0 select the transfer period as shown in Table 2.

Note: The minimum SCSI bus cycle times apply to DBA mode only. If DMA or Programmed I/O is being used, the resulting minimum cycle time is 1 CLK cycle less than shown in Table 2.

TABLE 2. TRANSFER PERIODS

TP2	TP1	TP0	SCSI Bus Cycle Time	DBA Mode RE/WE width
0	0	X	8 CLK Cycles	4 CLK Cycles
0	1	0	*2 "	1 "
0	1	1	3 "	1 "
1	0	0	4 "	2 "
1	0	1	5 "	3 "
1	1	0	6 "	4 "
1	1	1	7 "	4 "

*This setting is only allowed when DBA is selected.

Bit 2 - 0 **OF2, OF1, OF0 - Offset 2, 1, 0**

OF2, 1, and 0 select the desired Offset as follows:

TABLE 3. OFFSET

OF2	OF1	OF0	OFFSET
0	0	0	0 Selects Asynchronous transfers
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	not valid

This register is set to zero by the Reset Command.

TRANSFER COUNT REGISTER - Address 12 thru 14 Hex - RE WE

The Transfer Count Register is a 24-bit down counter. The number of data bytes to be transferred by a Send, Receive, or Transfer Command must be written into this register prior to issuing the command. As each data byte is transferred the counter is decremented by one. When the counter reaches zero, a "Successful Completion" interrupt is asserted.

The function of this counter can be inhibited by presetting it to zero or by setting the Single-Byte transfer bit in the Command Register, prior to or concurrent with issuing the command. When the Transfer Counter is disabled, the Send, Receive, or Transfer Command terminates when a single byte has been transferred.

This register is set to zero by the Reset Command.

DESTINATION ID REGISTER - Address 15 Hex - RE/WE

The encoded SCSI ID of the device to be selected or reselected by a Select or Reselect command is written into this register.

7	6	5	4	3	2	1	0
0	0	0	0	0	DI2	DI1	DI0

Bits 7 thru 3 - Not used, must be zero.

Bits 2 thru 0 - The encoded SCSI ID, 0 thru 7.

This register is set to zero by the Reset Command.

SOURCE ID REGISTER - Address 16 Hex - $\overline{RE}/\overline{WE}$

The Source ID Register contains the encoded SCSI bus ID of the device that last selected the WD33C92/3-SBIC, providing the Source ID Valid (SIV) bit is set, indicating that it also asserted its ID during the Selection or Reselection Phase. If the SIV bit is not set following a Selected or Reselected interrupt, the Source ID is not valid.

This register also provides an enable/disable bit for selecting or reselecting the WD33C92/3-SBIC.

7	6	5	4	3	2	1	0
ER	ES	DSP	0	SIV	SI2	S/1	SI0

Bit 7 - ER - Enable Reselection

Bit 6 - ES - Enable Selection.

Bit 5 - DSP - Disable Select/Resel Parity

This bit will cause the SBIC to ignore the SCSI bus parity while an attempt to select or reselect it is being made. This should therefore be used in systems which do not support parity.

For systems which support parity on the SCSI bus, bit 5 should be zero. This bit has been added despite the existence of the Halt on Parity Error bit in the CONTROL register (bit 0) in order to provide a separate control for parity during selection or reselection and during data transfers. Since a parity error status is always given in the AUXILIARY STATUS register, in certain situations it may be desirable to not use the HPE feature, despite the fact that parity is supported in the system.

In short, the new DSP bit will allow parity support during the sel/resel process independent of the impact of parity errors on data transfers.

Bit 4 - Not used, must be zero.

Bit 3 - SIV - Source ID Valid

The source device asserted its ID during selection or reselection.

Bits 2 thru 0 - S12 thru S10

The encoded SCSI ID of the last device to select or reselect the WD33C92/3-SBIC.

This register is set to zero by the Reset Command.

SCSI STATUS REGISTER - Address 17 Hex - $\overline{RE}$

The SCSI Status Register is a read-only register representing the condition at the time of the last Interrupt (INTRQ). Bits 7 thru 4 each represent one of four major reasons for the INTRQ, bits 3 thru 0 further define the condition within the major group. When a INTRQ has occurred and the status has been placed in this register, the register is not reset until another command is issued.

7	6	5	4	3	2	1	0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 7 - SS7 - SCSI Status Group Four

Another bus device needs service.

Bit 6 - SS6 - SCSI Status Group Three

A WD33C92/3-SBIC command terminated prematurely due to an error or unexpected condition.

Bit 5 - SCSI Status Group Two

A WD33C92/3-SBIC command paused or was aborted.

Bit 4 - SS4 - SCSI Status Group One

A WD33C92/3-SBIC command completed successfully.

Bit 3 thru 0 - SS3 thru SS0

SS3 thru SS0 further qualify the status within a particular group.

This register is set to zero by the Reset Command.

TABLE. SCSI STATUS CODES, SUCCESSFUL COMPLETION INTERRUPT

SSSS SSSS 7654	SS SS 32 10	DEFINITION
0000	00 00	Reset by command or power-up (MR—)
0001	00 00	A Reselect Command completed successfully.
0001	00 01	A Select Command completed successfully.
0001	00 11	A Receive, Send, Reselect-And-Transfer, or Wait-For Select-And-Receive Command completed successfully (ATN is not asserted).
0001	01 00	A Receive, Send, Reselect-And-Transfer, or Wait-For Select-And-Receive Command completed successfully (ATN is asserted).
0001	01 01	A Translate Address Command completed successfully.
0001	01 10	A Select-And-Transfer Command completed successfully.
0001	1M CI	A Transfer Command (not a Message-in phase) completed successfully. MCI = Message, C/D, I/O and defines the type of information being requested. See Table 12-13.

TABLE 5. SCSI STATUS CODES, PAUSE OR ABORTED INTERRUPT

SSSS 7654	SSSS 3210	DEFINITION T-52-33-27
0010	0000	A Transfer Command (Message-In phase) has paused with ACK asserted.
0010	0001	A Save Data Pointers message was received during a Select-And-Transfer Command.
0010	0010	A Select or Reselect Command was aborted.
0010	0011	A Receive or Send Command has halted or was aborted (ATN is not asserted).
0010	0100	A Receive or Send Command has halted or was aborted (ATN is asserted).
0010	1MCI	A Transfer Command was aborted. M C I = Message, C/D, I/O and defines the type of information being requested. See Table 12-13.

TABLE 6. SCSI STATUS CODES, TERMINATED INTERRUPT

SSSS 7654	SSSS 3210	DEFINITION
0100	0000	An invalid command was issued.
0100	0001	An unexpected disconnect caused a command to terminate.
0100	0010	A time-out occurred during a Select or Reselect Command.
0100	0011	A Parity Error caused a command to terminate (ATN is not asserted).
0100	0100	A Parity Error caused a command to terminate (ATN is asserted).
0100	0101	The Logical Address exceeded the disk boundaries.
0100	0110	The wrong Target device reselected the WD33C92/3-SBIC.
0100	0111	An incorrect message, status, or command byte was received.
0100	1MCI	An unexpected information phase was requested. M C I = Message, C/D, I/O and defines the type of information being requested. See Table 12-13.

TABLE 7. SCSI STATUS CODES, SERVICE REQUIRED INTERRUPT

SSSS 7654	SSSS 3210	DEFINITION
1000	0000	The WD33C92/3-SBIC has been reselected.
1000	0010	The WD33C92/3-SBIC has been selected (ATN is not asserted).
1000	0011	The WD33C92/3-SBIC has been selected (ATN is asserted).
1000	0100	The ATN signal has been asserted.
1000	0101	A Disconnect has occurred.
1000	1MCI	The REQ signal has been asserted following connection and the information phase type should be examined. M C I = Message, C/D, I/O and defines the type of information being requested. See Table 12-13.

The interrupts that contain the signals MCI to denote the requested SCSI bus phases define them according to logical levels as defined in the ANSI SCSI standard.

The MCI definitions are summarized below:

MSG	C/D	I/O	BUS PHASE	MSG	C/D	I/O	BUS PHASE
0	0	0	Data out to target	1	0	0	Reserved
0	0	1	Data in from target	1	0	1	Reserved
0	1	0	Command to target	1	1	0	Message out to target
0	1	1	Status from target	1	1	1	Message in from target

COMMAND REGISTER - Address 18 Hex - $\overline{RE}/\overline{WE}$

7	6	5	4	3	2	1	0
SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Bit 7 - SBT - Single-Byte Transfer

The SBT is only used during information transfer type commands. This bit, being set in conjunction with an information transfer command, disables the transfer counter and only one byte is transferred regardless of the value in the Transfer Count Register.

Bits 6 thru 0 - CC6 thru CC0 - Command Code 6 thru 0

Commands to be performed by the WD33C92/3-SBIC are written into bits 6 thru 0 of the Command Register. The WD33C92/3-SBIC expects the SCSI Status to have been read before the Host issues another command. Therefore, to avoid setting the LCI Status in the Auxiliary Status Register, there must be at least a seven usec. delay between the time the SCSI Status Register is read and the time the next command is loaded into the Command Register.

This register is set to zero by the Reset Command.

DATA REGISTER - Address 19 Hex - $\overline{RE}/\overline{WE}$

7	6	5	4	3	2	1	0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

The Data Register transfers data between the local processor/Host and SCSI bus during SCSI information transfer phases (command, data, status, or message phase). It may be accessed by the local processor/Host during any type of information phase, or via the DMA/WDB interface during a data phase.

The local processor/Host accesses the Data Register when the DMA and WDB bits in the Control Register are both zero, or when the information phase involves other than data transfers.

The DMA Controller accesses the Data Register when the DMA bit in the Control Register is one. The Data Register is then written to or read from when $\overline{DACK}$ and $\overline{WE}$ or $\overline{RE}$ are asserted in response to WD33C92/3-SBIC asserting $\overline{DRQ}$.

The WD33C92/3-SBIC accesses the Data Register in the DBA mode when the WDB bit in the Control Register is one. In this mode of operation $\overline{RCS}$ accesses the external buffer and $\overline{WE}$ and $\overline{RE}$ become output signals, allowing automatic data transfers between the Data Register and the external buffer. In this mode, bus control is returned to the local processor/Host or any other device by de-asserting DRQ. The transfer is then terminated by issuing an Abort Command or can be resumed by asserting DRQ.

The DBR Status within the Auxiliary Status Register is used by the local processor/Host during programmed I/O to determine when the Data Register is ready for reading or writing.

The Data Register is not affected by a Reset Command or by $\overline{MR}$

COMMAND DESCRIPTION

The WD33C92/3-SBIC commands are divided into two basic categories, Level I and Level II. Level I commands may be issued while a Level II command is being executed, as indicated by BSY = 1 and CIP = 0 in the Auxiliary Status Register. If a second Level II command is issued before the completion of the first, the second Level II command is ignored. Except for the abort and Reset Commands, Level I commands do not produce an Interrupt signal upon their completion while Level II commands always produce an Interrupt signal.

The WD33C92/3-SBIC operates in one of three modes: Disconnected, Target mode, or Initiator mode. Some commands are valid only when the WD33C92/3-SBIC is in a particular mode, as indicated in Table 8. Issuing a Level II command that is not valid for the mode in which the WD33C92/3-SBIC is operating at the time, results in an Invalid Command Interrupt (Status 40 Hex in the Status Register). Level I commands issued while the WD33C92/3-SBIC is in an invalid state are ignored.

TABLE 8. COMMAND LIST

COMM CODE (HEX)	COMMAND	VALID STATES	LEVEL
00	Reset	D T I	I
01	Abort	D T I	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T I	I
05	Reselect	D	II
06	Select-With-ATN	D	II
07	Select-Without-ATN	D	II
08	Select-With-ATN-And-Transfer	D	II
09	Select-Without-ATN-And Transfer	D	II
0A	Reselect-And-Receive Data	D	II
0B	Reselect-And-Send Data	D	II
0C	Wait-For-Select-And-Receive	D	II
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D T	II
20	Transfer Info	I	II
21	Transfer Pad	I	II

WD33C92/3-SBIC States:

D = Disconnected
T = Selected as a Target
I = Selected as an Initiator

RESET - Com. Code 00 - Valid Mode D, T, I - Level I

The Reset Command and $\overline{MR}$ asserted at power-up perform the same functions, with the following exceptions. The Own ID Register is sampled but not changed by the Reset Command while the Address and Data Registers are not initialized by the Reset Command. All other registers are initialized as described in the Register Description Section.

The Reset Command is valid in any mode of operation. When issued while another command is being executed, that command is aborted and the WD33C92/3-SBIC is placed in the Disconnected State. Upon completion of the Reset Command an interrupt is generated with a SCSI Status of 00 Hex.

ABORT - Com. Code 01 - Valid Mode D, T, I - Level I

When issued during the disconnected state, Abort halts an active selection or reselection attempt by the WD33C92/3-SBIC.

When the WD33C92/3-SBIC has not yet won arbitration, the Select and Reselect Commands are aborted immediately. Otherwise, the Abort Command releases the SCSI bus by removing the Bus ID bits and while still asserting SELO/$\overline{SEL}$, checks the BSYI/$\overline{BSY}$ signal. When BSYI/$\overline{BSY}$ is asserted before a 200 usec. period has elapsed, the selection or reselection has completed successfully and a Successful Completion Status (10, 11 Hex) is placed in the SCSI Status Register. When the 200 usec. period expires before BSYI/$\overline{BSY}$ is asserted, a Pause/Abort Status (22 Hex) is placed in the SCSI Status Register.

When the WD33C92/3-SBIC is connected as an Initiator or Target, it is possible to abort the Receive, Send, and Transfer Commands. The WD33C92/3-SBIC remains in its selected mode of operation and the Transfer Counter retains the number of bytes not yet transferred at the time of the abort. Therefore, the aborted command can be restarted simply by reissuing the command.

ASSERT ATN - Com. Code 02 - Valid Mode I - Level I

The Assert ATN Command is used to inform the Target that a message is pending. The Target should respond by performing a Message Out Command which causes the WD33C92/3-SBIC to automatically de-assert ATN upon completion of the message transfer.

The Select-With-ATN command causes the WD33C92/3-SBIC

to automatically assert ATN during selection, providing the bus arbitration is won.

NEGATE ACK - Com. Code 03 - Valid Mode I - Level I

The Negate ACK command is used following a Message-In transfer or when a Parity Error is detected on any received information, with the HPE bit in the Control Register set. For all other Initiator transfers, ACK is de-asserted automatically.

During Message-In transfers, the incoming message can be rejected and the Initiator indicate its intent to send either a Message-Reject or Message-Parity-Error by issuing the Assert-ATN command prior to issuing the Negate-ACK command. If the incoming message is to be accepted, only the Negate-ACK command is issued.

During other than Message-In transfers, if the Transfer Command is terminated due to a Parity Error, the Assert-ATN is generally issued prior to the Negate-ACK Command, indicating the Initiator's intent to send an Initiator Detected Error Message.

DISCONNECT - Com. Code 04 - Valid Mode T, I - Level I

In the Target Mode, the Disconnect Command is the normal method used to disconnect from the SCSI bus following an Information Transfer Phase.

In the Initiator Mode, the Disconnect command is generally used to release WD33C92/3-SBIC from the SCSI bus following a Timout condition. The Disconnect Command immediately releases all SCSI bus signals driven by the WD33C92/3-SBIC.

When the Disconnect Command is issued during the execution of a Level II command, the Level II command terminates immediately and the WD33C92/3-SBIC switches to the Disconnected Mode.

RESELECT - Com. Code 05 - Valid Mode D - Level II

The Reselect Command causes the WD33C92/3-SBIC to switch to the Target Mode of operation. Therefore, the SCSI bus ID of the Initiator device must be written into the Destination ID Register before issuing this command. When the Reselect Command is issued, the WD33C92/3-SBIC begins bus arbitration.

When the WD33C92/3-SBIC completes the arbitration successfully, SELO/$\overline{\text{SEL}}$ and I/O are asserted, the Target and Initiator IDs are placed on the SCSI Data Bus, and BSYO/$\overline{\text{BSY}}$ is de-asserted. The Timeout sequence now starts. The length of the timeout period is determined by the value placed in the Timeout Period Register prior to issuing the Reselect Command.

When the Initiator responds before the timeout period has elapsed or before the abort sequence is complete, the WD33C92/3-SBIC asserts the BSYO/$\overline{\text{BSY}}$ and then negates SELO/$\overline{\text{SEL}}$, putting the WD33C92/3-SBIC in a Target Mode of operation. A Successful Completion Status (10 Hex) is placed in SCSI Status Register, indicating that the command has completed successfully.

When the WD33C92/3-SBIC is selected or reselected by another device, the Reselect command is aborted and a Service Required Interrupt Status (80, 82, or 83 Hex) is placed in the SCSI Status Register.

When BSYI/$\overline{\text{BSY}}$ is not asserted by the Initiator before the end of the timeout period, the WD33C92/3-SBIC starts aborting the selection as described in the Abort Command. When there is still no response by the Initiator, the Reselect is terminated with a Terminated Interrupt Status (42 Hex) placed in the SCSI Status Register.

When the WD33C92/3-SBIC does not complete the arbitration successfully or there is no response from the Initiator and the timeout feature is disabled, the Reselect Command must be aborted with an Abort Command. Upon successful completion of the Abort Command, the WD33C92/3-SBIC disconnects from the bus and a Paused/Abort Status (22 Hex) is placed in the SCSI Status Register.

T-52-33-27

SELECT-WITH-ATN - Com. Code 06 - Valid Mode D - Level II

The Select-With-ATN causes the WD33C92/3-SBIC to switch to the Initiator Mode of operation. Therefore, the SCSI bus ID of the Target device must be written into the Destination ID Register before issuing this command. When the Select-With-ATN Command is issued, the WD33C92/3-SBIC begins bus arbitration.

When the WD33C92/3-SBIC completes the arbitration successfully, SELO/$\overline{\text{SEL}}$ and ATN/$\overline{\text{ATN}}$ are asserted, the Target and Initiator IDs are placed on the SCSI Data Bus, and the BSYO/$\overline{\text{BSY}}$ is de-asserted. The Timeout sequence now starts. The length of the timeout period is determined by the value placed in the Timeout Period Register prior to issuing the Select-With-ATN Command.

When the Target responds before the timeout period has elapsed or before the abort sequence is complete, the WD33C92/3-SBIC negates SELO/$\overline{\text{SEL}}$, putting the WD33C92/3-SBIC in an Initiator Mode of operation. A Successful Completion Status (11 Hex) is placed in the SCSI Status Register, indicating that the command has completed successfully.

When the WD33C92/3-SBIC is selected or reselected by another device during arbitration, the Select-With-ATN command is aborted and an Service Required Interrupt Status (80, 82, or 83 Hex) is placed in the SCSI Status Register.

When BSYI/$\overline{\text{BSY}}$ is not asserted by the Target before the end of the timeout period, the WD33C92/3-SBIC starts aborting the selection as described in the Abort Command. When there is still no response by the Target, the Select-With-ATN is terminated with a Terminated Interrupt Status (42 Hex) placed in the SCSI Status Register.

When the WD33C92/3-SBIC does not complete the arbitration successfully or there is no response from the Target and the timeout feature is disabled, the Select-With-ATN must be aborted with an Abort Command.

Upon successful completion of the Abort Command, the WD33C92/3-SBIC disconnects from the SCSI bus and a Paused/Abort Status (22 Hex) is placed in the SCSI Status Register.

T-52-33-27

SELECT-WITHOUT-ATN - Comm. Code 07 - Valid Mode D- Level II

Select-Without-ATN is identical to the Select-With-ATN Command, except that ATN is not asserted during the Selection Phase.

SELECT-AND-TRANSFER - Comm. Codes 08, 09 - Valid Mode D - Level II

The Select-And-Transfer Commands greatly reduce the processor interrupt-handling burden by chaining at least four SBIC commands together and creating an interrupt only after the final phase is completed or upon an abnormal condition.

Select-And-Transfer Commands cause the transition of a disconnected WD33C92/3-SBIC into the Initiator state. These commands consist of the following phases, Selection of a Target Device, Send a Command, Receive Status Information, and Receive a Command Complete Message, and may optionally include a Data Transfer Phase and several additional Message Transfer Phases.

When a Target disconnects during a Select-And-Transfer Command after sending a Disconnect Message, but without sending a Save Data Pointer message, execution is not terminated unless a different device attempts to Select or Reselect the WD33C92/3-SBIC. If the original Target is the first device to Reselect the WD33C92/3-SBIC, the Select-And-Transfer Command continues with the appropriate information transfer phase. Upon the completion or termination of a command, the Command Phase Register can be examined to determine which phase was the last to be completed by the Select-And-Transfer Command. Refer to Table 9 for the possible Command Phase Codes.

The Select-And-Transfer Commands differ only by whether or not they assert the ATN signal during the Selection phase. Select-And-Transfer Commands support group 0, 1, and 5 SCSI commands (6, 10, and 12 byte CDBs respectively). The ability to assert the ATN signal during the Selection phase supports the SCSI message protocol requiring an Identify Message Out phase following the selection.

During a Select-With-ATN-And-Transfer Command the WD33C92/3-SBIC expects the first Information Request Phase from the Target to be a Message Out Phase. The first Information Request Phase of a Select-Without-ATN-And-Transfer Command is expected to be a Send Command Phase.

Selection Phase

Just as in a Select Command, when either Select-And-Transfer Command is issued, the WD33C92/3-SBIC arbitrates for the bus and selects a Target. When the selection is successful, no interrupt is generated and the Command Phase Register Contains 10 Hex. If the Target does not respond, the Select-And-Transfer Command terminates, a Terminated Interrupt Status (42 Hex) is placed in the SCSI Status Register, and the Command Phase Register contains 00 Hex.

Information Transfer Phase - Identify Message Out

Following the Selection Phase, the WD33C92/3-SBIC starts an Information Transfer Phase. If the ATN has been included in the command, the Target requests a Message Out Phase and the WD33C92/3-SBIC responds by sending an Identify Message. This message consists of 1r00 0ttt. r equals the state of the Enable Reselect bit in the Source ID Register, ttt equals Logical Unit Number from the Target LUN Register. Upon completion of the Identify Message the WD33C92/3-SBIC places 20 Hex in the Command Phase Register.

When the first Information Phase Request is anything other than a Message Out request, the WD33C92/3-SBIC terminates the command and places a Terminated Interrupt Status (48 - 4F Hex) in the SCSI Status Register.

Information Transfer Phase - Send Command

The Send Command Phase follows the Selection Phase when ATN has not been included in the command, and follows the Message Out Phase when ATN has been included. The WD33C92/3-SBIC examines the SCSI command located in the internal Command Descriptor Block (CDB 1). Depending on the Group Code of the SCSI command, the WD33C92/3-SBIC sends the 6, 10, or 12 command descriptor bytes required by the SCSI command from the CDB 1 through CDB 12 Registers. The Command Phase Register is set to 30 Hex before the first CDB byte is sent and increments by one each time a byte is transferred. Therefore, the content of the Command Phase Register at the end of this phase will be either 36, 3A, or 3C Hex.

As before, and throughout the entire Select-And-Transfer command, if the Target requests an unexpected phase type, the WD33C92/3-SBIC terminates the command and places a Terminated Interrupt Status (48 - 4F Hex) in the SCSI Status Register.

Information Transfer Phase - Disconnect Message In

Following a Send Command Phase the WD33C92/3-SBIC expects either a Receive Data, Send Data, Receive Status, or Message In Phase. When the Target requests a Message In Phase, a pending disconnection is assumed.

The WD33C92/3-SBIC, therefore, expects to receive either a Save Data Pointer Message (02 Hex) or a Disconnect Message (04 Hex). When a correct Save Data Pointer Message is received, a Paused/Abort Status (21 Hex) is placed in the SCSI Status Register and the Select-And-Transfer Command terminates, allowing the Host to save the SCSI pointers. However, when a Disconnect Message is received, the Command Phase Register is updated to 42 Hex and the command continues. When Target-disconnection does occur, the Command Phase Register is updated to 43 Hex and the WD33C92/3-SBIC switches to the disconnected state until the Target reconnects.

The Save Data Pointer and Disconnect Messages are not normally passed on to the Host, but if either is incorrect, a different message is received, or the Target disconnects before sending the Disconnect Message, a Terminated Interrupt Status (48 - 4F Hex) is placed in the SCSI Status Register to alert the Host and allow the message to be read.

Information Transfer Phase - Identify Message In

When the original Target Reselects the WD33C92/3-SBIC, no interrupt is generated and the Command Phase Register is updated to 44 Hex. The Target then sends the WD33C92/3-SBIC an Identify Message, and the Command Phase Register is updated to 45 Hex. If the LUN contained in the Identify Message is not equal to that in the Target LUN Register, indicating that a different Target has reselected the WD33C92/3-SBIC (1000 0ttt, ttt = the Target LUN), an interrupt is generated, and a Terminated Interrupt Status (48 - 4F Hex) is placed in the SCSI Status Register.

Information Transfer Phase - Receive/Send Data

A Receive Data, Send Data or Receive Status Phase follows an Identify Message Phase if there had been a disconnect, or a Send Command Phase if no disconnect occurred.

When the Transfer Count Register contains a quantity other than zero, the WD33C92/3-SBIC enters a Data Transfer Phase and uses this count to control the number of bytes transferred. The Data Register is accessed via the DMAC or WD local data bus depending on whether the DMA or WDB bit is set in the Control Register. When the Transfer Count Register reaches zero the Data Transfer Phase terminates and the Command Phase Register is updated to 46 Hex.

The WD33C92/3-SBIC may disconnect and reconnect any number of times during a Data Transfer Phase, providing the defined message protocol is followed. The Command Phase Register cycles through the disconnect and reconnect phases (41 - 45 Hex) until all data has been transferred and the Data Transfer Phase is completed (46 Hex).

Information Transfer Phase - Receive Status

The WD33C92/3-SBIC enters the Receive Status Phase from the Command Phase or the Identify Message Phase if the Transfer Count Register had not been preset to a quantity greater than zero, or from the Data Transfer Phase when it reaches zero if it had been preset.

The received status is placed in the Target LUN Register where it can be read by the Host upon completion of the command. When the Receive Status Phase is completed a 50 Hex is placed in the Command Phase Register.

Information Transfer Phase - Command Complete Message In

The Target signals the end of the SCSI command by sending a Command Completed Message (00 Hex). Upon receipt of this message the WD33C92/3-SBIC updates the Command Phase Register to 60 Hex, places a Successful Completion Status (16 Hex) in the SCSI Status Register and creates an interrupt. The Host should then examine the Target Status in the Target LUN Register. Under normal circumstances, once the Select-And-Transfer Command has been issued, the only Host intervention required by the WD33C92/3-SBIC is to read the Target Status after the SCSI Command, Message, Data and Status information has been transferred.

When the WD33C92/3-SBIC experiences an abnormal or unexpected condition during the execution of the Select-And-Transfer Command, the command terminates, generates an Interrupt, and places the appropriate Terminated Interrupt Status in the SCSI Status Register. Unless the termination is caused by a sudden Target disconnect, the WD33C92/3-SBIC is left in the Initiator mode of operation when the termination occurs during an Information Transfer Phase. Termination during any other phase leaves the WD33C92/3-SBIC in the disconnected state.

T-52-33-27

TABLE 9.
SELECT-AND-TRANSFER COMMAND PHASE CODES

CODE	DESCRIPTION
00	Selection not successful
10	Selection successful
20	Identify message sent
30	Start of CDB transfers
36	6 CDB transfers made
3A	10 CDB transfers made
3C	12 CDB transfers made
41	Message, Data or Status Phase is requested
42	Disconnect message received
43	Target disconnected
44	Original Target reselected
45	Correct Identify (right LUN) message received
46	Data transfer completed
50	Status byte received
60	Command Complete message received

RESELECT-AND-TRANSFER - Comm. Codes 0A, 0B - Valid Mode D - Level II

The Reselect-And-Receive-Data and Reselect-And-Send-Data Commands eliminate the interrupt following the Reselection Phase, and cause the WD33C92/3-SBIC to send an Identify Message to the Initiator, followed by the execution of an implied Receive Data or Send Data Command. Upon successful completion of the command, a Successful Completion Status (13 or 14 Hex) is placed in the SCSI Status Register and an interrupt is generated.

A reselection timeout (Status 42 Hex), ATN asserted before data transfers start (Status 84 Hex), or a Parity Error on a received data byte with HPE bit set in the Control Register (Status 43, 44 Hex), causes the command to terminate and place the appropriate status in the SCSI Status Register. The local processor/Host should examine the Command Phase Register to determine the last phase successfully completed. Refer to Table 10 for the possible Command Phase Codes. 10 Hex indicates a successful reselection, 20 Hex indicates the Identify Message was successful and the data transfer started.

TABLE 10.
RESELECT-AND-TRANSFER COMMAND PHASE CODES

CODE	DESCRIPTION
00	Reselection not successful
10	Reselection successful
20	Identify message sent (data transfer started)

WAIT-FOR-SELECT-AND-RECEIVE - Com. Code 0C - Valid Mode D - Level II

The Wait-For-Select-And-Receive command eliminates the interrupt that normally occurs following a selection. The WD33C92/3-SBIC is idle until selected by an Initiator, at which time one or two implied Receive Commands are executed to fetch the SCSI command.

When the Initiator asserts ATN during the Selection Phase, the WD33C92/3-SBIC must first get the Initiator Identify Message and store it in the Target LUN Register located at address 0F Hex. To do this an implied Receive Message Out Command is executed, prior to the implied Receive Command.

The Implied Receive Command fetches the SCSI Command Descriptor Block and writes it into the CDB Registers in location 03 through 0E Hex. The number of bytes transferred by the Receive Command is determined by the Group Code in the first byte of the CDB. Group 0, 1, or 5 will transfer 6, 10, or 12 bytes respectively. The Command Phase Register is preset to 30 Hex at the start of the Message Phase and is incremented by one as each CDB byte is written to the CDB Register. Upon successful completion of the command, the Command Phase Register contains 36, 3A, or 3C depending on the SCSI command, and a Successful Completion Status (13, 14 Hex) is placed in the SCSI Status Register. Refer to Table 11 for the possible Command Phase Codes.

When the message or command information is invalid, the implied receive command is terminated and the appropriate status stored in the SCSI Status Register. The local processor/Host should then read the Command Phase Register to determine the last successful phase prior to the error. 10 Hex indicates the WD33C92/3-SBIC was selected successfully. 20 Hex indicates that the message was received from the Initiator and any count from 30 to the valid number of CDB bytes, indicates the number of CDB bytes received before the error.

TABLE 11.
WAIT-FOR-SELECT-AND-RECEIVE PHASE CODES

CODE	DESCRIPTION
00	WD33C92/3-SBIC is not yet selected
10	WD33C92/3-SBIC is selected successfully
20	Identify message received
30	Start of CDB transfers made
36	6 CDB transfers made
3A	10 CDB transfers made
3C	12 CDB transfers made

RECEIVE - Com. Code 10, 11, 12, 13 - Valid Mode T - Level II

The Receive-Command, Receive-Data, Receive-Message-Out, and Receive-Unspecified-Info-Out Commands differ only in the type of information transferred and how they control the SCSI interface signals I/O, C/D and MSG. Table 12 shows the state of each signal as controlled by the respective command.

TABLE 12. I/O, C/D, MSG DURING RECEIVE

COMMAND	WD33C92			WD33C93		
	I/O	C/D	MSG	I/O	C/D	MSG
Receive Command	0	1	0	1	0	1
Receive Data	0	0	0	1	1	1
Receive Message Out	0	1	1	1	0	0
Receive Unspecified Info Out	0	0	1	1	1	0

As with all commands involving data transfer, the Receive Data Command uses the DMA and WDB bits in the Control Register to determine which device has access to the Data Register. WDB = 1 for DBA mode, DMA = 1 for a DMA Controller, WDB = 0 and DMA = 0 for the local processor/Host.

When the local processor/Host has access to the Data Register, it must monitor the Data Buffer Ready (DBR) in the Auxiliary Status Register to determine when to read the Data Register. DBR is reset when the Receive Command is issued. When the Data Register is written to by the SCSI bus, the DBR bit is set (DBR = 1), indicating to the local processor/Host that a data byte is available. When the local processor/Host reads this data byte from the Data Register, DBR is reset (DBR = 0), indicating that the SCSI bus is required to write another data byte to the Data Register.

Data Information Phases may involve synchronous transfers as determined by the contents of the Synchronous Transfer Register. An offset (OF2 - OF0) of 1 through 5 results in that number of "REQ Burst" transfers, and an Offset of 0 specifies asynchronous data transfers. The Transfer Period is determined by the TP bits in the Synchronous Transfer Register. All Information Phases other than Data Transfers are Asynchronous.

The completion or termination of a Receive Command may be caused by any of the following events:

- $\overline{MR}$ has been asserted.
- A Reset Command has been issued by the local processor/Host.
- The Single Byte Transfer (SBT) bit in the Command Register equals one, or the Transfer Count Register has been set to zero, and a byte has been read from the Data Register.
- SBT = 0, and the Transfer Counter has decremented to zero, indicating that the desired number of bytes have been transferred.
- During an Asynchronous transfer with the Halt on Parity

Error bit (HPE) set in the Control Register, a Parity Error has occurred on the received data byte.
- During an Asynchronous transfer with the Halt on Attention bit (HA) set in the Control Register, the ATN/$\overline{ATN}$ signal has been asserted.
- An Abort Command has been issued.
- A Disconnect Command has been issued.

When the command terminates as a result of transferring the correct number of bytes, a Successful Completion Status (13, 14 Hex) is placed in the SCSI Status Register. When a Parity Error occurs, a Terminated Interrupt Status is placed in the SCSI Status Register (43, 44 Hex). The last byte read from the Data Register is the one with the Parity Error, and the Transfer Count Register represents the number of remaining bytes to be transferred.

Except when terminated by a Disconnect or Reset Command, the WD33C92/3-SBIC remains in the Target Mode of operation upon completion of the Receive Commands.

SEND - Com. Code 14, 15, 16, 17 - Valid Mode T - Level II

The Send-Status, Send-Data, Send-Message-In, and Send-Unspecified-Info-In Commands differ only in the type of information transferred and how they control the SCSI interface signals I/O, C/D, and MSG. Table 13 shows the state of each signal as controlled by the respective command.

TABLE 13. I/O, C/D, MSG DURING SEND

COMMAND	WD33C92			WD33C93		
	I/$\overline{O}$	C/$\overline{D}$	MSG	I/$\overline{O}$	C/$\overline{D}$	$\overline{MSG}$
Send Status	1	1	0	0	0	1
Send Data	1	0	0	0	1	1
Send Message In	1	1	1	0	0	0
Send Unspecified Info In	1	0	1	0	1	0

As with all commands involving data transfer, the Send Data Command makes use of the DMA and WDB bits in the Control Register to determine which device has access to the Data Register. WDB = 1 for DBA mode, DMA = 1 for a DMA Controller, WDB = 0 and DMA = 0 for the local processor/Host.

When the local processor/Host has access to the Data Register, it must monitor the Data Buffer Ready status (DBR) in the Auxiliary Status Register to determine when to write to the Data Register. DBR is set (DBR = 1) when the Send Command is issued and each time the content of the Data Register is transferred across the SCSI bus, indicating to the local processor/Host that the Data Register is in need of a Data Byte. When the local processor/Host writes a data byte to the Data Register DBR is reset (DBR = 0), indicating that the Data Register has another data byte available for the SCSI bus.

Data Information Phases may be synchronous transfers as determined by the content of the Synchronous Transfer Register. An offset (OF2 - OF0) of 1 through 5 results in that number of "REQ Burst" transfers, an Offset of 0 specifies asychronous data transfers. The Transfer Period is determined by the TP bits in the Synchronous Transfer Register. All Information Phases other than Data Transfers are Asynchronous.

The completion or termination of a Send Command may be caused by any of the following events:
- $\overline{MR}$ has been asserted.
- A Reset Command has been issued by the local processor/Host.
- The Single Byte Transfer (SBT) bit in the Command Register equals one, or the Transfer Count Register has been set to zero, and a byte has been sent over the SCSI Bus.
- SBT = 0, and the Transfer Counter has decremented to zero, indicating that the desired number of bytes have been transferred.
- During an Asynchronous transfer with the Halt on Attention bit (HA) set in the Control Register, the ATN/$\overline{ATN}$ signal has been asserted.
- An Abort Command has been issued.
- A Disconnect Command has been issued.

When the command terminates as a result of transferring the correct number of bytes, a Successful Completion Status (13, 14 Hex) is placed in the SCSI Status Register.

Except when terminated by a Disconnect or Reset Command, the WD33C92/3-SBIC remains in the Target Mode of operation upon completion of the Send Commands.

TRANSLATE ADDRESS - Comm. Code 18 - Valid Mode D, T - Level II

The Translate Address Command converts a logical address to the physical sector address.

Prior to issuing a Translate Address Command, the disk parameters must be written to the Total Sectors, Total Heads, and Total Cylinder Registers (address 03 - 06 Hex). Also, when the WD33C92/3-SBIC is to perform Bad-Block-Mapping compensation, the number of spare sectors per cylinder must be written in the Head Number Register (address 0C Hex) and the total number of sectors per cylinder in the Cylinder Number Register (address 0D, 0E Hex). When the local processor/Host detects a SCSI command that requires translation, it writes the logical address to the Logical Address Register (address 07 - 0A Hex) and issues a Translate Address Command. Upon detecting a successful completion status, the local processor/Host can read the correct physical address from the Sector Number, Head Number, and Cylinder Number registers (address 0B - 0E Hex).

Should an overflow occur as a result of any division during this command, a Terminated Interrupt is generated and a 45 Hex status is placed in the SCSI Status Register.

TRANSFER - Comm. Codes 20, 21 - Valid Mode I - Level II

The Transfer Info Command is used to send and receive command, data, status, and message information. The Transfer Pad Command forces the WD33C92/3-SBIC to maintain SCSI bus handshaking without requiring access of the Data Register.

The local processor/Host issues a Transfer Command after first examining the SCSI Status Register to determine the type and direction of transfer requested by the Target. With the first REQ after connection as an Initiator, the WD33C92/3-SBIC generates an Interrupt and places a Service Required Status (1000 1MCI) in the SCSI Status Register. The WD33C92/3-SBIC also generates an interrupt each time the Target device requests a new type of Information Transfer.

When the completion of the Transfer Command is dependent upon the Transfer Count Register, this register must be loaded with the number of bytes to be transferred before the Transfer Command is issued.

As with all commands involving data transfers, the Transfer Command makes use of the DMA and WDB bits in the Control Register to determine which device has access to the Data Register. WDB = 1 for DBA mode, DMA = 1 for a DMA Controller, WDB = 0 and DMA = 0 for the Host.

When the local processor/Host has access to the Data Register, it must monitor the Data Buffer Ready status (DBR) in the Auxiliary Status Register to determine when to write to or read from the Data Register. Whether the local processor/Host writes to or reads from the Data Register is dependent upon the state of the I/O signal.

When the transfer is to the Target, I/O is asserted as an output. DBR is set (DBR = 1) when the Transfer Command is issued and each time the content of the Data Register is transferred across the SCSI bus. In this case DBR equal to one indicates to the local processor/Host that the Data Register is in need of a data byte. When the local processor/Host writes a data byte to the Data Register, DBR is reset (DBR = 0), indicating that the Data Register has another data byte available for the SCSI bus.

When the transfer is from the Target, I/O is asserted as an input. DBR is reset (DBR = 0) at the time the Transfer Command is issued and each time the content of the Data Register is read by the local processor/Host. When the Target transfers a data byte across the SCSI Bus into the Data Register, DBR is set (DBR = 1), indicating that the Data Register has another data byte available for the Host to read.

In summary:

Initiator to Target - I/$\overline{O}$ = 0, $\overline{I/O}$ = 1 for the WD33C92/3.
DBR-1 = Data Register is empty and needs to be written to by the Host.
DBR-0 = Data Register is full and needs to be transferred to the Target over the SCSI Bus.

Target to Initiator - I/$\overline{O}$ = 1, $\overline{I/O}$ = 0 for the WD33C92/3.
DBR-1 = Data Register is full and needs to be read by the Host.
DBR-0 = Data Register is empty and needs to be written to by the Target over the SCSI Bus.

Data Information Phases may be synchronous transfers as determined by the contents of the Synchronous Transfer Register. An offset (OF2 - OF0) of 1 through 5 results in that number of "REQ Burst" transfers, and an Offset of 0 specifies asynchronous data transfers. The Transfer Period is determined by the TP bits in the Synchronous Transfer Register. All Information Phases, other than Data Transfers, are Asynchronous.

The completion or termination of a Transfer Info Command may be caused by any of the following events:

- $\overline{MR}$ has been asserted.
- A Reset Command issued by the Host.
- The Single Byte Transfer (SBT) bit in the Command Register equals one, or the Transfer Count Register has been set to zero, and a byte has been read from the Data Register.
- SBT = 0, and the Transfer Counter has decremented to zero, indicating that the desired number of bytes have been transferred.
- During an Asynchronous transfer with the Halt on Parity Error bit (HPE) set in the Control Register, a Parity Error occurred on the received data byte.
- An Abort Command has been issued.
- A Disconnect Command has been issued.
- BSYI/$\overline{BSY}$ has been released by the Target, causing transition to the disconnected state.
- A change has occured in the I/O, C/D, or MSG signals during a Transfer Command.

During Non-Message-In Information Phases, when the number of bytes specified in the Transfer Count Register have been satisfied according to the SBT bit in the Control Register, the WD33C92/3-SBIC generates a Successful Completion Interrupt only after receiving another REQ from the Target. During Message-In Phases, the WD33C92/3-SBIC generates a Pause/Aborted interrupt upon the trailing edge of the last message-byte REQ. This results in the ACK signal remaining asserted and requires the Host to issue a Negate ACK or an Assert ATN followed by a Negate ACK command to accept or reject the message respectively.

When a Parity Error is detected on a received byte during asynchronous transfers and HPE = 1, the WD33C92/3-SBIC terminates the command, leaves ACK asserted to halt the Target, generates a Terminated Interrupt, and places a 43 or 44 Hex in the SCSI Status Register.

When a Parity Error is detected on a received byte during synchronous transfers or HPE = 0, the WD33C92/3-SBIC sets the Parity Error Status (PE) in the Auxiliary Status Register, but does not terminate the command.

Negation of the BSYI/$\overline{BSY}$ (Target suddenly disconnects) or a transition of I/O, C/D, and/or MSG during a Transfer Command terminates the command and places Terminated Interrupt (41 or 48 - 4F Hex) in the SCSI Status Register.

The Transfer Pad Command operates and terminates the same as the Transfer Info Command with the following exceptions:

- The first byte written to the Data Register is repeatedly transmitted across the SCSI Bus during an Information Out Phase.
- There are no parity checks.
- There are no Data Buffer Ready (DBR) indications when receiving data.

Therefore, Host intervention is not required to maintain the handshake sequence.

WD33C92/3-SBIC ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Voltage on any pin with respect to V_{SS} (Ground) .....-0.2V to +7.0V

Operating Temperature... 0°C (32°F) to 70°C (158°F)
Storage Temperature... −55°C (−67°F) to 125°C (257°F)
Power Dissipation: WD33C92.....100mW
WD33C93.....500mW

NOTE T-52-33-27

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

DC OPERATING CHARACTERISTICS

T_A = 0°C(32°F) to 70°C(158°F)
V_{CC} = +5V ± .25V
V_{SS} = 0V

TABLE 14. DC OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	CONDITION
I_{IL}	Input Leakage		10	uA	VIN = .4 to V_{CC}
I_{OL2}	SCSI Output Leakage * (inactive)		50	uA	VOUT = .5 to V_{CC}
I_{OL1}	Output Leakage (tri-state)		10	uA	VOUT = .4 to V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	IO = -400 uA
V_{OL1}	SCSI Output Low Voltage *		0.5	V	IO = 48.0 mA
V_{OL2}	Output Low Voltage * (all others)		0.4	V	IO = 4.0 mA
V_{OL1}	Output Low Voltage ** (TGS and IGS)		0.4	V	IO = 7.0 mA
V_{OL2}	Output Low Voltage ** (all others)		0.4	V	IO = 2.0 mA
I_{CC}	Supply Current		20	mA	T_A = +25°C 77°F

* Represents WD33C93 only

** Represents WD33C92 only

TIMING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature, 0°C(32°F) to 70°C(158°F), and voltage range (4.75 to 5.25 volts), and are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. All outputs are assumed to have a load capacitance of 50 pf.

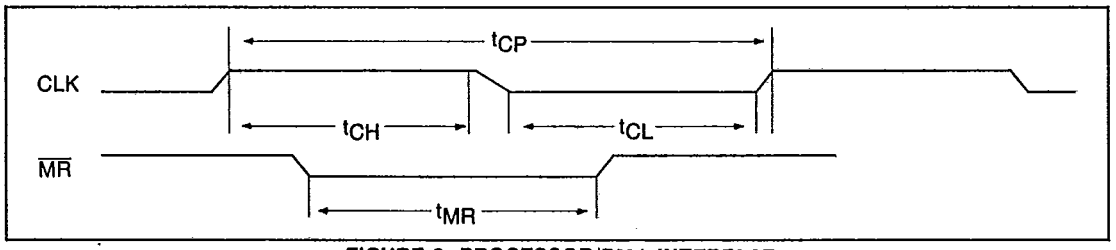


FIGURE 2. PROCESSOR/DMA INTERFACE

TABLE 15. PROCESSOR/DMA INTERFACE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{CP}	Clock Period	100	125	nsec
t_{CH}	Clock High	45		nsec
t_{CL}	Clock Low	45		nsec
t_{MR}	$\overline{MR}$ Pulse Width	1		usec

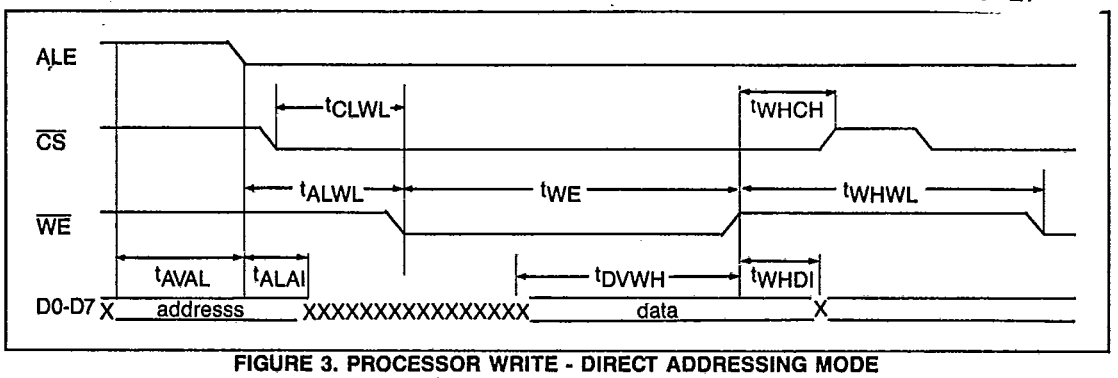


FIGURE 3. PROCESSOR WRITE - DIRECT ADDRESSING MODE

TABLE 16. PROCESSOR WRITE - DIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{AVAL}	ADDR Valid To ALE Low	40		nsec
t_{ALAI}	ALE Low To ADDR Invalid	10		nsec
t_{ALWL}	ALE Low To $\overline{WE}$ Low	100		nsec
t_{CLWL}	$\overline{CS}$ Low To $\overline{WE}$ Low	0		nsec
t_{WE}	$\overline{WE}$ Pulse Width	120		nsec
t_{DVWH}	Data Valid To $\overline{WE}$ High	70		nsec
t_{WHCH}	$\overline{WE}$ High To $\overline{CS}$ High	0		nsec
t_{WHDI}	$\overline{WE}$ High To Data Invalid	0		nsec
t_{WHWL}	$\overline{WE}$ High To $\overline{WE}$ Or $\overline{RE}$ Low	100		nsec

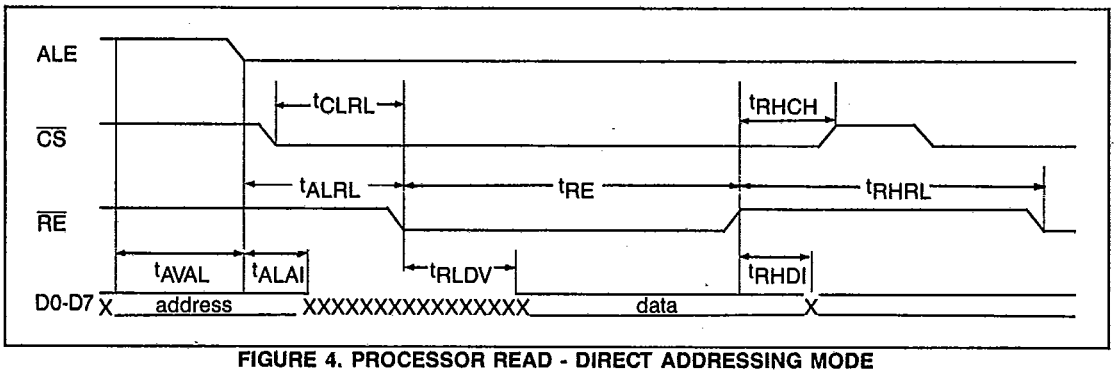


FIGURE 4. PROCESSOR READ - DIRECT ADDRESSING MODE

TABLE 17. PROCESSOR READ — DIRECT ADDRESSING MODE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{AVAL}	ADDR Valid To ALE Low	40		nsec
t_{ALAI}	ALE Low To ADDR Invalid	10		nsec
t_{ALAR}	ALE Low To $\overline{RE}$ Low	30		nsec
t_{CLRL}	$\overline{CS}$ Low To $\overline{RE}$ Low	0		nsec
t_{RE}	$\overline{RE}$ Pulse Width	180	10000	nsec
t_{RLDV}	$\overline{RE}$ Low To Data Valid		175	nsec
t_{RHCH}	$\overline{RE}$ High To $\overline{CS}$ High	0		nsec
t_{RHDI}	$\overline{RE}$ High To Data Invalid	10	100	nsec
t_{RHRL}	$\overline{RE}$ High To $\overline{RE}$ Or $\overline{WE}$ Low	100		nsec

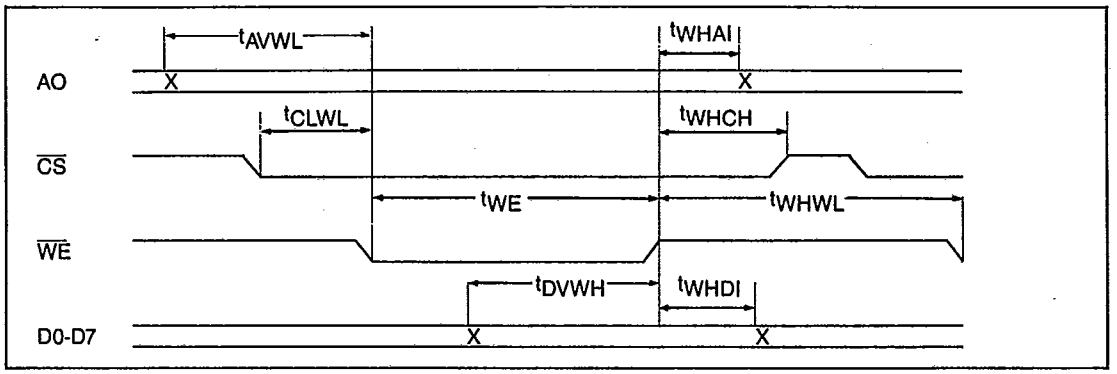


FIGURE 5. PROCESSOR WRITE - INDIRECT ADDRESSING

TABLE 18. PROCESSOR WRITE - INDIRECT ADDRESSING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{AVWL}	ADDR Valid To $\overline{WE}$ Low	0		nsec
t_{CLWL}	$\overline{CS}$ Low To $\overline{WE}$ Low	0		nsec
t_{WE}	$\overline{WE}$ Pulse Width	120		nsec
t_{DVWH}	Data Valid to $\overline{WE}$ High	70		nsec
t_{WHAI}	$\overline{WE}$ High to ADDR Invalid	0		nsec
t_{WHCH}	$\overline{WE}$ High To $\overline{CS}$ High	0		nsec
t_{WHDI}	$\overline{WE}$ High To Data Invalid	0		nsec
t_{WHWL}	$\overline{WE}$ High To $\overline{WE}$ Or $\overline{RE}$ Low	100		nsec

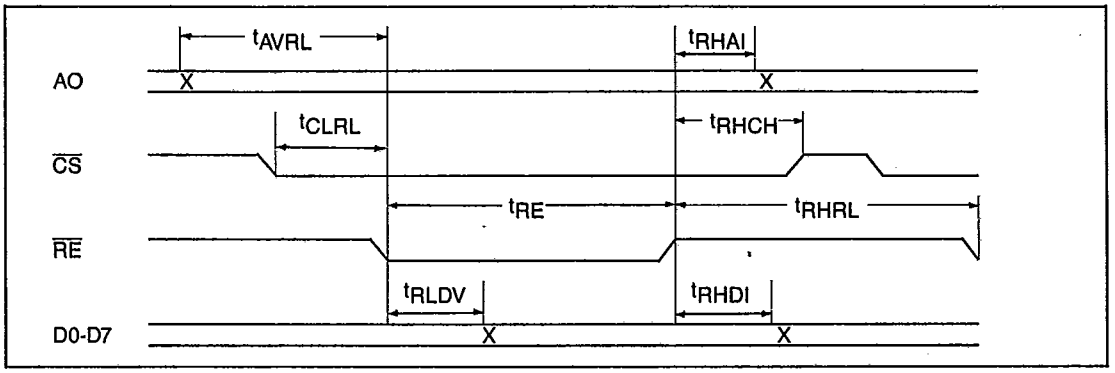


FIGURE 6. PROCESSOR READ - INDIRECT ADDRESSING

TABLE 19. PROCESSOR READ - INDIRECT ADDRESSING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{AVRL}	ADDR Valid To $\overline{RE}$ Low	0		nsec
t_{CLRL}	$\overline{CS}$ Low To $\overline{RE}$ Low	0		nsec
t_{RE}	$\overline{RE}$ Pulse Width	180	10000	nsec
t_{RLDV}	$\overline{RE}$ Low To Data Valid		175	nsec
t_{RHAI}	$\overline{RE}$ High To ADDR Invalid	0		nsec
t_{RHCH}	$\overline{RE}$ High To $\overline{CS}$ High	0		nsec
t_{RHDI}	$\overline{RE}$ High To Data Invalid	10	100	nsec
t_{RHRL}	$\overline{RE}$ High To $\overline{RE}$ Or $\overline{WE}$ Low	250		nsec

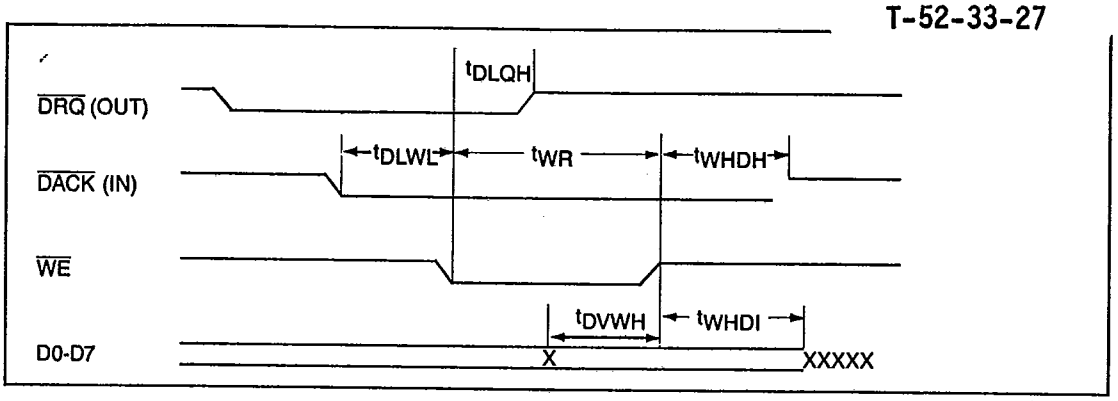


FIGURE 7. DMA WRITE

TABLE 20. DMA WRITE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{DLQH}	$\overline{DACK}$, $\overline{WE}$ Low To $\overline{DRQ}$ High		125	nsec
t_{DLWL}	$\overline{DACK}$ Low To $\overline{WE}$ Low	0		nsec
t_{WR}	$\overline{WE}$ Pulse Width	50		nsec
t_{DVWH}	Data Valid To $\overline{WE}$ High	25		nsec
t_{WHDH}	$\overline{WE}$ High To $\overline{DACK}$ High	0		nsec
t_{WHDI}	$\overline{WE}$ High To Data Invalid	0		nsec

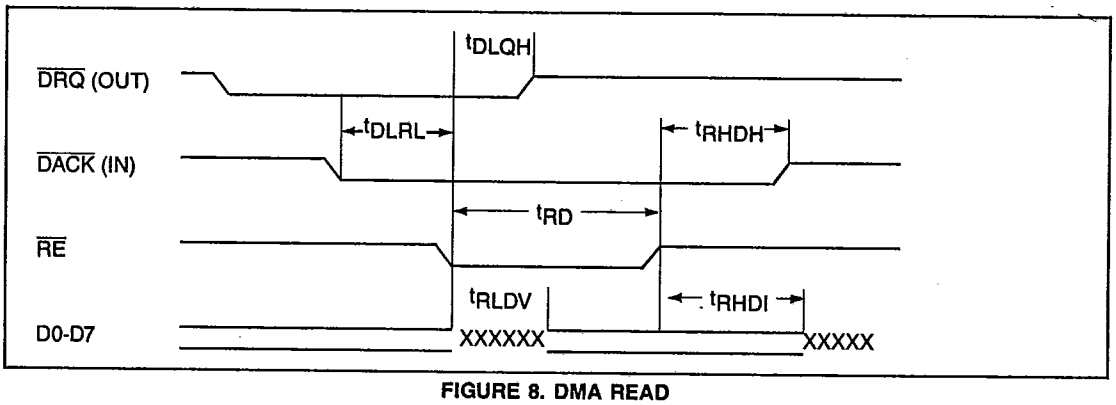


FIGURE 8. DMA READ

TABLE 21. DMA READ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{DLQH}	$\overline{DACK}$, $\overline{RE}$ Low To $\overline{DRQ}$ High		125	nsec
t_{DLRL}	$\overline{DACK}$ Low to $\overline{RE}$ Low	0		nsec
t_{RD}	$\overline{RE}$ Pulse Width	80	10000	nsec
t_{RLDV}	$\overline{RE}$ Low To Data Valid		80	nsec
t_{RHDH}	$\overline{RE}$ High To $\overline{DACK}$ High	0		nsec
t_{RHDI}	$\overline{RE}$ High To Data Invalid	10	100	nsec

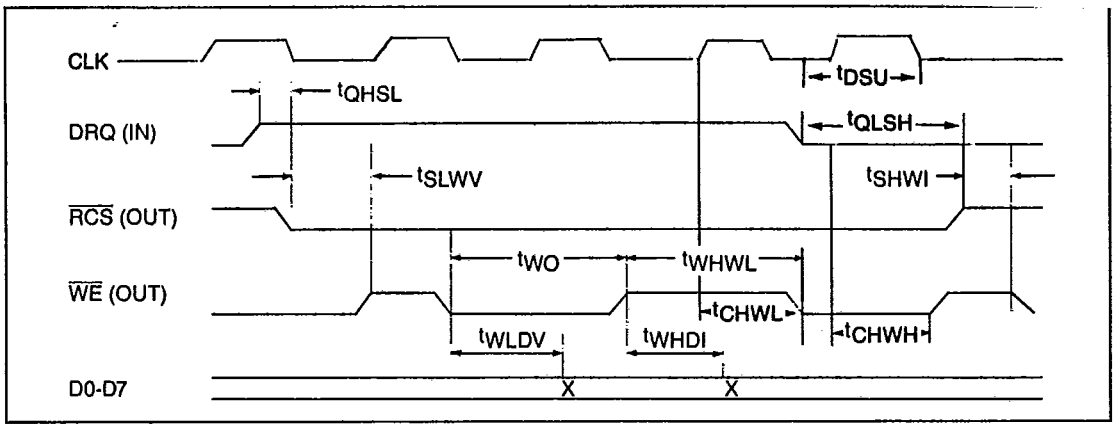


FIGURE 9. WD-BUS BUFFER WRITE

TABLE 22. WD-BUS BUFFER WRITE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{QHSL}	DRQ High To $\overline{RCS}$ Low	0		nsec
t_{SLWV}	$\overline{RCS}$ Low To $\overline{WE}$ Valid	0	50	nsec
t_{WO}	$\overline{WE}$ Pulse Width	1		t_{CP}
		−20		nsec
t_{WLDV}	$\overline{WE}$ Low To Data Valid		50	nsec
t_{WHDI}	$\overline{WE}$ High To Data Invalid	30		nsec
t_{WHWL}	$\overline{WE}$ High To $\overline{WE}$ Low	1		t_{CP}
		−20		nsec
t_{QLSH}	DRQ Low to $\overline{RCS}$ High	8	10	t_{CP}
t_{SHWI}	$\overline{RCS}$ High to $\overline{WE}$ Invalid	0	100	nsec
t_{CHWH}	CLK High To $\overline{WE}$ High	40	125	nsec
t_{CHWL}	CLK High to $\overline{WE}$ Low	40	125	nsec
t_{DSU}	DRQ Setup to CLK High	1		t_{CP}
		+20		nsec

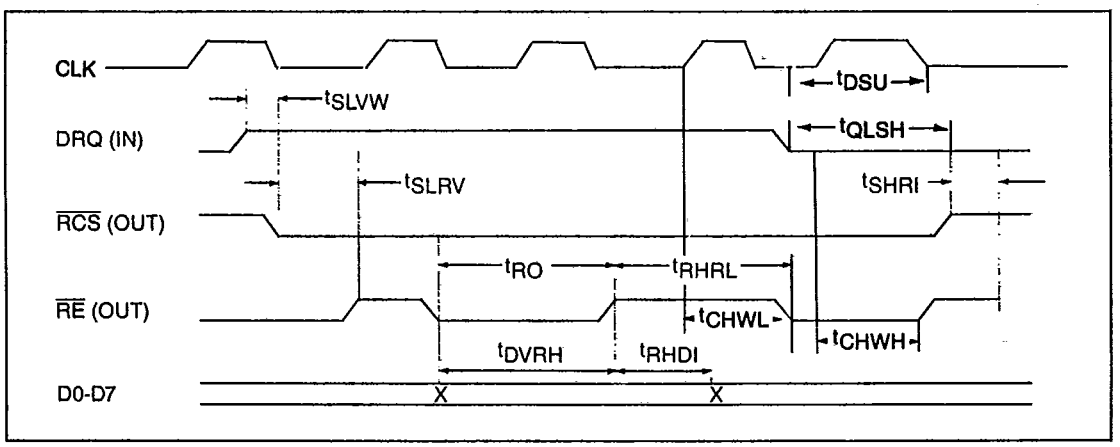


FIGURE 10. WD-BUS BUFFER READ

T-52-33-27

TABLE 23. WD-BUS BUFFER READ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLWV}	DRQ High To $\overline{RCS}$ Low	0		nsec
t_{SLRV}	$\overline{RCS}$ Low To $\overline{RE}$ Valid	0	50	nsec
t_{RO}	$\overline{RE}$ Pulse Width	1		t_{CP}
		−20		nsec
t_{DVRH}	Data Valid to $\overline{RE}$ High	10		nsec
t_{RHDI}	$\overline{RE}$ High To Data Invalid	10		nsec
t_{RHRL}	$\overline{RE}$ High To $\overline{RE}$ Low	1		t_{CP}
		−20		nsec
t_{QLSH}	DRQ Low to $\overline{RCS}$ High	8	10	t_{CP}
t_{SHRI}	$\overline{RCS}$ High to $\overline{RE}$ Invalid	0	100	nsec
t_{CHRH}	CLK High to $\overline{RE}$ High	40	125	nsec
t_{CHRL}	CLK High to $\overline{RE}$ Low	40	125	nsec
t_{DSU}	DRQ Setup to CLK High	1		t_{CP}
		+20		nsec

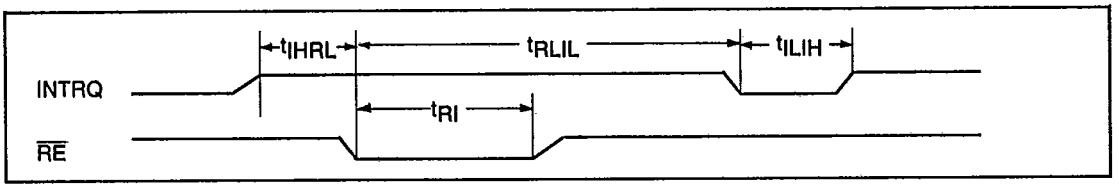


FIGURE 11. INTRQ

TABLE 24. INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{IHRL}	INTRQ High To $\overline{RE}$ Low	0		nsec
t_{RI}	$\overline{RE}$ Pulse Width	200		nsec
t_{RLIL}	$\overline{RE}$ Low To INTRQ Low	0	100	nsec
t_{ILIH}	INTRO Low To INTRQ High	100		nsec

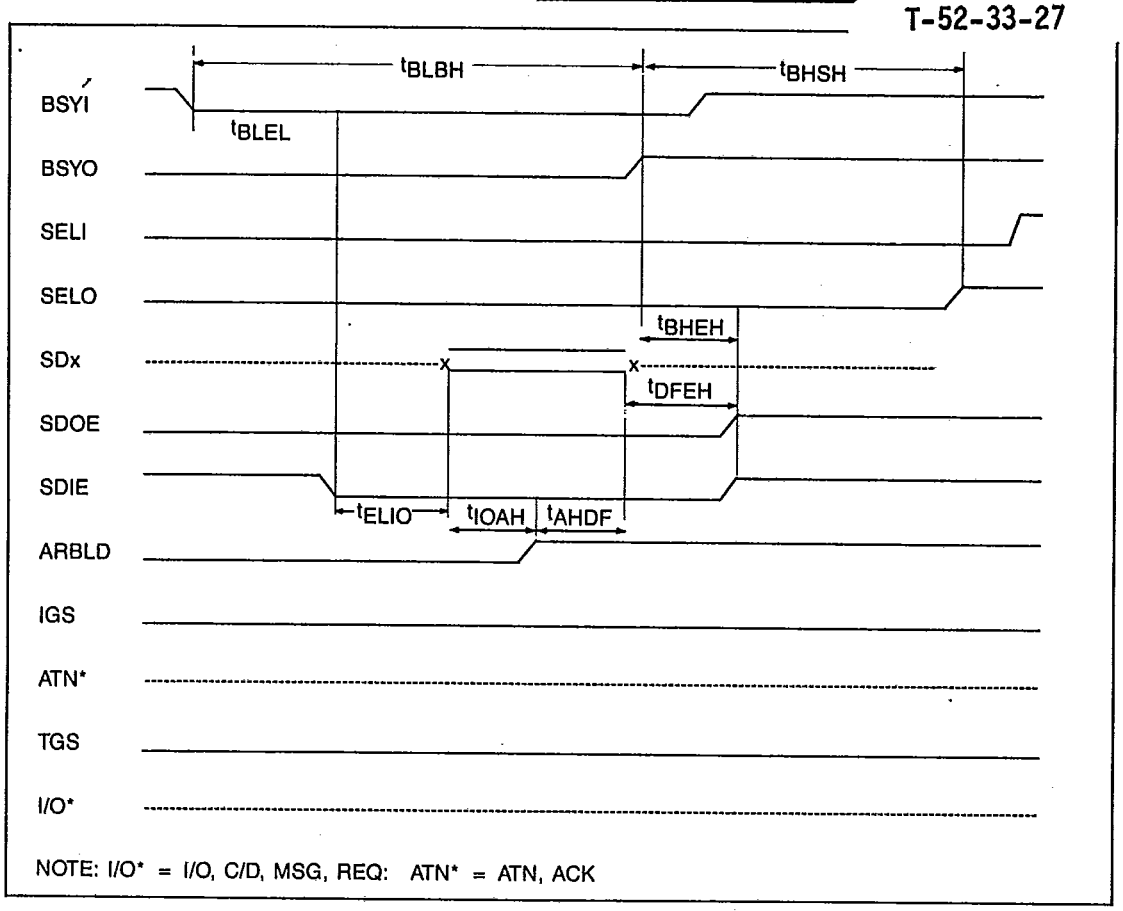


FIGURE 12. ARBITRATION - WD33C92

TABLE 25. ARBITRATION - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{BLEL}	BSYI, SELI Low To SDIE Low	4		t_{CP}
t_{ELIO}	SDIE Low To Bus ID Out	−30	50	t_{CP}
t_{IOAH}	Bus ID Out To ARBLD High	1		t_{CP}
t_{AHDF}	ARBLD High To Data Float	1		t_{CP}
t_{DFEH}	Data Float To SDIE, SDOE High	1		t_{CP}
t_{BLBH}	BSYI, SELI Low To BSYO High	12	17	t_{CP}
t_{BHEH}	BSYO High To SDIE High	−0	200	nsec
t_{BHSH}	BSYO High To SELO High	2.2		usec

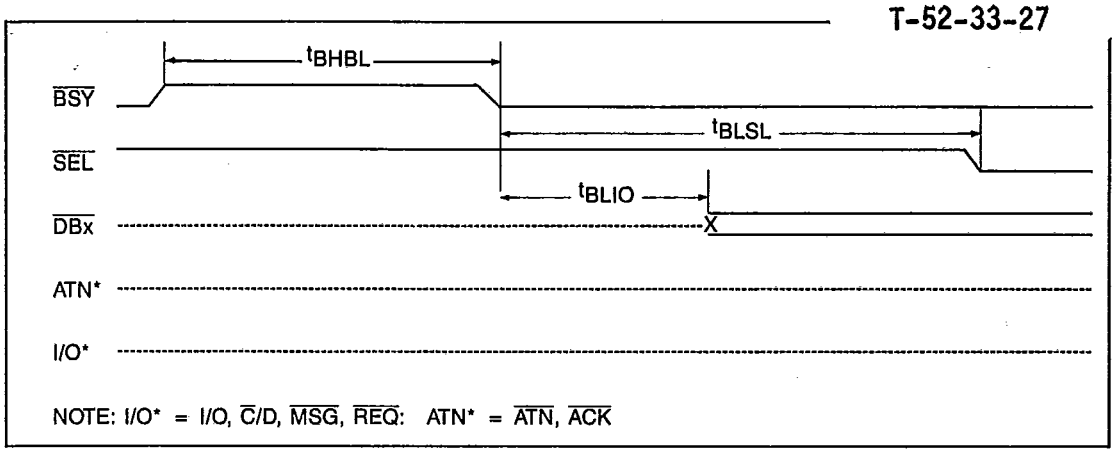


FIGURE 13. ARBITRATION - WD33C93

TABLE 26. ARBITRATION - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{BHBL}	BSY, SEL In High to BSY Out Low	12	15	t_{CP}
t_{BLIO}	BSY Out Low To Bus ID Out	−50	50	nsec
t_{BLSL}	BSY Out Low To SEL Out Low	2.2		usec

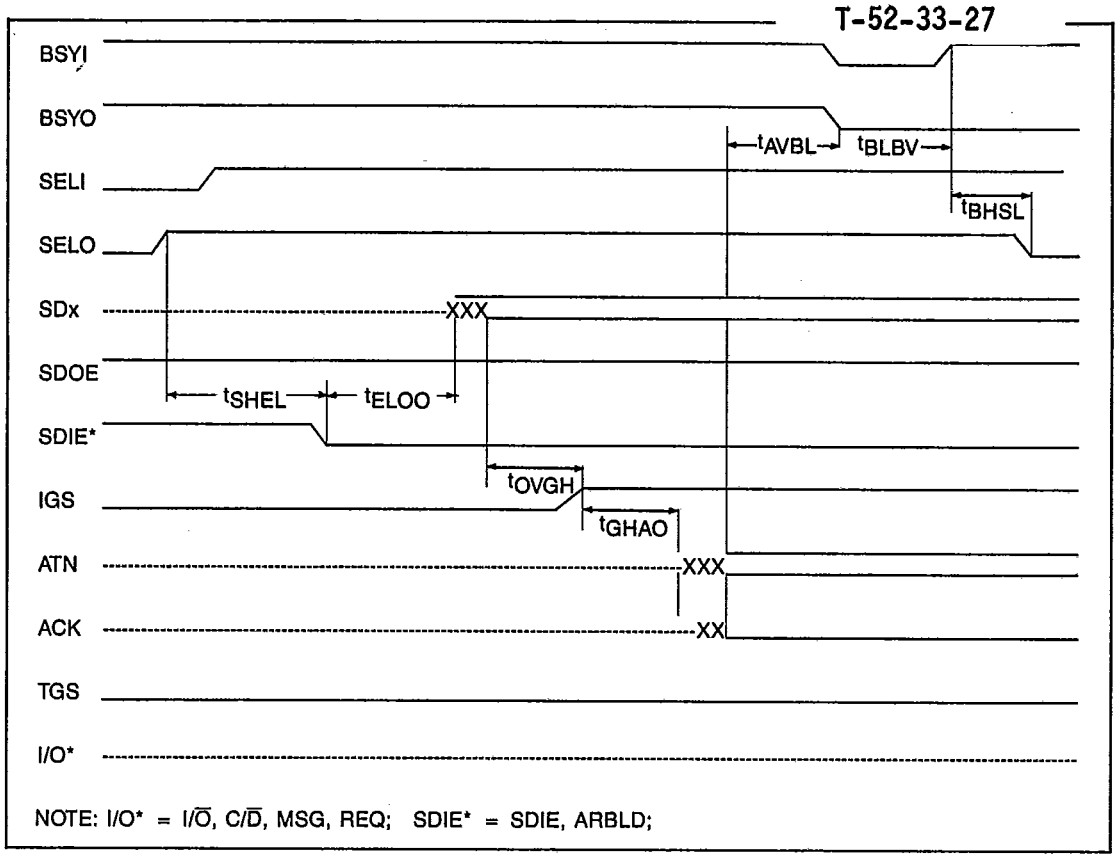


FIGURE 14. SELECTION - INITIATOR - WD33C92

TABLE 27. SELECTION - INITIATOR - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHEL}	SELO High To SDIE Low	1.2		usec
t_{ELOO}	SDIE Low To "ORed" ID Out	100		nsec
t_{OVGH}	"ORed" ID Out Valid To IGS High	100		nsec
t_{GHAO}	IGS High To ATN, ACK Out	100		nsec
t_{AVBL}	ATN, ACK Valid Out To BSYO Low	100		nsec
t_{BLBV}	BSYO Low To BSYI High Valid	400		nsec
t_{BHSL}	BSYI High To SELO Low	100		nsec

T-52-33-27

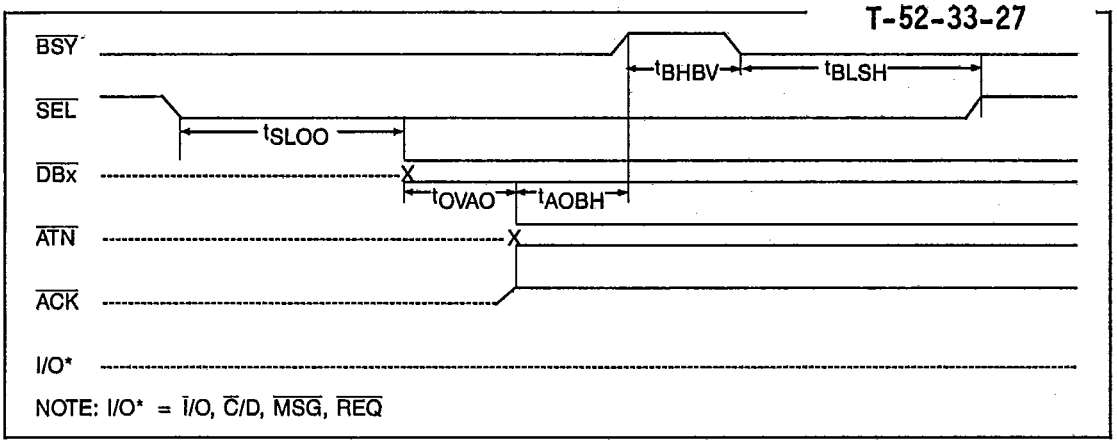
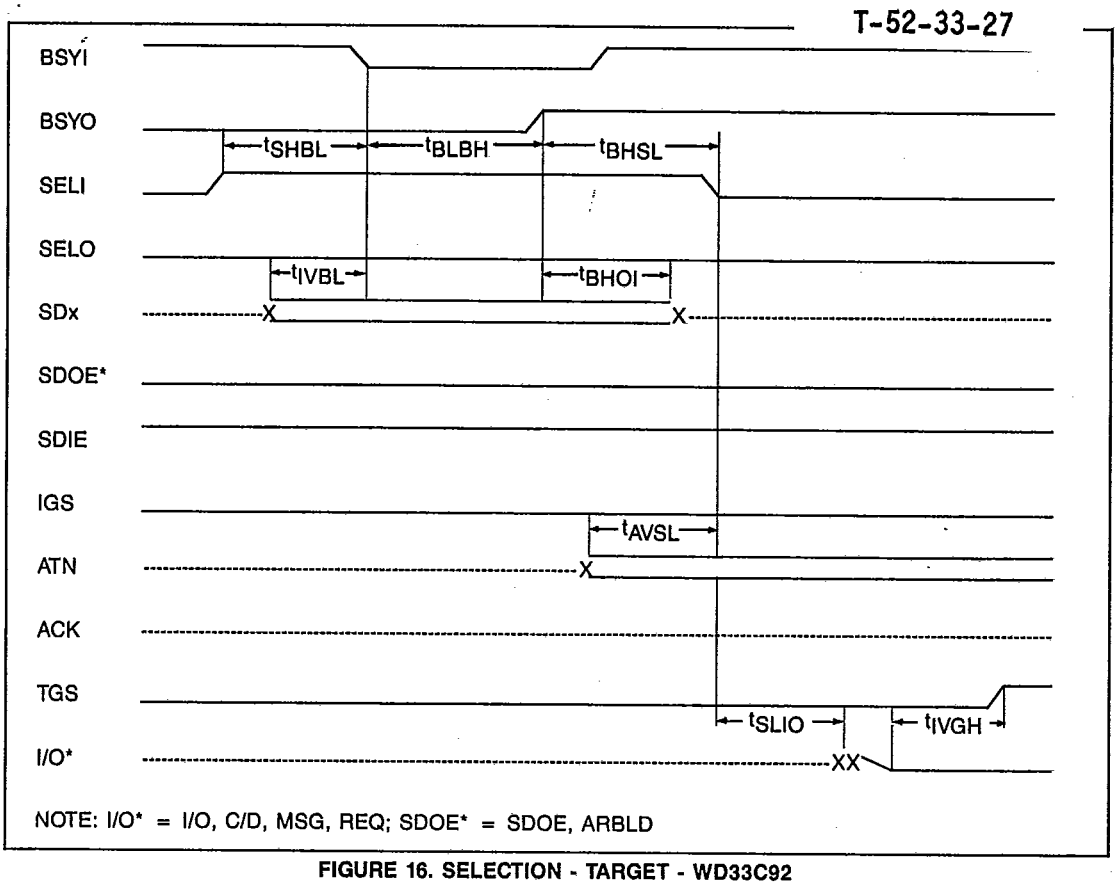


FIGURE 15. SELECTION - INITIATOR - WD33C93

TABLE 28. SELECTION - INITIATOR - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLOO}	SEL Out Low To "ORed" ID Out	1.2		usec
t_{OVOA}	"ORed" ID Out Valid To ACK, ATN Out	100		nsec
t_{AOBH}	ACK, ATN Out Valid To BSY Out High	100		nsec
t_{BHBV}	BSY Out High To BSY In Low Valid	400		nsec
t_{BLSH}	BSY In Low To SEL Out High	100		nsec



NOTE: I/O* = I/O, C/D, MSG, REQ; SDOE* = SDOE, ARBLD

FIGURE 16. SELECTION - TARGET - WD33C92

TABLE 29. SELECTION - TARGET - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHBL}	SELI High To BSYI Low	0		nsec
t_{IVBL}	ORed ID Valid In To BSYI Low	0		nsec
t_{BLBH}	SELI High, ID Valid, BSYI Low To BSYO High	0.4	200	usec
t_{BHOI}	BSYO High To ORed ID Invalid In	0		nsec
t_{BHSL}	BSYO High To SELI Low	0		nsec
t_{AVSL}	ATN Valid In To SELI Low	0		nsec
t_{SLIO}	SELI Low TO I/$\overline{O}$ Out	100		nsec
t_{IVGH}	I/$\overline{O}$ Out Valid To TGS High	100		nsec

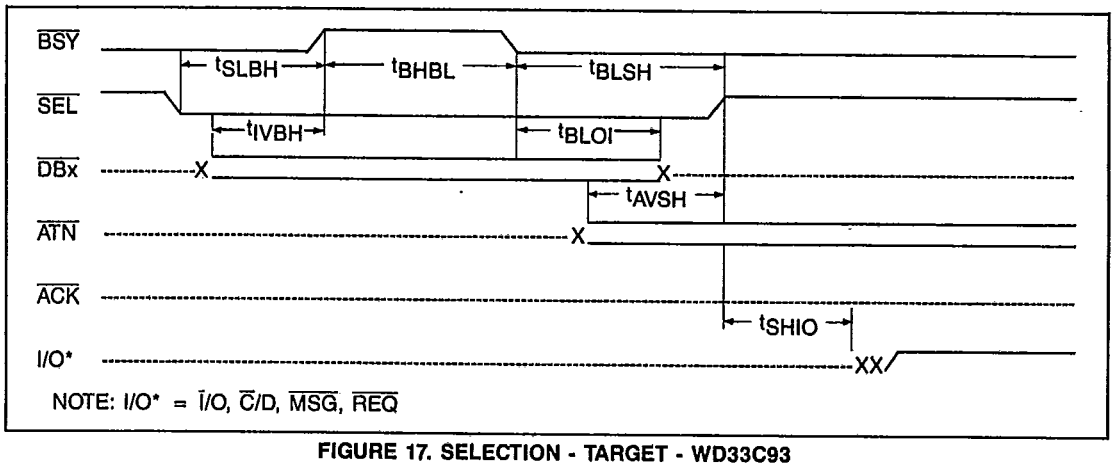
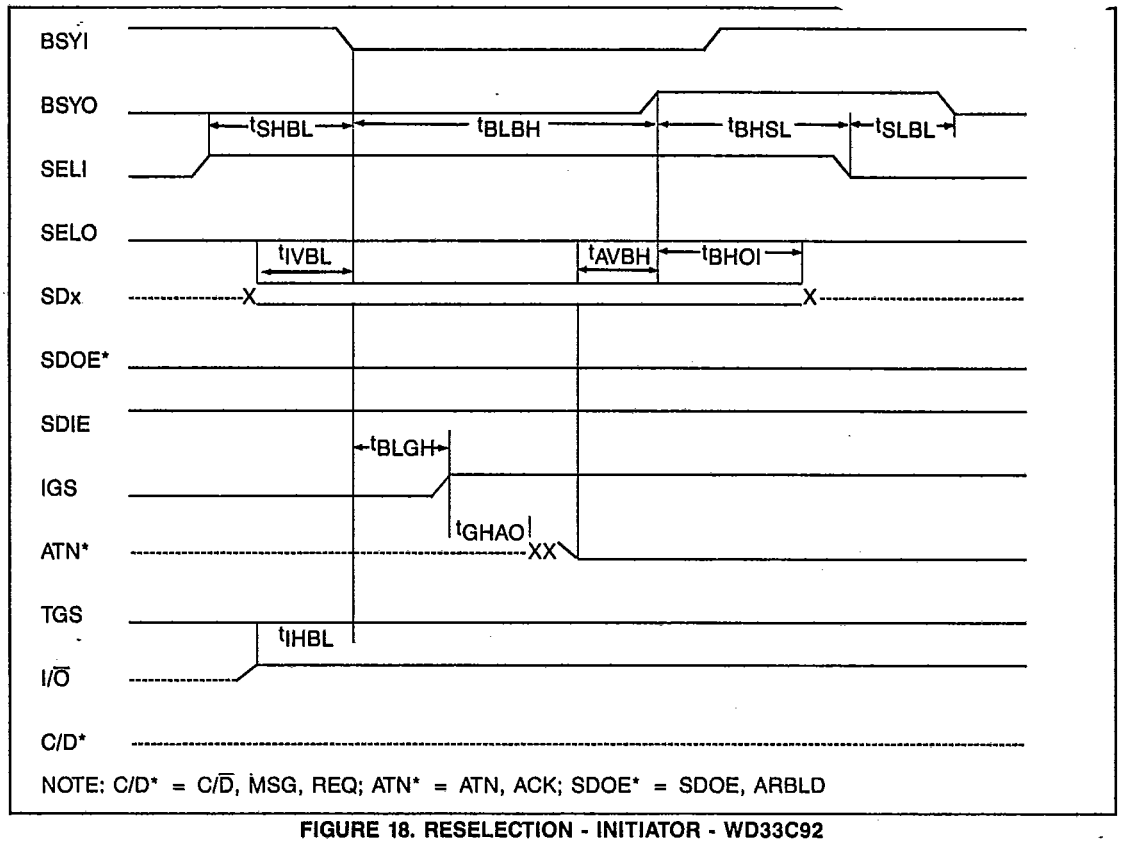


FIGURE 17. SELECTION - TARGET - WD33C93

TABLE 30. SELECTION - TARGET - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLHB}	SEL In Low To BSY In High	0		nsec
t_{IVBH}	ORed ID Valid In To BSY In High	0		nsec
t_{BHBL}	SEL Low, ID Valid, BSY High To BSY Low	0.4	200	usec
t_{BLOI}	BSY Out Low To ORed ID Invalid In	0		nsec
t_{BLSH}	BSY Out Low To SEL In High	0		nsec
t_{AVSH}	ATN Valid In To SEL In High	0		nsec
t_{SHIO}	SEL In High To I/O Out	100		nsec

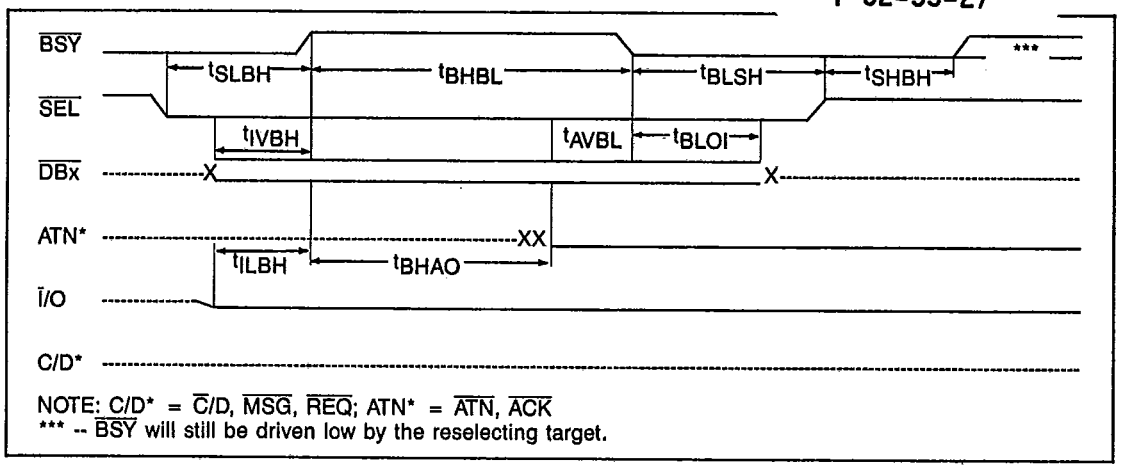


NOTE: C/D* = C/$\overline{D}$, MSG, REQ; ATN* = ATN, ACK; SDOE* = SDOE, ARBLD

FIGURE 18. RESELECTION - INITIATOR - WD33C92

TABLE 31. RESELECTION - INITIATOR - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHBL}	SELI High To BSYI Low	0		nsec
t_{IVBL}	ORed ID Valid In To BSYI Low	0		nsec
t_{IHBL}	I/O In High To BSYI Low	0		nsec
t_{BLGH}	SELI High, ID Valid, BSYI Low To IGS High	0		nsec
t_{GHAO}	IGS High To ATN Out	100		nsec
t_{AVBH}	ATN Valid Out TO BSYO High	100		nsec
t_{BLBH}	BSYI Low To BSYO High	0.4	200	usec
t_{BHOI}	BSYO High To ORed Invalid In	0		nsec
t_{SLBL}	SELI Low To BSYO Low	0		nsec
t_{BHSL}	BSYO High To SELI Low	0		nsec

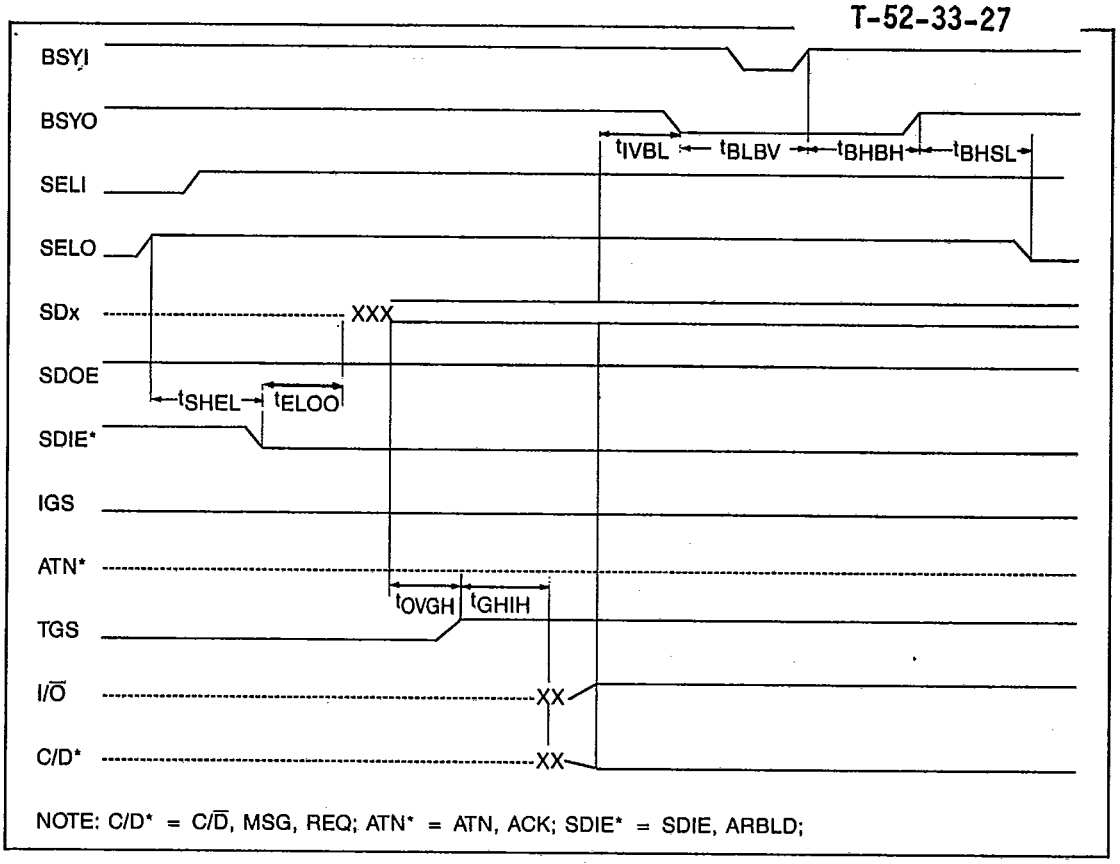


NOTE: C/D* = C/D, MSG, REQ; ATN* = ATN, ACK
*** -- BSY will still be driven low by the reselecting target.

FIGURE 19. RESELECTION - INITIATOR - WD33C93

TABLE 32. RESELECTION - INTIATOR - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLBH}	SEL In Low To BSY In High	0		nsec
t_{IVBH}	ORed ID Valid In To BSY In High	0		nsec
t_{ILBH}	I/O In Low To BSY In High	0		nsec
t_{BHAO}	SEL Low, ID Valid, BSY High To ATN Out	0		nsec
t_{AVBI}	ATN Valid Out To BSY Out Low	100		nsec
t_{BHBL}	BSY In High To BSY Out Low	0.4	200	usec
t_{BLOI}	BSY Out Low To ORed Invalid In	0		nsec
t_{BLSH}	BSY Out Low To SEL In High	0		nsec
t_{SHBH}	SEL In High To BSY Out High	0		nsec



NOTE: C/D* = C/D, MSG, REQ; ATN* = ATN, ACK; SDIE* = SDIE, ARBLD;

FIGURE 20. RESELECTION - TARGET - WD33C92

TABLE 33. RESELECTION - TARGET - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHEL}	SELI High To SDIE Low	1.2		usec
t_{ELOO}	SDIE Low To ORed ID Out	100		nsec
t_{OVGH}	ORed ID Out Valid To TGS High	0		nsec
t_{GHIH}	TGS High I/O Out, C/D Out	100		nsec
t_{IVBL}	I/O, C/D Out Valid To BSYO Low	100		nsec
t_{BLBV}	BSYO Low To BSYI High Valid	400		nsec
t_{BHBH}	BSYI High To BSYO High	0		usec
t_{BHSL}	BSYO High To SELO Low	100		nsec

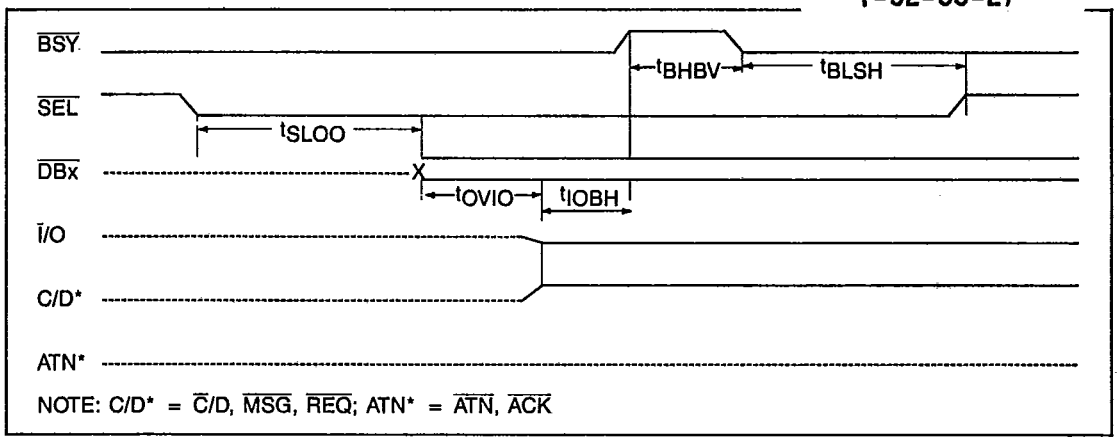


FIGURE 21. RESELECTION - TARGET - WD33C93

TABLE 34. RESELECTION - TARGET - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLOO}	SEL Out Low To ORed ID Out	1.2		usec
t_{OVIO}	ORed ID Out Valid To I/O Out Valid	100		nsec
t_{IOBH}	I/O Out Valid To BSY Out High	100		nsec
tBHBV	BSY Out To BSY In Low Valid	400		nsec
t_{BLSH}	BSY In Low To SEL Out High	100		nsec

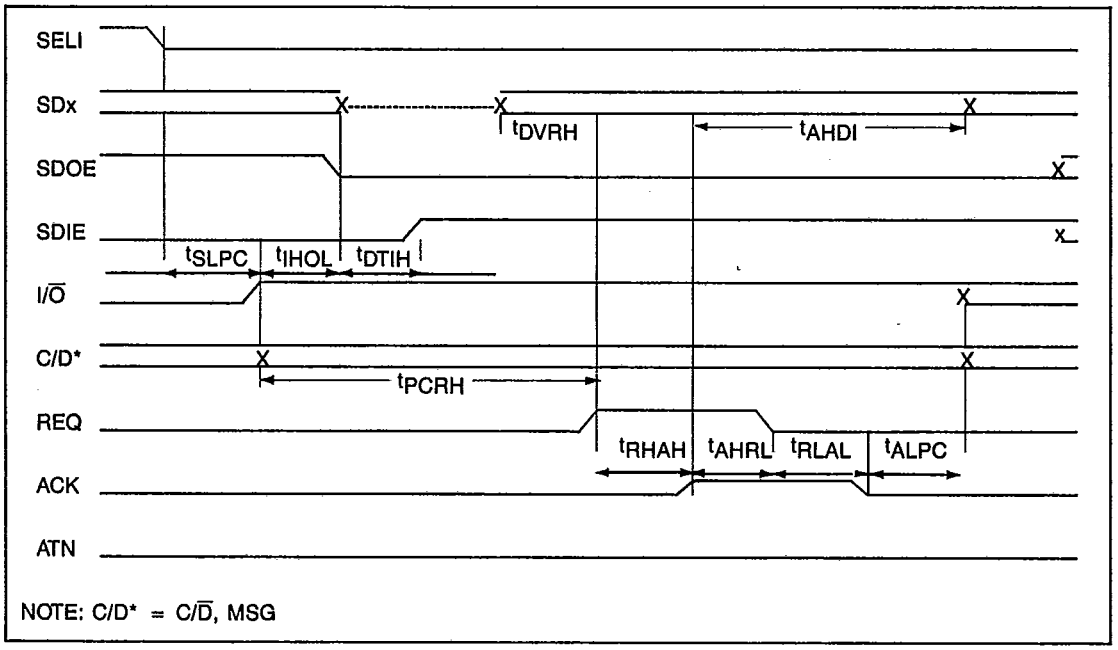
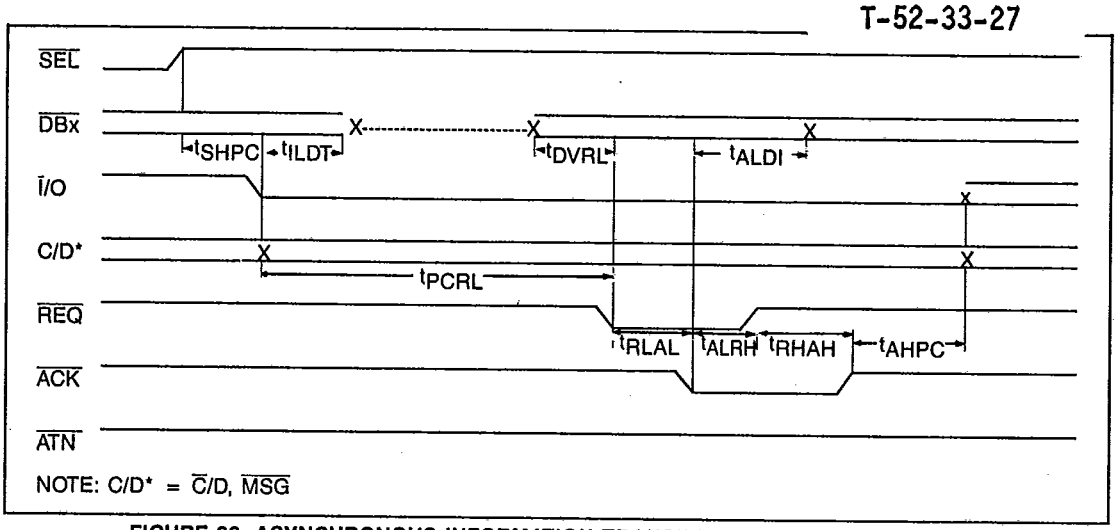


FIGURE 22. ASYNCHRONOUS INFORMATION TRANSFER IN - INITIATOR - WD3392

TABLE 35. ASYNCHRONOUS INFORMATION TRANSFER IN - INITIATOR - WD3392

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLPC}	SELI Low To Phase Change In	0		nsec
t_{IHOL}	I/O In High To SDOE Low, Data Bus Tri-State	0	125	nsec
t_{DTIH}	Data Bus Tri-State To SDIE High	30		nsec
t_{PCRH}	Phase Change In To REQ In High	400		nsec
t_{DVRH}	Data Valid In To REQ In High	5		nsec
t_{RHAH}	REQ In High To ACK Out High	0		nsec
t_{AHRL}	ACK Out High To REQ In Low	0		nsec
t_{AHDI}	ACK Out High To Data Invalid In	0		nsec
t_{ALPC}	ACK Out Low To Phase Change In	0		nsec
t_{RLAL}	REQ In Low To ACK Out Low	0		nsec

T-52-33-27



NOTE: C/D* = C/D, MSG

FIGURE 23. ASYNCHRONOUS INFORMATION TRANSFER IN - INITIATOR - WD3393

TABLE 36. ASYNCHRONOUS INFORMATION TRANSFER IN - INITIATOR - WD3393

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHPC}	SEL In High To Phase Change In	0		nsec
t_{ILTD}	I/O In Low To Data Bus Tri-State	0	125	nsec
t_{PCRL}	Phase Change In To REQ In Low	400		nsec
t_{DVRL}	Data Valid In To REQ In Low	5		nsec
t_{RLAL}	REQ In Low To ACK Out Low	0	175*	nsec
t_{ALDI}	ACK Out Low To Data Invalid In	0		nsec
t_{ALRH}	ACK Out Low To REQ In High	0		nsec
t_{RHAH}	REQ In High To ACK Out High	0	175*	nsec
t_{AHPC}	ACK Out High To Phase Change In	0		nsec

* All other conditions for ACK signal transition must exist.

T-52-33-27

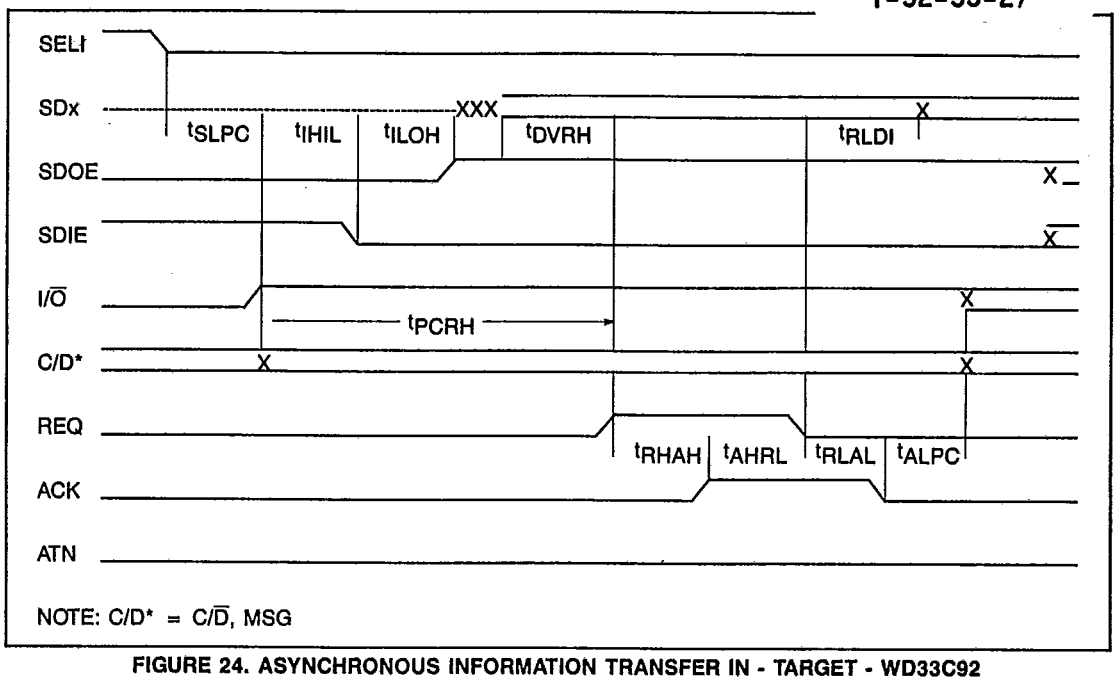


FIGURE 24. ASYNCHRONOUS INFORMATION TRANSFER IN - TARGET - WD33C92

TABLE 37. ASYNCHRONOUS INFORMATION TRANSFER IN - TARGET - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLPC}	SELI Low To Phase Change Out	100		nsec
t_{IHIL}	I/O Out High To SDIE Low	0		nsec
t_{ILOH}	SDIE Low To SDOE High, Data Out	0		nsec
t_{PCRH}	Phase Change Out To REQ Out High	500		nsec
t_{DVRH}	Data Out Valid To REQ Out High	55		nsec
t_{RHAH}	REQ Out High To ACK In High	0		nsec
t_{AHRL}	ACK In High To REQ Out Low	0		nsec
t_{RLDI}	REQ Out Low To Data Out Invalid	0		nsec
t_{ALPC}	ACK In Low To Phase Change Out	100		nsec
t_{RLAL}	REQ Out Low To ACK In Low	0		nsec

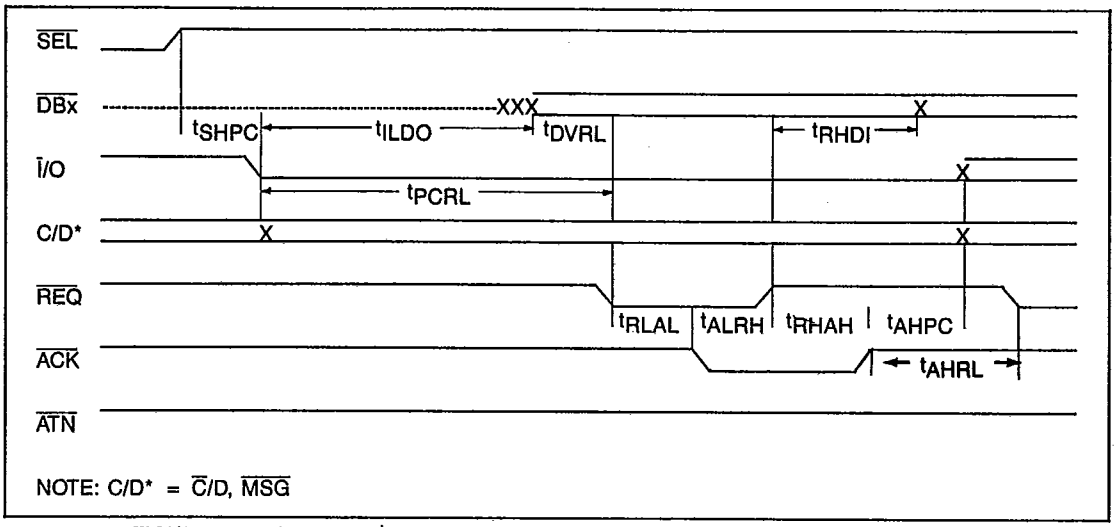


FIGURE 25. ASYNCHRONOUS INFORMATION TRANSFER IN - TARGET - WD33C93

TABLE 38. ASYNCHRONOUS INFORMATION TRANSFER IN - TARGET - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
tSHPC	SEL In High To Phase Change Out	100		nsec
tILDO	I/O Out Low To Data Out	0		nsec
tPCRL	Phase Change Out To REQ Out Low	500		nsec
tDVRL	Data Out Valid To REQ Out Low	55		nsec
tRLAL	REQ Out Low To ACK In Low	0		nsec
tALRH	ACK In Low To REQ Out High	0	175*	nsec
tRHDI	REQ Out High To Data Out Invalid	0		nsec
tAHPC	ACK In High To Phase Change Out	100		nsec
tRHAH	REQ Out High To ACK In High	0		nsec
tAHRL	ACK In High To REQ Out Low	0	175*	nsec

* All other conditions for ACK signal transition must exist.

T-52-33-27

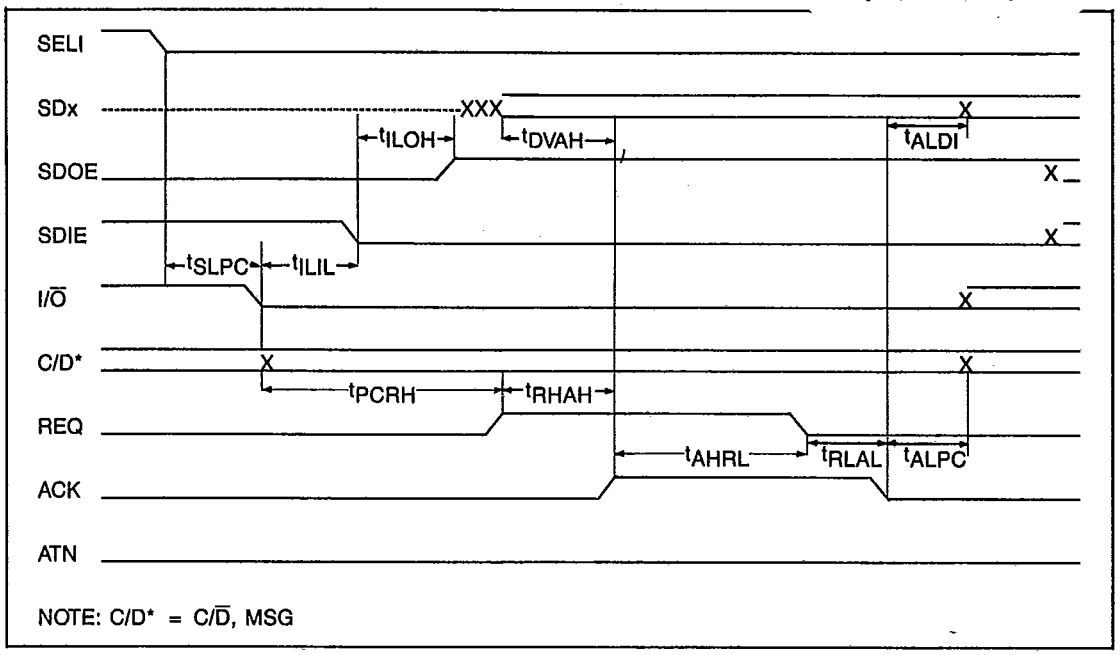


FIGURE 26. ASYNCHRONOUS INFORMATION TRANSFER OUT - INITIATOR - WD33C92

TABLE 39. ASYNCHRONOUS INFORMATION TRANSFER OUT - INITIATOR - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLPC}	SELI Low To Phase Change In	0		nsec
t_{ILIL}	I/O In Low To SDIE Low	0		nsec
t_{ILOH}	SDIE Low To SDOE High, Data Out	0		nsec
t_{PCRH}	Phase Change In To REQ In High	400		nsec
t_{DVAH}	Data Out Valid To ACK Out High	55		nsec
t_{RHAH}	REQ In High To ACK Out High	0		nsec
t_{AHRL}	ACK Out High To REQ In Low	0		nsec
t_{ALDI}	ACK Out Low To Data Out Invalid	0		nsec
t_{ALPC}	ACK In Low To Phase In Change	0		nsec
t_{RLAL}	REQ In Low To ACK Out Low	0		nsec

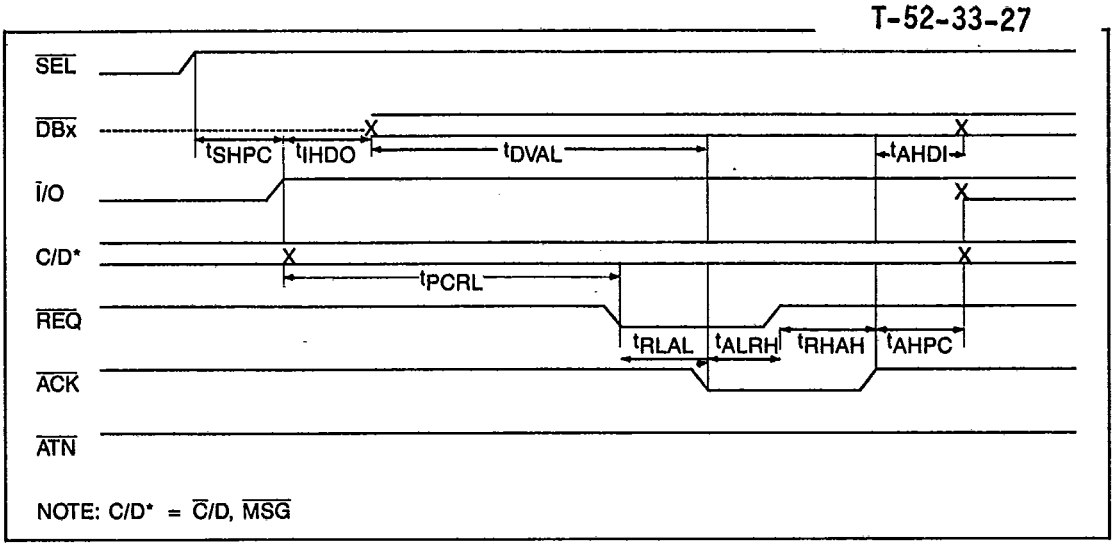


FIGURE 27. ASYNCHRONOUS INFORMATION TRANSFER OUT - INITIATOR - WD33C93

TABLE 40. ASYNCHRONOUS INFORMATION TRANSFER OUT - INITIATOR - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHPC}	SEL In High To Phase Change In	0		nsec
t_{IHDO}	I/O In High To Data Out	0		nsec
t_{PCRL}	Phase Change In To REQ In Low	400		nsec
t_{DVAL}	Data Out Valid To ACK Out Low	55		nsec
t_{RLAL}	REQ In Low To ACK Out Low	0	175*	nsec
t_{ALRH}	ACK Out Low To REQ In High	0		nsec
t_{AHDI}	ACK Out High To Data Out Invalid	0		nsec
t_{AHPC}	ACK Out High To Phase In Change	0		nsec
t_{RHAH}	REQ In High To ACK Out High	0	175*	nsec

* All other conditions for REQ transition must exist.

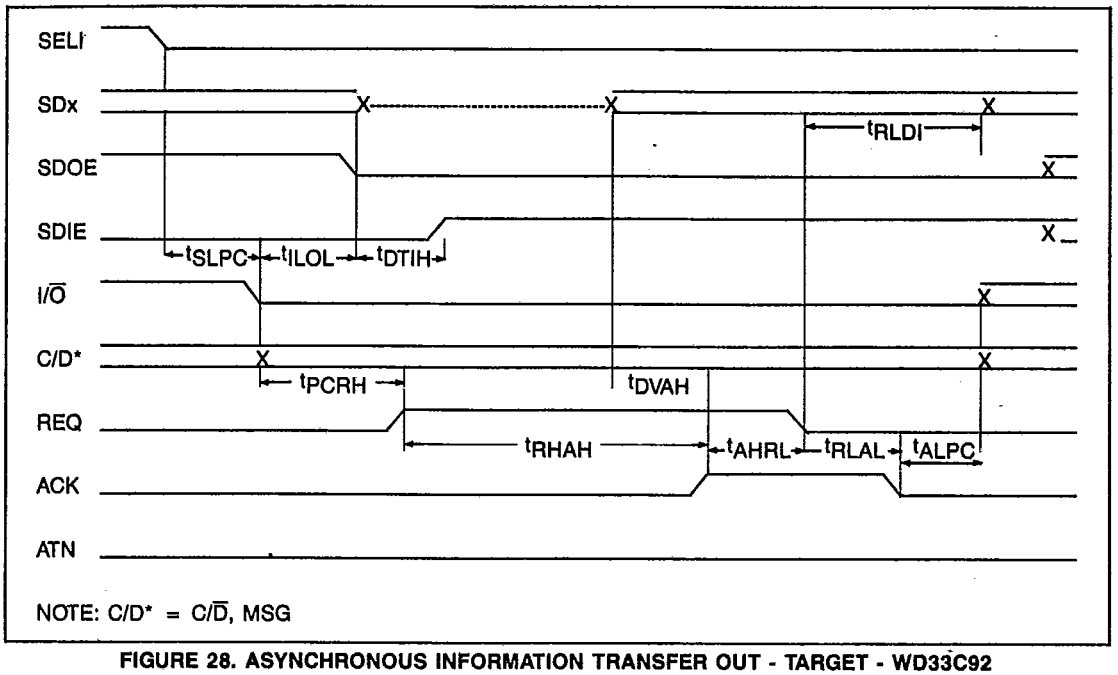


FIGURE 28. ASYNCHRONOUS INFORMATION TRANSFER OUT - TARGET - WD33C92

TABLE 41. ASYNCHRONOUS INFORMATION TRANSFER OUT - TARGET - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLPC}	SELI Low To Phase Change Out	100		nsec
t_{ILOL}	I/O Out To SDOE Low, Data Bus Tri-State	0	125	nsec
t_{DTIH}	Data Bus Tri-State To SDIE High	30		nsec
t_{PCRH}	Phase Change To REQ Out High	500		nsec
t_{DVAH}	Data In Valid To ACK In High	5		nsec
t_{RHAH}	REQ Out High To ACK In High	0		nsec
t_{AHRL}	ACK In High To REQ Out Low	0		nsec
t_{RLDI}	REQ Out Low To Data In Invalid	0		nsec
t_{ALPC}	ACK In Low To Phase Change Out	0		nsec
t_{RLAL}	REQ Out Low To ACK In Low	0		nsec

T-52-33-27

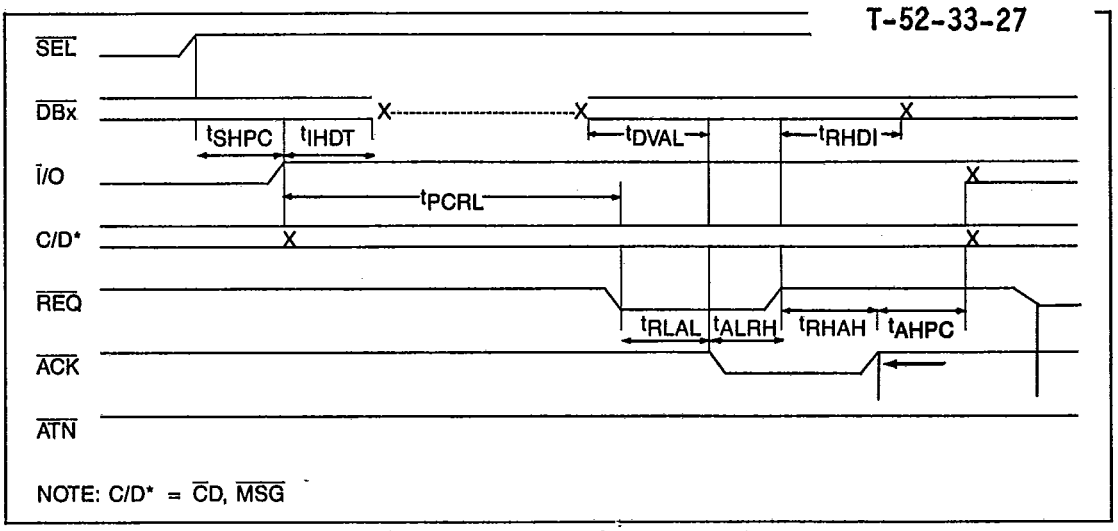


FIGURE 29. ASYNCHRONOUS INFORMATION TRANSFER OUT - TARGET - WD33C93

TABLE 42. ASYNCHRONOUS INFORMATION TRANSFER OUT - TARGET - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHPC}	SEL In High To Phase Change Out	100		nsec
t_{IHDT}	I/O Out High To Data Bus Tri-State	0	125	nsec
t_{PCRL}	Phase Change To REQ Out Low	500		nsec
t_{DVAL}	Data In Valid To ACK In Low	5		nsec
t_{RLAL}	REQ Out Low To ACK In Low	0		nsec
t_{ALRH}	ACK In Low To REQ Out High	0	175*	nsec
t_{RHDI}	REQ Out High To Data In Invalid	0		nsec
t_{AHPC}	ACK In High To Phase Change Out	0		nsec
t_{RHAH}	REQ Out High To ACK In High	0		nsec
t_{AHRL}	ACK In High To REQ Out Low	0	175*	nsec

* All other conditions for ACK signal transition must exist.

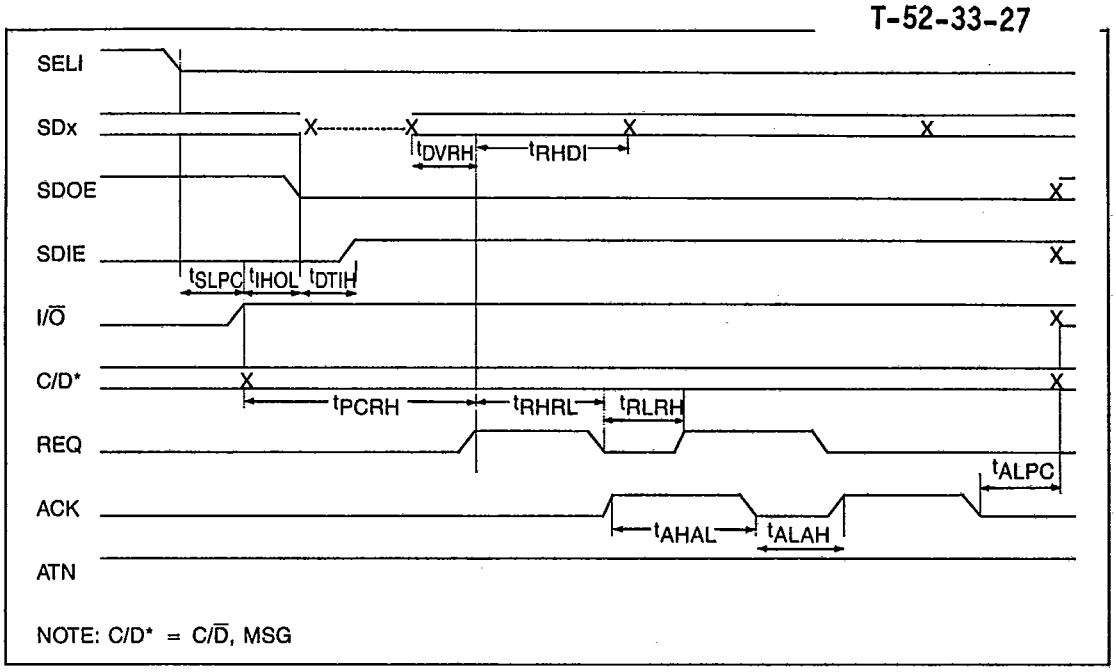


FIGURE 30. SYNCHRONOUS INFORMATION TRANSFER IN - INITIATOR - WD33C92

TABLE 43. SYNCHRONOUS INFORMATION TRANSFER IN - INITIATOR - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLPC}	SELI Low To Phase Change In	0		nsec
t_{IHOL}	I/O In High To SDOE Low, Data Bus Tri-State	0	100	nsec
t_{DTIH}	Data Bus Tri-State to SDIE High	30		nsec
t_{PCRH}	Phase Change In To REQ In High	400		nsec
t_{DVRH}	Data Valid In To REQ In High	5		nsec
t_{RHDI}	REQ In High To Data Invalid In	45		nsec
t_{RHRL}	REQ In High To REQ In Low	50		nsec
t_{RLRH}	REQ In Low To REQ In High	50		nsec
t_{AHAL}	ACK Out High To ACK Out Low	1		t_{CP}
		25		nsec
t_{ALAH}	ACK Out Low To ACK Out High	1		t_{CP}
		−25		nsec
t_{ALPC}	ACK Out Low To Phase Change In	0		nsec

* All other conditions for ACK signal transition must exist.

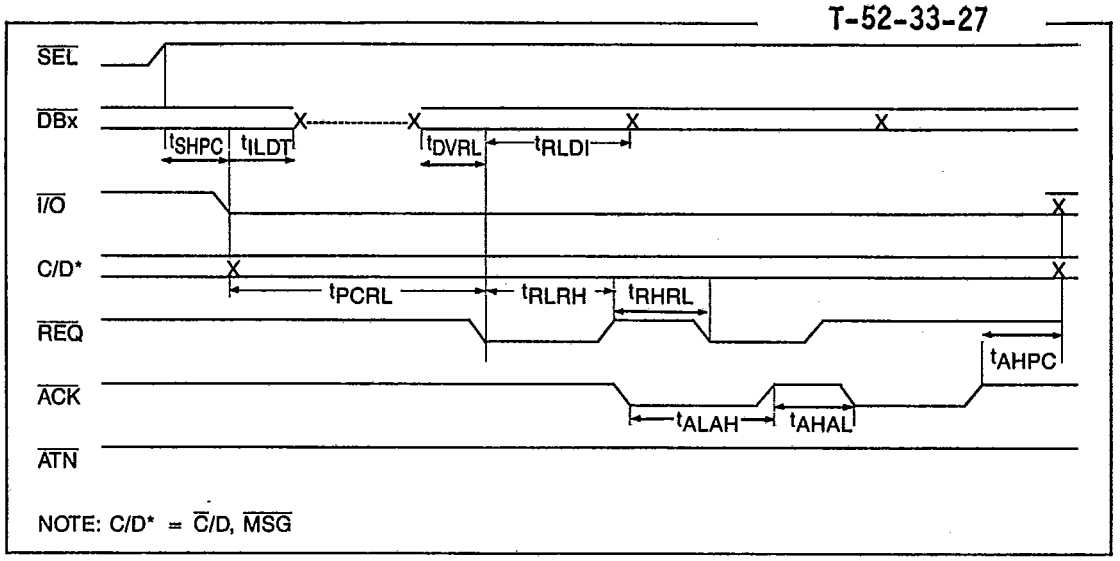


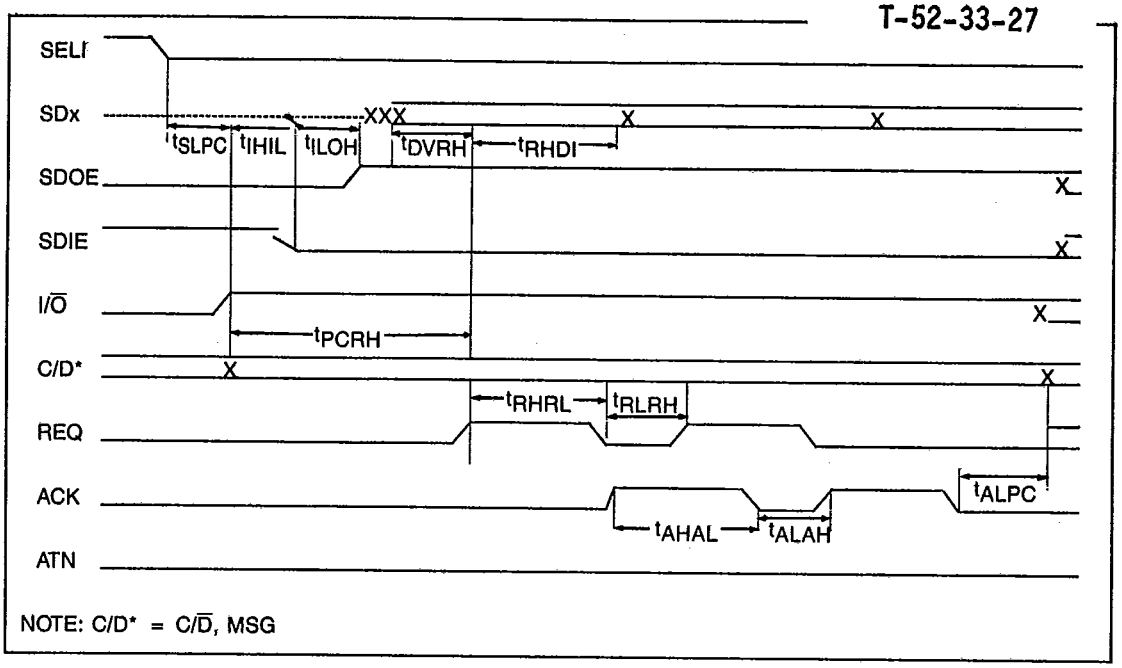
FIGURE 31. SYNCHRONOUS INFORMATION TRANSFER IN - INITIATOR - WD33C93

TABLE 44. SYNCHRONOUS INFORMATION TRANSFER IN - INITIATOR - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHPC}	SEL In High To Phase Change In	0		nsec
t_{ILDT}	I/O In Low To Data Bus Tri-State	0	125	nsec
t_{PCRL}	Phase Change In To REQ In Low	400		nsec
t_{DVRL}	Data Valid In To REQ In Low	5		nsec
t_{RLDI}	REQ In Low To Data Invalid In	45		nsec
t_{RLRH}	REQ In Low To REQ In High	50		nsec
t_{RHRL}	REQ In High To REQ In Low	50		nsec
t_{ALAH}	ACK Out Low To ACK Out High	1 −10		t_{CP} nsec
t_{AHAL}	ACK Out High To ACK Out Low	1 −25		t_{CP} nsec
t_{AHPC}	ACK Out High To Phase Change In	0		nsec

* All other conditions for ACK signal transition must exist.

T-52-33-27



NOTE: C/D* = C/$\overline{D}$, MSG

FIGURE 32. SYNCHRONOUS INFORMATION TRANSFER IN - TARGET - WD33C92

TABLE 45. SYNCHRONOUS INFORMATION TRANSFER IN - TARGET - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLPC}	SELI Low To Phase Change Out	100		nsec
t_{IHIL}	I/O Out High To SDIE Low	0		nsec
t_{ILOH}	SDIE Low To SDOE High, Data Out	0		nsec
t_{PCRH}	Phase Change Out To REQ Out High	500		nsec
t_{DVRH}	Data Valid Out To REQ Out High	55		nsec
t_{RHDI}	REQ Out High To Data Invalid Out	100		nsec
t_{RHRL}	REQ Out High To REQ Out Low	1		t_{CP}
		25		nsec
t_{RLRH}	REQ Out Low To REQ Out High	1		t_{CP}
		−25		nsec
t_{AHAL}	ACK In High To ACK In Low	50		nsec
t_{ALAH}	ACK In Low To ACK In High	50		nsec
t_{ALPC}	ACK In Low To Phase Change Out	0		nsec

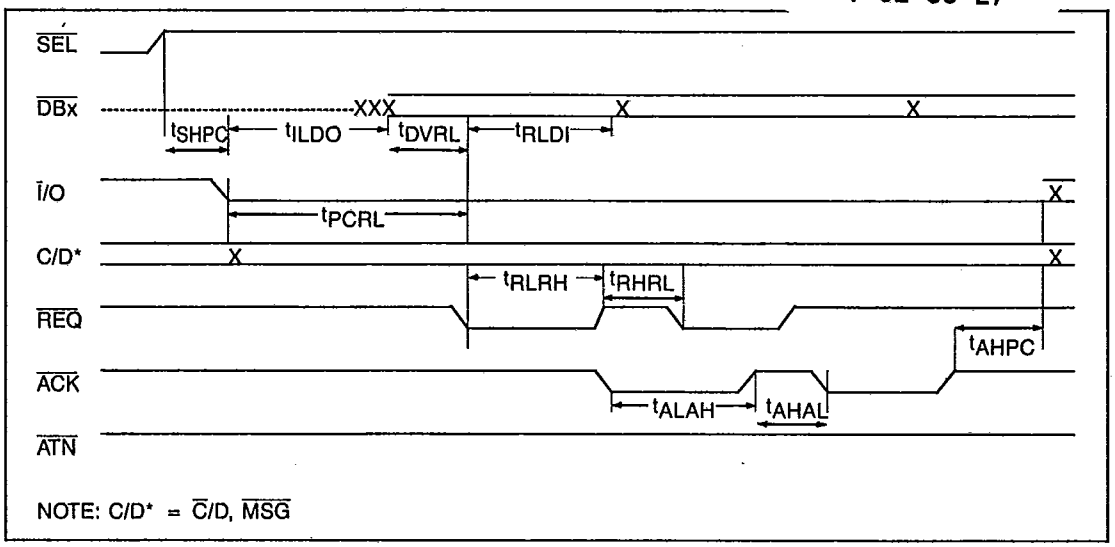


FIGURE 33. SYNCHRONOUS INFORMATION TRANSFER IN - TARGET - WD33C93

TABLE 46. SYNCHRONOUS INFORMATION TRANSFER IN - TARGET - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHPC}	SEL In High To Phase Change Out	100		nsec
t_{ILDO}	I/O Out Low To Data Out	0		nsec
t_{PCRL}	Phase Change Out To REQ Out Low	500		nsec
t_{DVRL}	Data Valid Out To REQ Out Low	55		nsec
t_{RLDI}	REQ Out Low To Data Invalid Out	100		nsec
t_{RLRH}	REQ Out Low To REQ Out High	1		t_{CP}
		−10		nsec
t_{RHRL}	REQ Out Low To REQ Out Low	1		t_{CP}
		−25		nsec
t_{AHAL}	ACK In High To ACK In Low	50		nsec
t_{ALAH}	ACK In Low To ACK In High	50		nsec
t_{AHPC}	ACK In High To Phase Change Out	0		nsec

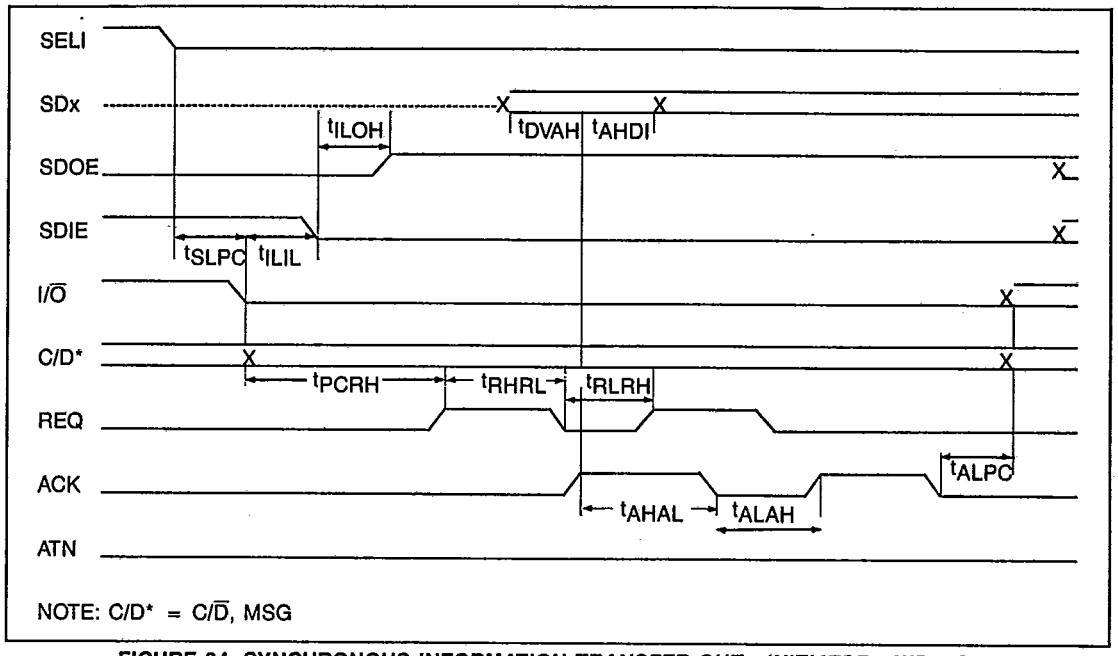
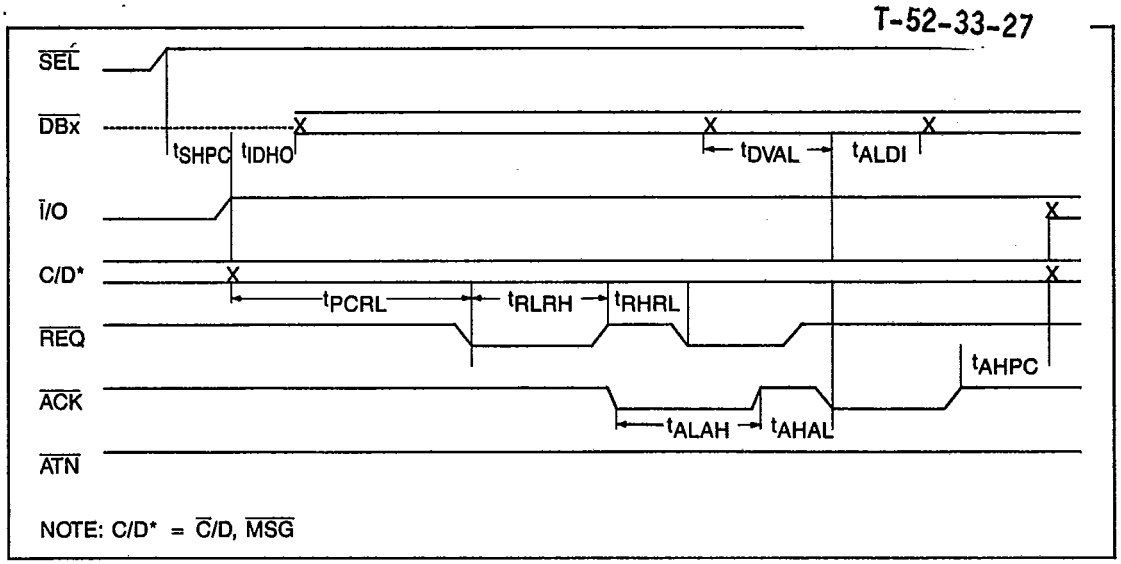


FIGURE 34. SYNCHRONOUS INFORMATION TRANSFER OUT - INITIATOR - WD33C92

TABLE 47. SYNCHRONOUS INFORMATION TRANSFER OUT - INITIATOR - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLPC}	SELI Low To Phase Change In	0		nsec
t_{ILIL}	I/O In Low To SDIE Low	0		nsec
t_{ILOH}	SDIE Low To SDOE High, Data Out	0		nsec
t_{PCRH}	Phase Change In To REQ In High	400		nsec
t_{DVAH}	Data Valid Out To ACK Out High	55		nsec
t_{AHDI}	ACK Out High To Data Invalid Out	100		nsec
t_{RHRL}	REQ In High To REQ In Low	50		nsec
t_{RLRH}	REQ In Low To REQ In High	50		nsec
t_{AHAL}	ACK Out High To ACK Out Low	1 25		t_{CP} nsec
t_{ALAH}	ACK Out Low To ACK Out High	1 −25		t_{CP} nsec
t_{ALPC}	ACK Out Low To Phase Change In	0		nsec

T-52-33-27



NOTE: C/D* = C/D, MSG

FIGURE 35. SYNCHRONOUS INFORMATION TRANSFER OUT - INITIATOR - WD33C93

TABLE 48. SYNCHRONOUS INFORMATION TRANSFER OUT - INITIATOR - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHPC}	SEL In High To Phase Change In	0		nsec
t_{IHDO}	I/O In High To Data Out	0		nsec
t_{PCRL}	Phase Change In To REQ In Low	400		nsec
t_{DVAL}	Data Valid Out To ACK Out Low	55		nsec
t_{ALDI}	ACK Out Low To Data Invalid Out	100		nsec
t_{RHRL}	REQ In High To REQ In Low	50		nsec
t_{RLRH}	REQ In Low To REQ In High	50		nsec
t_{AHAL}	ACK Out High To ACK Out Low	1 −10		t_{CP} nsec
t_{ALAH}	ACK Out Low To ACK Out High	1 −25		t_{CP} nsec
t_{AHPC}	ACK Out High To Phase Change In	0		nsec

T-52-33-27

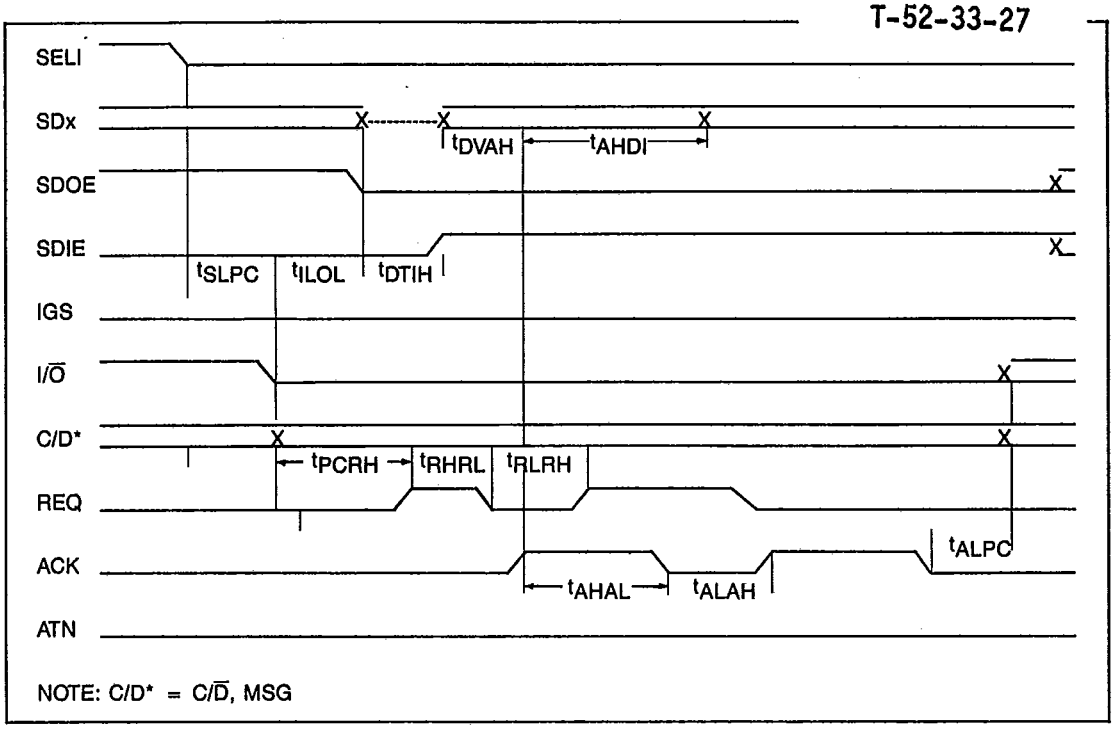


FIGURE 36. SYNCHRONOUS INFORMATION TRANSFER OUT - TARGET - WD33C92

TABLE 49. SYNCHRONOUS INFORMATION TRANSFER OUT - TARGET - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SLPC}	SELI Low To Phase Change Out	100		nsec
t_{ILOL}	I/O Out Low To SDOE Low, Data Bus Tri-State	0	125	nsec
t_{DTIH}	Data Bus Tri-State to SDIE High	30		nsec
t_{PCRH}	Phase Change To REQ Out High	500		nsec
t_{DVAH}	Data Valid In To ACK In High	5		nsec
t_{AHDI}	ACK In High To Data Invalid In	45		nsec
t_{RHRL}	REQ Out High To REQ Out Low	1		t_{CP}
		25		nsec
t_{RLRH}	REQ Out Low To REQ Out High	1		t_{CP}
		−25		nsec
t_{AHAL}	ACK In High To ACK In Low	50		nsec
t_{ALAH}	ACK In Low To ACK In High	50		nsec
t_{ALPC}	ACK In Low To Phase Change Out	0		nsec

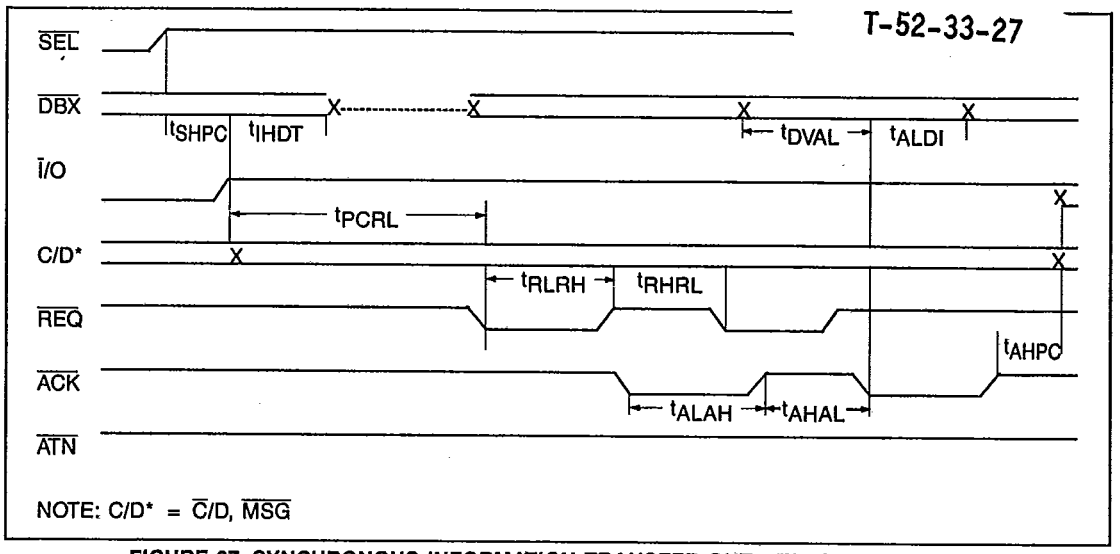


FIGURE 37. SYNCHRONOUS INFORMATION TRANSFER OUT - TARGET - WD33C93

TABLE 50. SYNCHRONOUS INFORMATION TRANSFER OUT - TARGET - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHPC}	SEL In High To Phase Change Out	100		nsec
t_{IHDT}	I/O Out High To Data Bus Tri-State	0	125	nsec
t_{PCRL}	Phase Change To REQ Out Low	500		nsec
t_{DVAL}	Data Valid In To ACK In Low	5		nsec
t_{ALDI}	ACK In Low To Data Invalid In	45		nsec
t_{RHRL}	REQ Out High To REQ Out Low	1		t_{CP}
		−25		nsec
t_{RLRH}	REQ Out Low To REQ Out High	1		t_{CP}
		−10		nsec
t_{AHAL}	ACK In High To ACK In Low	50		nsec
t_{ALAH}	ACK In Low To ACK In High	50		nsec
t_{AHPC}	ACK In Low To Phase Change Out	0		nsec

T-52-33-27

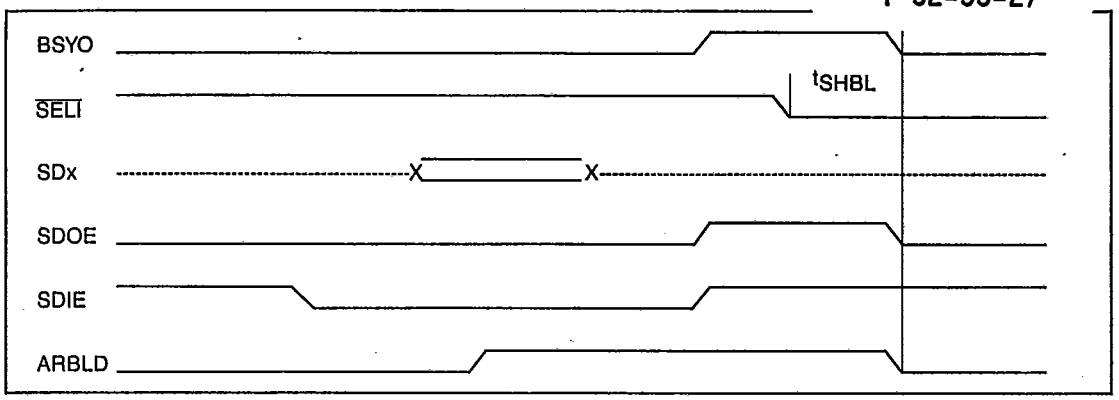


FIGURE 38. ARBITRATION TO BUS FREE - WD33C92

TABLE 51. ARBITRATION TO BUS FREE - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHBL}	$\overline{SEL}$I High To BSYO, SDOE, And ARBLD Low		9 +75	t_{CP} nsec

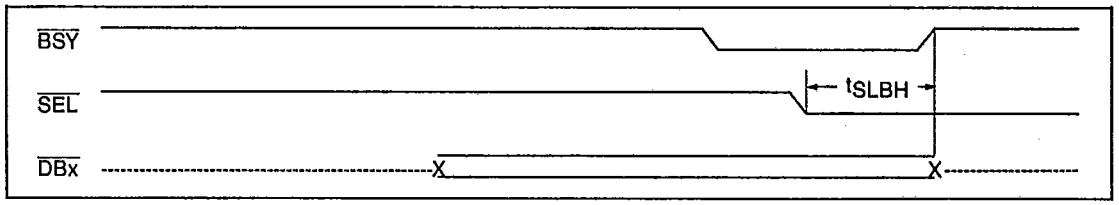


FIGURE 39. ARBITRATION TO BUS FREE - WD33C93

TABLE 52. ARBITRATION TO BUS FREE - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{SHBL}	$\overline{SEL}$ In Low To $\overline{BSY}$ High, Data Tri-State		9 +75	t_{CP} nsec

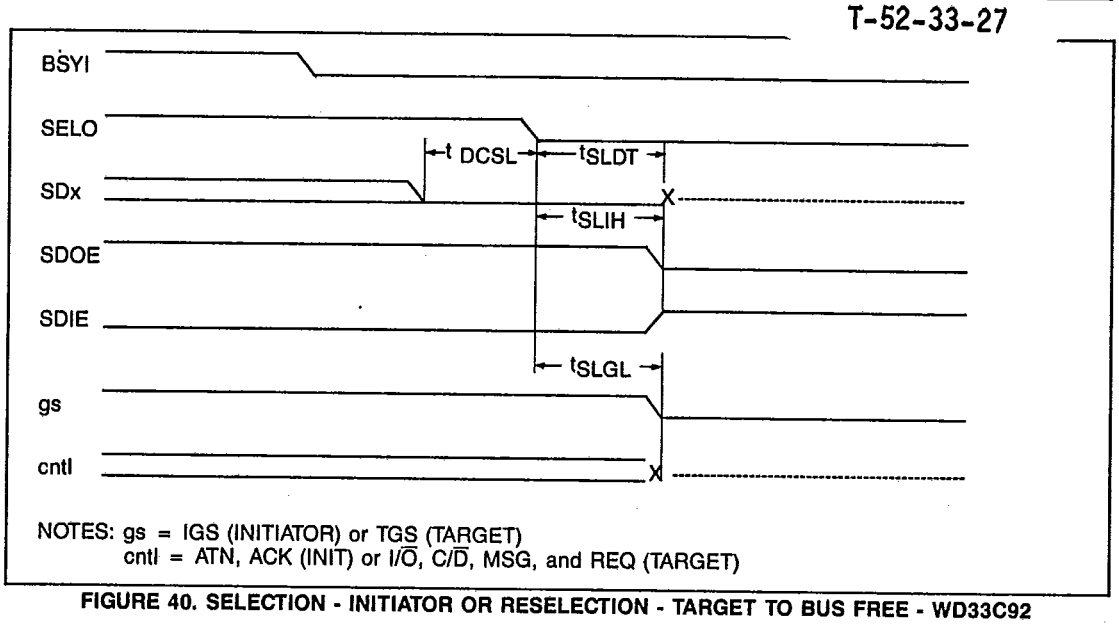


FIGURE 40. SELECTION - INITIATOR OR RESELECTION - TARGET TO BUS FREE - WD33C92

TABLE 53. SELECTION - INITIATOR OR RESELECTION - TARGET TO BUS FREE - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{DCSL}	Data Bus Cleared To SELO Low	200		usec
t_{SLIH}	SELO To SDIE High, SDOE Low		9	t_{CP}
			+75	nsec
t_{SLDT}	SELO Low To Data Bus Tri-State		9	t_{CP}
			+75	nsec
t_{SLGL}	SELO Low To gs Low, cntl Tri-State		9	t_{CP}
			+75	nsec

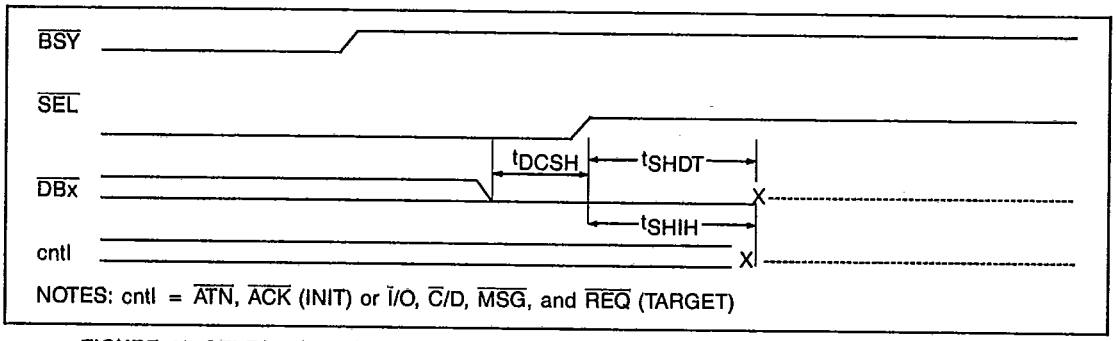


FIGURE 41. SELECTION - INITIATOR OR RESELECTION - TARGET TO BUS FREE - WD33C93

TABLE 54. SELECTION - INITIATOR OR RESELECTION - TARGET TO BUS FREE - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{DCSH}	Data Bus Cleared To SEL Out High	200		usec
t_{SHDT}	SEL Out High To Data Bus Tri-State		9	t_{CP}
			+75	nsec
t_{SHIH}	SEL Out High To cntl Tri-State		9	t_{CP}
			+75	nsec

T-52-33-27

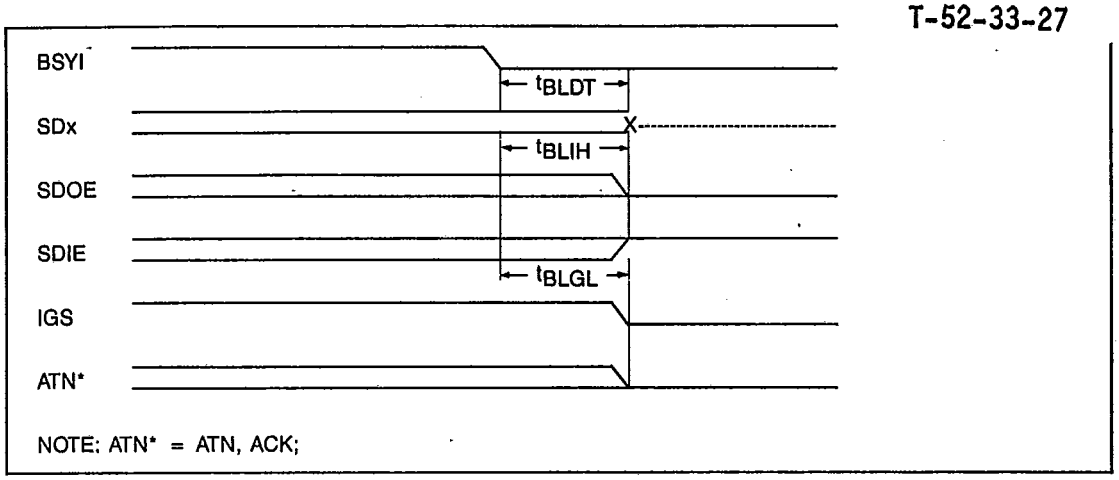


FIGURE 42. CONNECTED-AS-AN-INITIATOR TO BUS FREE - WD33C92

TABLE 55. CONNECTED-AS-AN-INITIATOR TO BUS FREE - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{BLIH}	BSYI Low To SDIE High, SDOE Low		9 +75	t_{CP} nsec
t_{BLDT}	BSYI Low To Data Bus Tri-State		9 +75	t_{CP} nsec
t_{BLGL}	BSYI Low To IGS Low, ATN Tri-State		9 +75	t_{CP} nsec

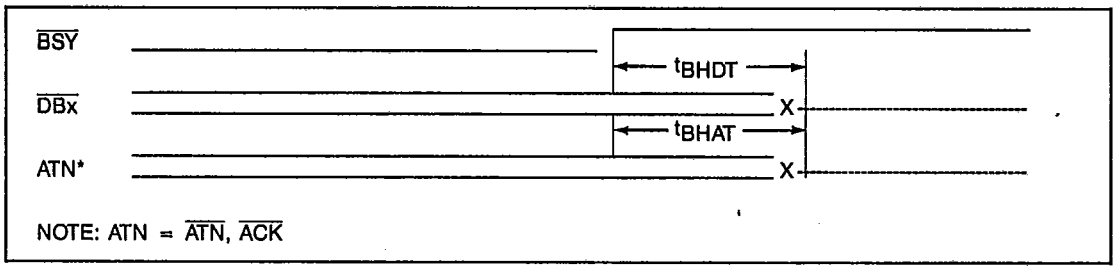


FIGURE 43. CONNECTED-AS-AN-INITIATOR TO BUS FREE - WD33C93

TABLE 56. CONNECTED-AS-AN-INITIATOR TO BUS FREE - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{BHDT}	BSY In High To Data Bus Tri-State		9 +75	t_{CP} nsec
t_{BHAT}	BSY Low To ATN Tri-State		9 +75	t_{CP} nsec

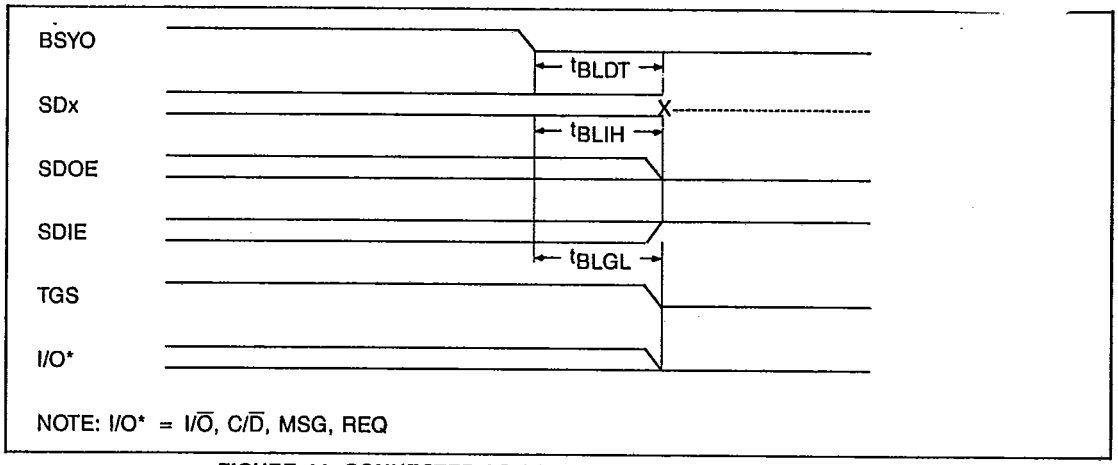


FIGURE 44. CONNECTED-AS-A-TARGET TO BUS FREE - WD33C92

TABLE 57. CONNECTED-AS-A-TARGET TO BUS FREE - WD33C92

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{BLIH}	BSYO Low To SDIE High, SDOE Low		9 +75	t_{CP} nsec
t_{BLDT}	BSYO Low To Data Bus Tri-State		9 +75	t_{CP} nsec
t_{BLGL}	BSYO Low To TGS Low, I/O Tri-State		9 +75	t_{CP} nsec

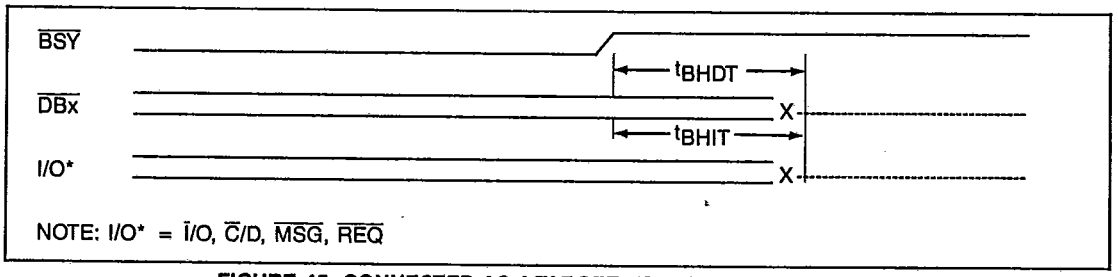
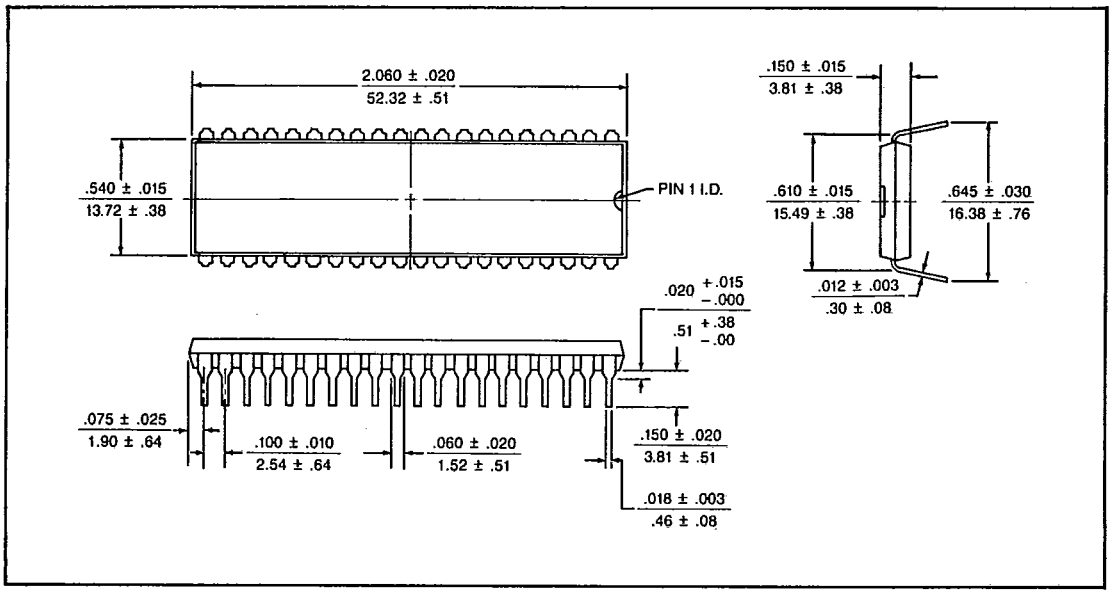


FIGURE 45. CONNECTED-AS-A-TARGET TO BUS FREE - WD33C93

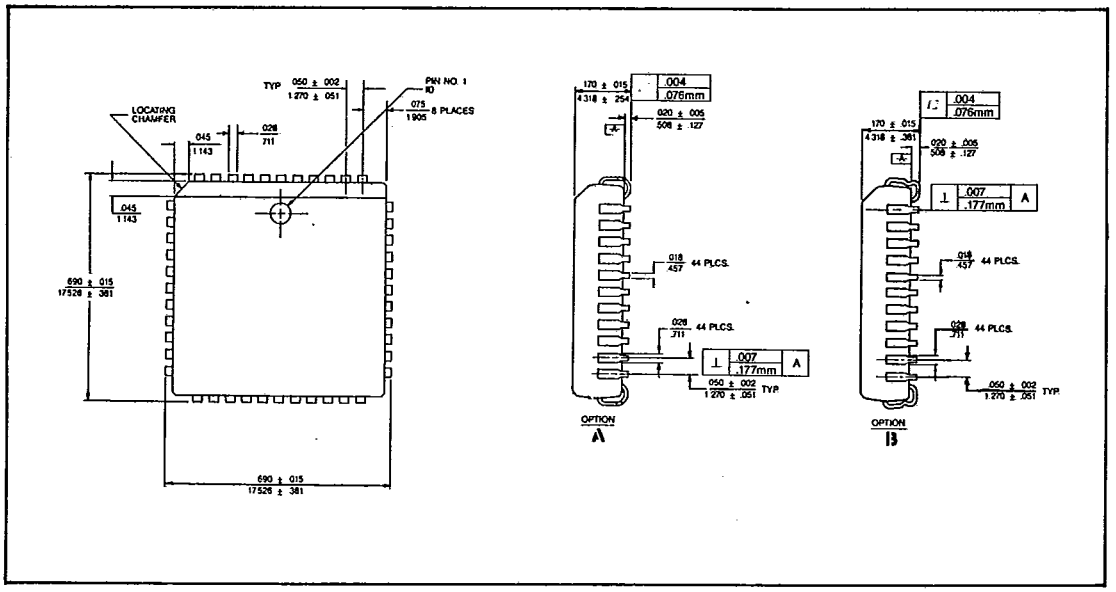
TABLE 58. CONNECTED-AS-A-TARGET TO BUS FREE - WD33C93

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
t_{BHDT}	BSY Out High To Data Bus Tri-State		9 +75	t_{CP} nsec
t_{BHIT}	BSY Out High To I/O Tri-State		9 +75	t_{CP} nsec

PACKAGE DIAGRAMS



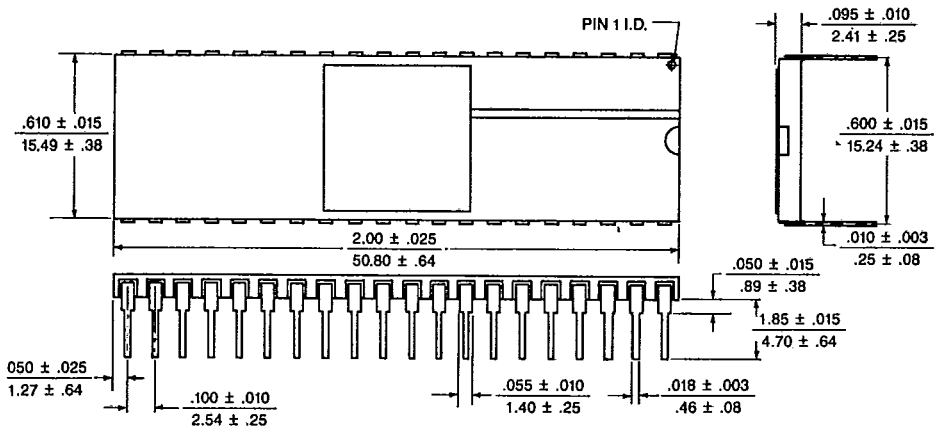
40 LEAD PLASTIC "PL"
WD33C93



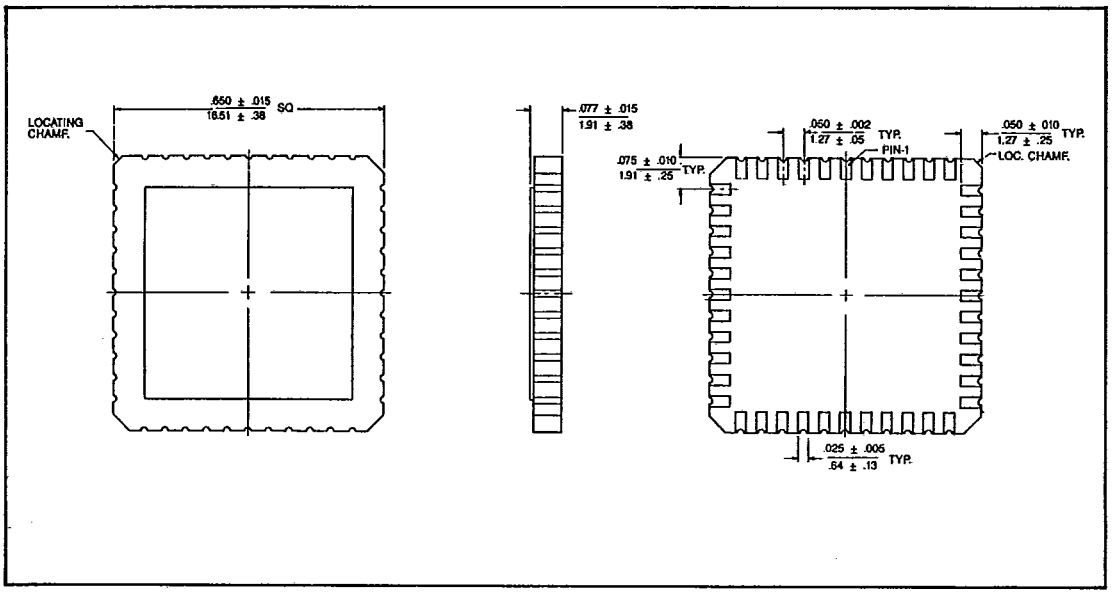
44 LEAD PLASTIC "JM"
WD33C92 and WD33C93

DRAWING NOT AVAILABLE
AT THIS TIME

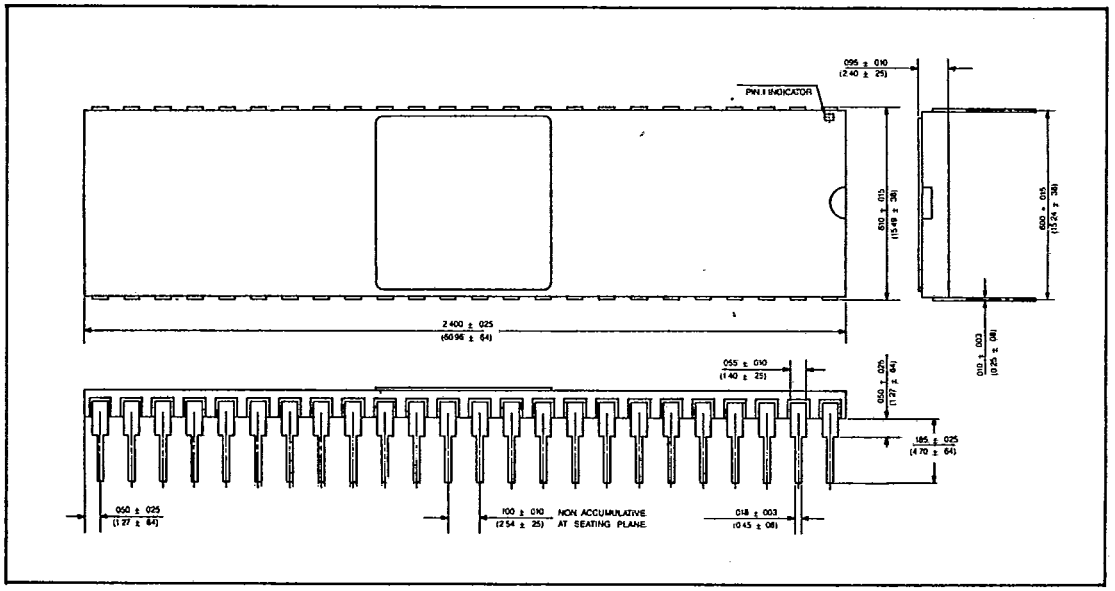
48 LEAD PLASTIC "JN"
WD33C92



40 LEAD CERAMIC "AL"
WD33C93



44 LEAD CERAMIC "DM"
WD33C92 and WD33C93



48 LEAD CERAMIC "AN"
WD33C92