WESTERN DIGITAL

Storage LSI Applications Note

T-52-38

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PRODUCT: Model # WD60C31B
Manf # 7032

January 20, 1993
E-301A

WD60C31B Data Sheet

Documentation Source: Preliminary Engineering Specification rev. X.3, 1/20/93

General Features: The WD60C31B is an optical disk drive encoder/decoder. The primary functions of this device are the conversion of NRZ data to RLL 2:7 encoded data, conversion of RLL 2:7 encoded data to NRZ data, detection and generation of a variety of special marks on the media, and the detection of certain data error conditions.

Refer to Applications Note: E146 for version differences
E147 for manual corrections, additions, and notes
E-301A for Bin 03 and Bin 04 version differences

Branding Information:

Model#	Manf#	Description
WD60C31BJM00 03	7032_B00JM03	Current Production
WD60C31BJM00 04	7032_B00JM04	Current Production
WD60C31AJM00 02	7031_A00JM02	Obsolete
WD60C31JM00 02	6031KB00JM02	Obsolete

Application Note revision history:

revision	E052-A:	Initial release
	E052-B:	Added page numbers, register bit corrections for Primary Configuration register in section 4.2.1, page 28, 29, 29a.
	E-301A:	Added 30MHz Bin 03 and 40MHz Bin 04 differences Applications Note and updated table 5.1, page 55 with Bin 03 and Bin 04 differences.

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WD60C31B

OPTICAL DRIVE ENCODER/DECODER

ENGINEERING SPECIFICATION

January 20, 1993
REVISION X.3

SPECIFICATION UPDATES

DATE	SECTION	DESCRIPTION
5/25/89	4.21	Redefine Status Bit (Enable Flag Field Enable)
5/25/89	4.2.2	Define Status Clear Operation
5/25/89	4.2.15	Reorder Status Bits
01/20/93	5.1 &5.2	Table 5.1 (Added Bin 04 Timings)

TABLE OF CONTENTS

TABLES

FIGURES

SECTION 1 GENERAL DESCRIPTION

1.1 Scope

This specification provides design, interface, and programming information which is needed to use the WD60C31B in an optical disc drive enviornment. The following documents are recommended as reference material:

ADS10C00 Programming Reference Manual
ADS10C00 Product Specification
X3B11/88-095-R1 ANSII 130mm Reversible Optical Disk Cartridge Part 4
X3B11/88-150-R2 ANSII 90mm Reversible Optical Disk Cartridge Part 4
WD60C31B Firmware Application Note

1.2 Description

The WD60C31B is an optical disc drive encoder/decoder. The primary functions of this device are the conversion of NRZ data to 2:7 data, conversion of 2:7 data to NRZ data, detection and generation of a variety of special marks on the media, and the detection of certain data error conditions.

This device supports the "Continous/Composite" data format as proposed in the ANSI X3B11 committee. In addition, soft sectored media is also supported. However, the format must conform to specifications defined in Section 2.

1.3 Features

- o ANSI X3B11 5.25 and 3.5 inch Format compatibility
- o Conversion of RLL (2:7) data to NRZ data
- o Conversion of NRZ data to RLL (2:7) data
- o Track formatting capability
- o Sector Mark Detection and Generation (5 3 3 7 3 3 3 5)
- o Programmable Rotational Speed tolerance of +/- .5 % and +/- 1 %
- o ID Address Mark Detection and Generation (16 code bits)
- o Data Address Mark Generation and Detection (48 code bits)
- o Variable Threshold Voting for Data Address Mark Detection
- o RESYNC generation and detection (16 code bits)
- o Programmable Resync Window Size

- Support Extended Recovery Techniques
- WORM flag generation and detection
- WD10C00 interface support
- 3 ID "on the fly " Support (ID Voting Capability)
- Automatic ID Track and Sector Increment Functionality
- Track Streaming Support
- Extensive Error Status

SECTION 2 FUNCTIONAL OVERVIEW

2.1 Introduction

The following section describes the WD60C31B functionality as it relates to the ANSI standard Continuous-Composite Format for 5 1/4" and 3 1/2" optical drives. In addition, the WD60C31B can perform a track format operation on medias which is not preformatted. This device also performs ID voting functions that previously was the responsibility of the ADS10C00.

2.2 Optical Format Review

The ANSI specified Continuous-Composite Optical Media format is intended for use in WORM and magneto-optic drive applications. The WD60C31B is tailored for this application. Programmability of the WD60C31B has been added to accomodate many possible changes to the present format.

2.2.1 Sector Format Description

The sector format is divided into three primary zones. The first zone is the ID area. This contains the sector mark and the three unique ID fields. The second zone is the Drive area. The Mirror Mark, FLAG, and ALPC fields are contained in the area. The Mirror Mark and ALPC are intended for servo use. The FLAG field is WORM application specific. The FLAG and ALPC are not used in the 3.5" application. The last zone is the Data field. The Data, CRC, and ECC are contained in this area.

2.2.1.1 Sector Mark

The five byte sector mark is intended to be detected without recourse to use of the phase-locked loop. This pattern does not exist in data. Alternating long burn times of 3 and 5 equivalent NRZ data bit times are used to identify the sector mark.

2.2.1.2 VFO Areas

There are three different lock up areas designated as VFO1, VFO2, and VFO3. The recorded information for VFO1 and VFO3 is identical in length and pattern. The area for VFO2 will have one of two different patterns and will be 4 bytes shorter than VFO1 and VFO3.

Given that there are three concatenated I.D. fields and RLL 2,7 modulation coding is used, the conditions leading into each VFO2 area will be different depending on the last byte of CRC recorded in the preceeding I.D. field.

A different VFO pattern prior to ID 2 and 3 is needed in order to allow the last byte of CRC to achieve correct decoding. Notice that while the entering pattern is different, the VFO2 fields always end in the same pattern. The choice between the two patterns for VFO2 will depend on the content of the last byte of CRC in the ID field immediately preceeding the one being read.

2.2.1.3 AM Address Mark

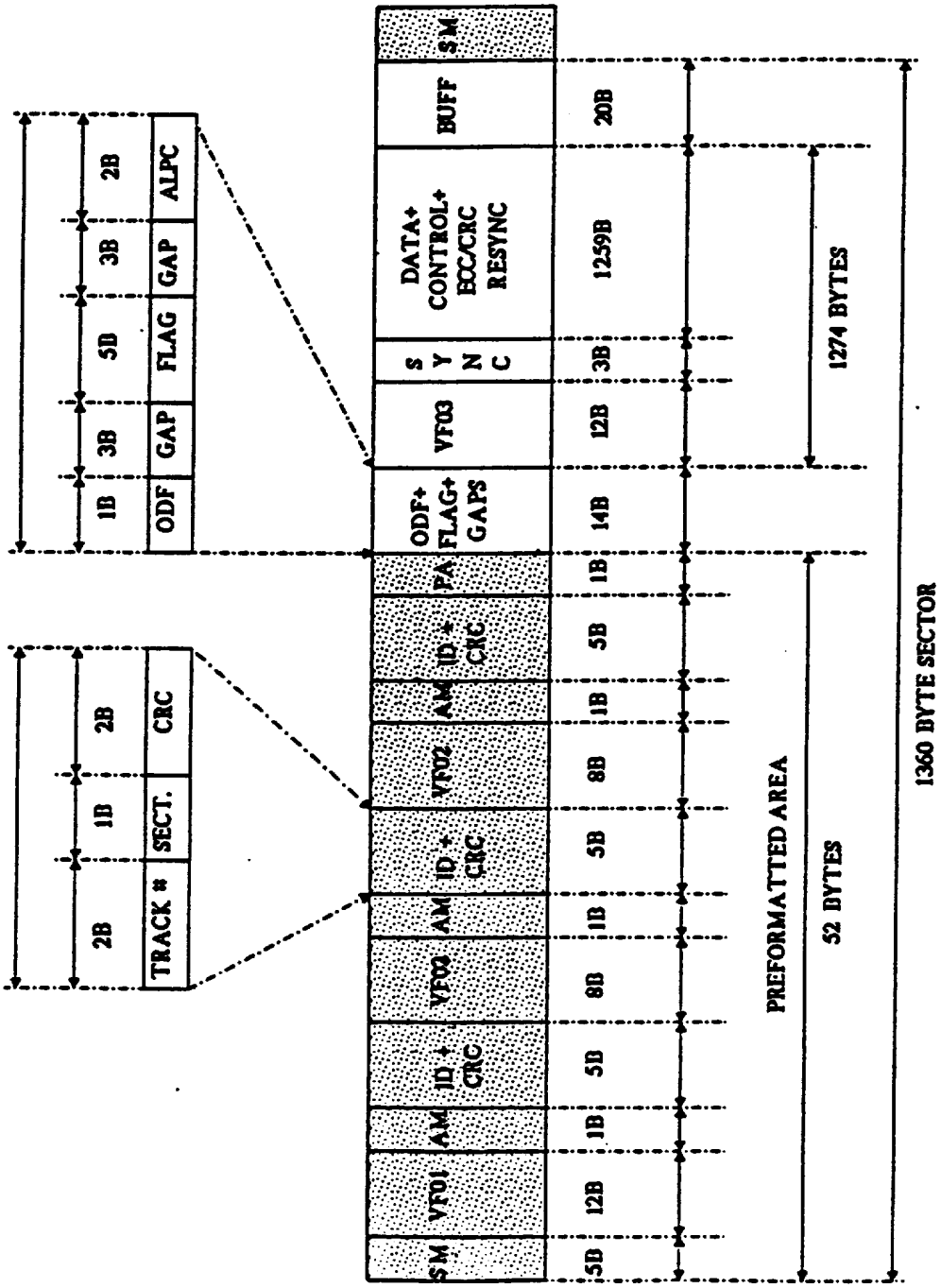
The Address Mark is a special pattern, not used in RLL 2,7 data, and is a run-length violation for RLL (2,7) encoding.

SECTOR FIELD FUNCTIONS

Name	Function	Pattern
SM	Sector Mark	Special Redundant Pattern = 5 3 3 7 3 3 3 3 5 channel code bit pattern following sector mark = = 0010010010
VFO1,2,3	Lock up Field	VFO1= 01001001001...010010 VFO2= 10010010010...010010 VFO2= 00010010010...010010 VFO3= 01001001001...010010 NOTE: VFO2 varies based on previous CRC pattern
AM	Address Mark	(Bit/Byte Sync) 16 code bits, (1 byte) 0100 1000 0000 0100
SYNC	Redundant sync for data	: Triple sync pattern 0100 0010 0100 0010 0010 0010 0100 0100 1000 0010 0100 1000
ID	Track no. (2B) Sector no. (1B)	High order/Low order bits 7-6= ID Number(ID 0-2) bit 5 = Reserved,(S/B 0) bits 4-0= Sector Number
CRC	ID Field Check Bytes	CCITT Polynomial seed=1's
PA	Postamble	Allows last CRC byte closure under RLL (2,7) modulation
ODF	Offset Detection Flag	Not written, no grooves
Gap	Gap (Splice)	Not written 3 byte areas
FLAG	Indicate Written Block	Continuous Pulse (5byte area, decision by majority) 1001001001001001001001001100..
ALPC	Auto Laser Pwr Control	Blank 2 byte zone
DATA	User Data, Control,CRC,ECC & Resync	Info see fig. 7
BUFFER	Used for RPM timing margins	Not Written area
RESYNC	Data Field byte sync	16 code bits (1byte) 0010 0000 0010 0100

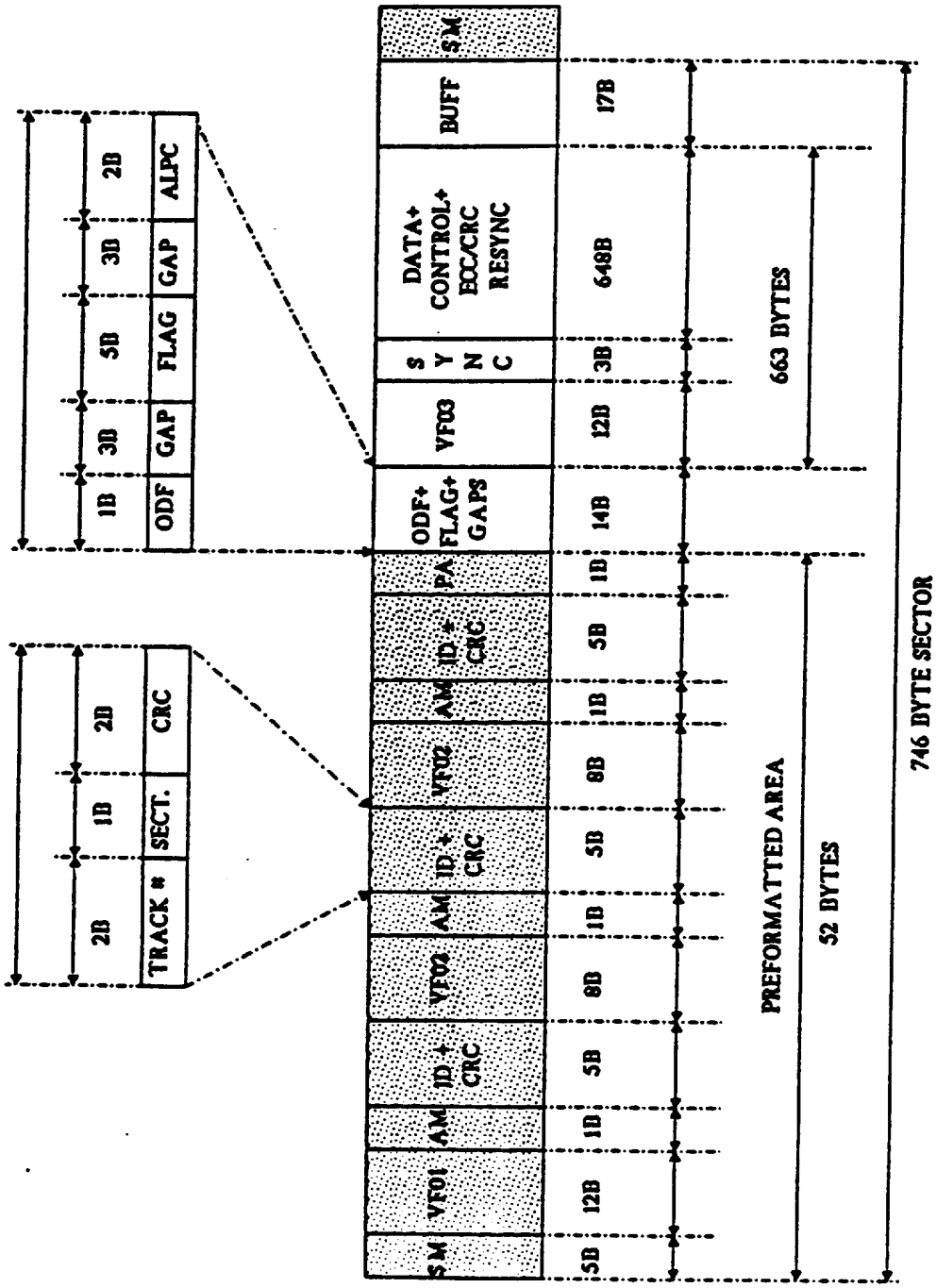
TABLE 2.1

NOTE:All patterns show channel code bits in RLL (2,7) modulation.



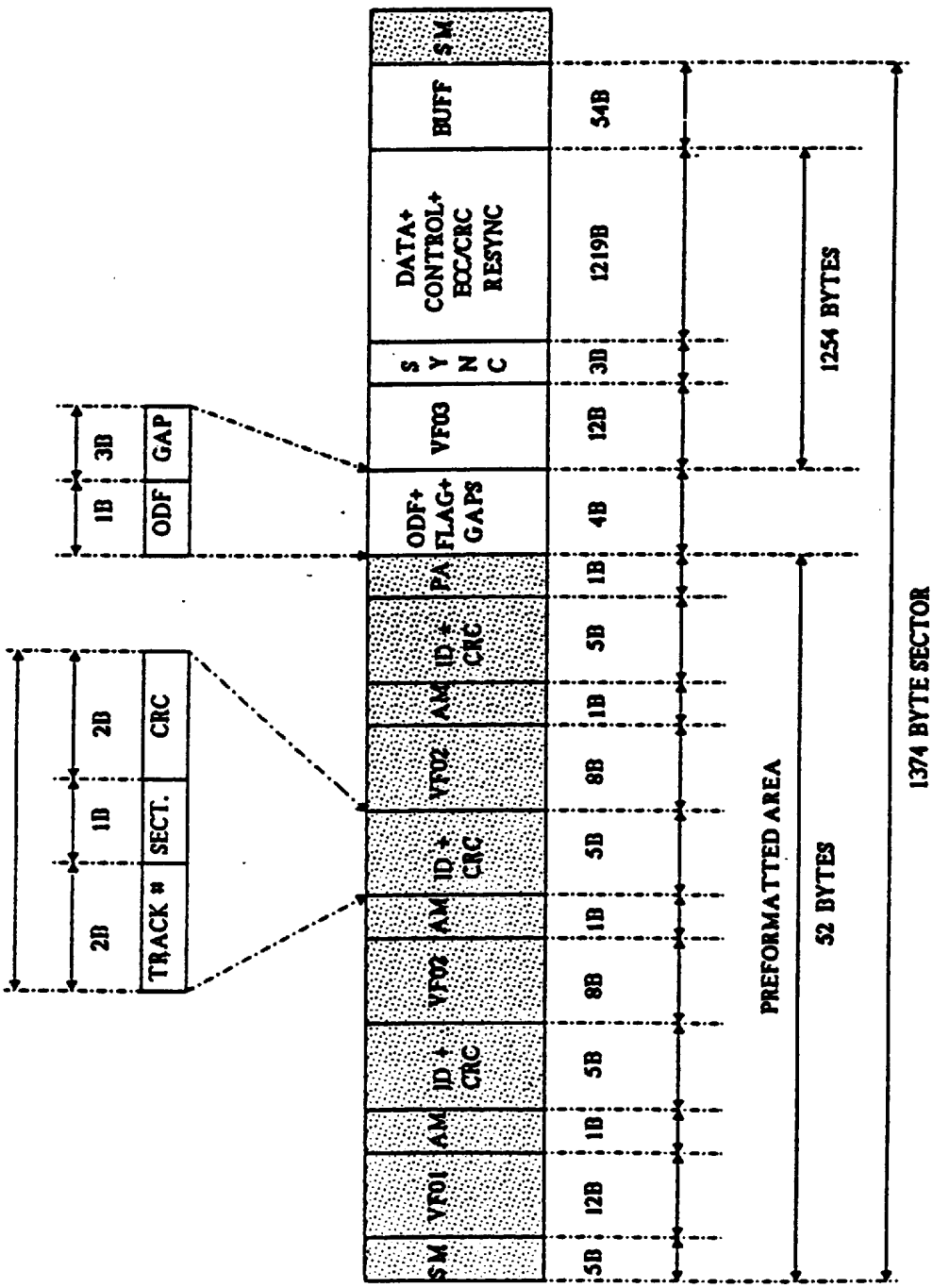
5 1/4" 1024 BYTE FORMAT

Fig. 21



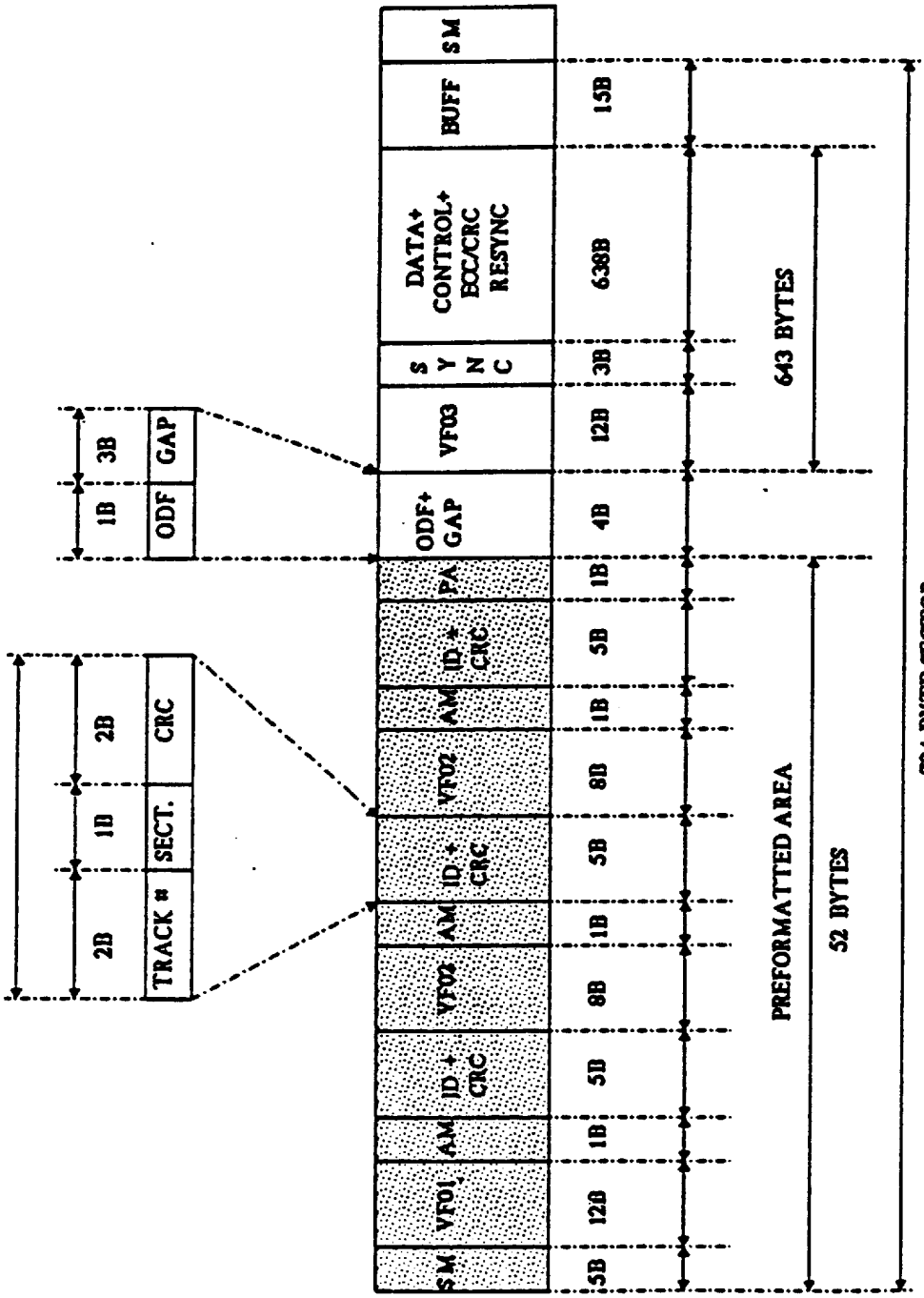
5 1/4" 512 BYTE FORMAT

Fig. 22



3 1/2" 1024 BYTE FORMAT

Fig. 23



3 1/2" 512 BYTE FORMAT

Fig. 24

2.2.1.4 ID + CRC

The ID field consists of 5 bytes, allocated as follows:

- o 2 bytes of track address, MSB/LSB.
- o 1 byte of sector address:

bits 7,6 = ID number, (which of 3 ID fields)
00 = 1st ID
01 = 2nd ID
10 = 3rd ID
bit 5 = Reserved for future expansion, (S/B 0)
bits 4-0 = Sector Number, (binary value, MSbit = 4)

The CRC consists of two bytes calculated over the previous three bytes of ID information using the polynomial:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The CRC calculation is begun with the registers seeded to all 1's, (Ref. CCITT CRC standard). Input and output sequence uses MSB first.

2.2.1.5 PA Postamble

The last portion of the preformatted area consists of a one byte postamble on the third ID field. Due to the use of the RLL 2,7 encoding scheme, the framing of the last byte of CRC in the last ID field is uncertain within a few bit times. The postamble allows the last byte of CRC to achieve closure and permits the ID field to always end in a predictable manner. This is necessary in order to locate the following field, (ODF /mirror mark) in a consistent manner.

2.2.1.6 ODF / Mirror Mark

The Offset Detection Flag or Mirror Mark is an area with no grooves or preformatted data. The purpose is to allow track offset detection within the drive.

2.2.1.7 FLAG

The purpose of the flag area is to prevent inadvertent write operations over previously written data in WORM drive application. The flag may be written after the data area write operation successfully completes or during the same pass. The use of this field is optional. This field is not used in 3.5 inch format.

2.2.1.8 ALPC

This area is designated as a test area for calibration of the laser power levels by the drive. It is grooved. This area is not used on 3.5 inch format.

2.2.1.9 DATA FIELD

The data field consists of 1024 bytes of user data and 223 bytes of CRC/ECC/Resync information, plus 12 bytes of control information. A 512 byte data field is optional. The 3.5" format has reduced the pointer field to XXX bytes for the 512 byte sector.

2.2.1.10 RESYNC

The purpose of the resync mark is to reestablish byte synchronization when byte synchronization is lost during a data segment. (A "data segment" is the bytes of data, usually 15 or 20 bytes, between resync marks.

Resync marks are used in only the Data/Control/ECC/CRC field.

Resync marks are written within the data field as shown in figures 7 and 8.

2.2.1.11 BUFFER

Motor speed tolerances and other electrical /mechanical tolerances require a buffer zone at the end of each sector. No written information is present in the buffer. Also present in the Buffer field is a one byte postamble to the Data Field to allow closure of channel bits in the RLL 2,7 encoding scheme. However, during format this area is filled with the high frquency pattern "100".

2.2.2 WD60C31B Functions

2.2.2.1 Read Operation

The WD60C31B is responsible for the detection of the following special format marks :

- Sector Mark

The WD60C31B is constantly in a sector mark detection mode. If a sector mark is detected (3 of 5 majority), a SPDET pulse is sent to the ADS10C00. If no sector mark is detected at the end of each sector, the WD60C31B creates a SPDET. The created SPDET is based on a worst case speed tolerance of +/-.5 or 1 % . This mark is detected under a window, .5% or 1%, thereby minimizing misdetection.

- ID Address Mark

The WD60C31B examines the input RLL bit stream whenever an ID field area is expected and RDGATE is active. RDGATE should be applied after a SPDET is sent. The RLL pattern that is expected is microproceesor programmable. The RRCLKs are paused when RDGATE is raised and NRZI goes from high to a low. Once the ID AM is detected, the RRCLKs begin again. The NRZI data stream will be a byte of zeros and the ID field; track high byte, track low byte and sector byte, follows. A SYNCDET pulse is also sent. This pulse is sent along with the first ID address byte. Refer to Section 5.1.4. The ADS10C00 should be programmed to wait for the SYNCDET and expect the track high byte to be the Address mark. The ADS10C00 then performs a bit for bit comparision and CRC verification. The WD60C31B can also be placed in another mode, the ID Search mode. This mode should be used whenever the track high byte is not predictable. This is used to satisfy ADS10C00 requirements. In this mode, the SYNCDET signal is moved forward one byte. This means that this signal becomes active during the byte of zeros preceding the track high byte. The ADS10C00 should be programmed to wait for the SYNCDET and an address mark of zeros. A bit for bit comparision over the complete ID field is performed. The ADS10C00 stores the full ID field in its internal registers. The Normal mode only stores the track low byte, sector byte, and CRC.

- Data Address Mark

The WD60C31B examines the input RLL bit stream whenever the Data field area is expected and RDGATE is active. The RLL pattern that is expected is microprocessor programmable. In addition, the level of pattern corelation is programmable. A SYNCDET pulse is sent whenever a comparison is made. This pulse is sent along with a psuedo-address mark NRZ byte of '00's. The ADS10C00 is programmed for this comparision.

- Data Resync Marks

The WD60C31B must detect and remove the Resync marks from the NRZI data stream. An internal window is generated which predicts the location of next resync. This window minimizes the probabilty of misdetection. In the normal mode the internal resync window is opened if RDGATE is raised in the data field the Data Sync has been detected and a data segment has passed. The size of this window is programmable to four sizes. Two sizes are fixed. Two sizes are variable sizes. The ANSI specification states that the quantity of bytes of a data segment is 15 or 20. The WD60C31B permits the microprocessor the set the value from 0 to 31 bytes. A value of zero assumes that there are no resyncs. In addi-

tion, the Resync mark pattern can also be programmed. In an error recovery mode, the RDGATE must be applied in a data field but data sync mark need not be detected. Instead, the Resync mark is the first mark to be detected. The first resync window is opened after a preprogrammed number of bytes are sent to the ADS10C00. This means that the ADS10C00 receives the exact number of data bytes per sector. This mode is used if the the data sync was undetectable after lowering the Data Sync Threshold value.

2.2.2.2 Write Operation

During write, the ADS10C00 and WD60C31B work together to write the following patterns: 1) VFO field, 2) Data Address Mark, 3) Encoded RLL Data, 4) Data Resync Marks, and 5) Data Postamble. It is the responsibility of the ADS10C00 to send a 'dummy' VFO pattern. This 'dummy' VFO pattern is the exact number of bytes that are written on the disc. The WD60C31B creates the actual high frequency pattern,100100. The WD60C31B continues writing this pattern until an AMENA signal is sent from the ADS10C00. This AMENA signal is sent with the last byte of the 'dummy' VFO. When the AMENA is received, the VFO is completed at a byte boundary and the Data Sync Mark is injected into the RLL data stream. pulse which intiates the writing of the Data Sync Mark. When the WD60C31B inserts the Data Sync Mark or the Rsync Marks into the RLL data stream, the RRCLKs are paused. This action halts the data byte transfer through the ADS10C00. In effect, the ADS10C00 is unaware of this pause. The This pausing of the RRCLKs is also performed during a read operation. The ADS10C00 sends data bytes, CRC bytes, and ECC bytes. An AMENA is sent with the last byte of the ECC field. This action ends the insetion of the RESYNC marks into the encoded RLL data stream. Refer to Section 5.1.5 for the AMENA timing requirements. In addition, 3 bytes of pad should be sent after the last byte of ECC. These bytes are required to compensate for the WD60C31B internal pipeline structure and closure requirements of the last bit of the last byte of ECC.

2.2.2.3 Format Operation

The WD60C31B is also capable of performing a track format operation. This permits the WD60C31B to operate with drives which use prestamped media and nonstamped media. The format must conform to the prestamped format requirements.

The task of formatting the media is shared by the ADS10C00 and WD60C31B. In general, the ADS10C00 must 1)keep track of the quantity bytes that are written on the track and 2) inform the WD60C31B when the special marks;(sector mark, ID address marks, and Data Sync Mark), are to be inserted into the RLL data stream. The WD60C31B is responsible for 1) encoding and decoding the NRZ serial data from the ADS10C00, 2) inserting the special marks mentioned above (also Resync marks), and predicting the next type of special mark to be written.

The general format sequence is as follows:

1) All special marks are programmed in the WD60C31B

2) The WD60C31B has been set for Track Format (Secondary Configuration Reg)

3) An Index is provided by the drive to the ADS10C00

4) The ADS10C00 raises Write Gate when Index is received. NRZ data transfer begins. The first NRZ data bit that is sent must a 1 which indicate.

5) Upon receiving Write Gate, the WD60C31B begins writing the first Sector Mark. All subsequent sector marks are written when a specific number of AMENAs are received. The NRZ data from the ADS10C00 is internally pipelined within the WD60C31B. When the pipeline is full, the RRCLKs are paused. When the writing of the sector mark is complete the RRCLKs start again and NRZ data encoding begins and is merged into the RLL data stream.

6) The WD60C31B continues to encode the NRZ data until it receives an AMENA. This pulse from the ADS10C00 define the concurrent NRZ data byte as the last byte before the next special mark. The special mark is inserted and encoding continues. RRCLKs are restarted. The WD60C31B keeps track of the quantity of AMENAs that are sent. The type of special mark to be inserted is based on the quantity of AMENA signals received.

2.2.2.4 Modulation Method

The modulation method used to record all information on the disk in the formatted areas shall be the Run-Length Limiting, (RLL) code known as RLL (2,7).

CODE CONVERSION

NRZ Input Bits	RLL (2,7) Channel Code Bits
10	0100
010	100100
0010	00100100
11	1000
011	001000
0011	00001000
000	000100

TABLE 2.2

2.2.2.5 ID Voting ("On the Fly" ID Verification)

In addition to the previously mentioned methods of ID read operations, the WD60C31B can perform ID Voting. In this mode, the WD60C31B detects and verifies the validity of the 3 IDs. The IDs undergo the following test. A valid ID Address Mark byte must be detected, a bit for bit comparision of the Track and sector bytes must be sucessful, and the CRC from the drive must match an internally derived CRC. If these parameters are met, a single ID is considered valid. The user can program the quantity of ID(s) which must be found to satisfy a write or read operation. When all conditions are met, the ADS10C00 is sent SYNCDET and an address mark byte of "F0" on the NRZI line. If all conditions are not met, the ADS10C00 is set a SYNCDET and an address mark byte of "FF".

Track Streaming is also supported. This means that the internally stored track and sector values can automatically be incremented when the ID threshold is met. The user must set up three conditions. First, the three ID mode must be enabled. Second, the maximum sectors per track must be set.Third, the track and/or sector autoincrement funtion can be independently enabled. This function minimizes the microprocessor overhead between sector IDs.

SECTION 3 SIGNAL DESCRIPTION

3.1 ORGANIZATION

The WD60C31B signals are functional divided into the following three (3) groups:

- o Disc Controller Interface 11 pins
- o PLL Interface 11 pins
- o Microprocessor Bus Interface 17 pins
- o General Support 5 pins

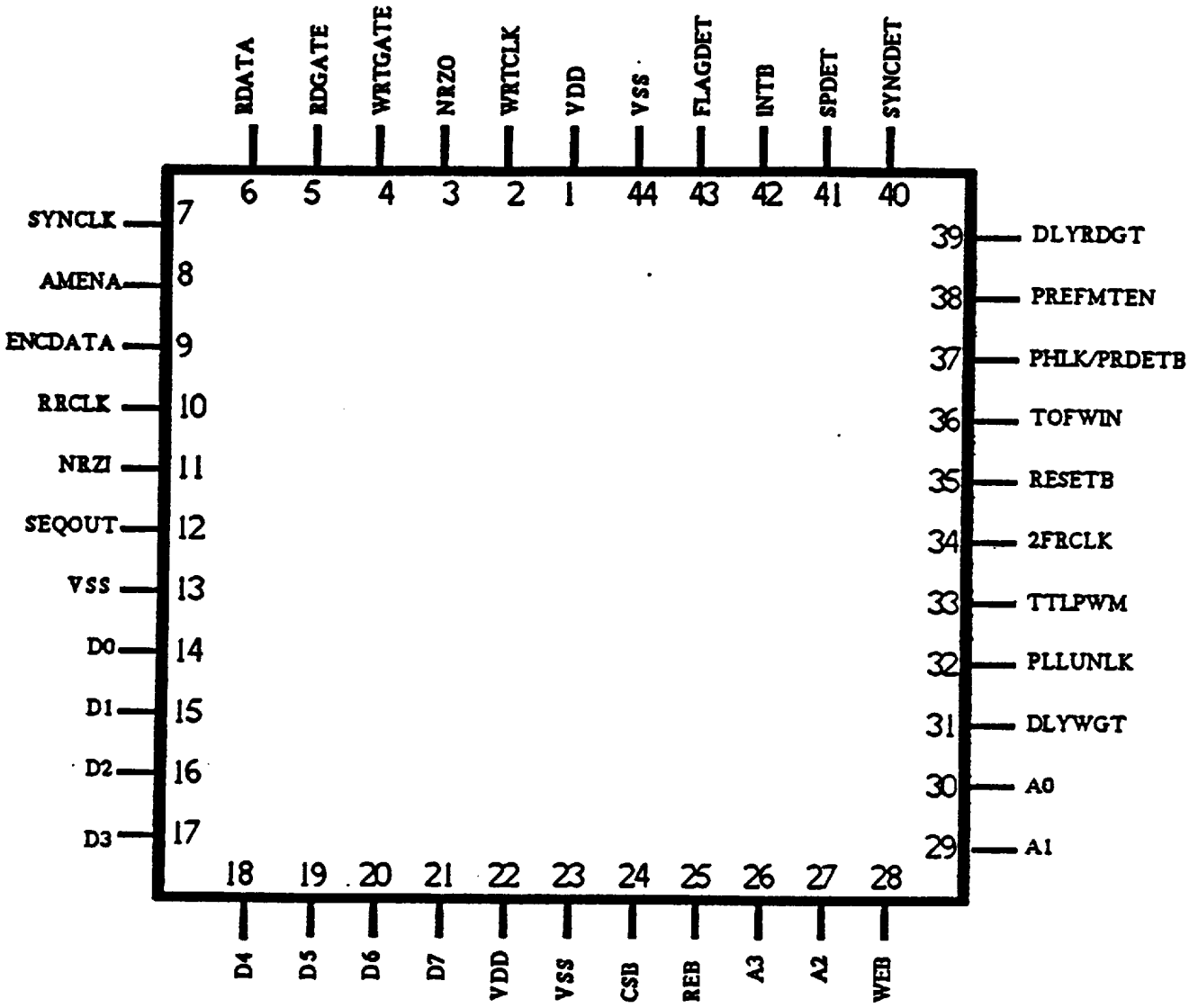
The following tables describe each of the pins. The pins are identified by pin number, name, input or output, and circuit descriptor (Section 6 has more details).A small explanation is also included.

3.2.1 Disc Controller

PIN NO.	PIN NAME	NAME	I/O	CKT TYP	FUNCTION
4	WRTGATE	Write Gate	I	A	Writing of data onto the drive
3	NRZO	NRZ data input	I	A	NRZ serial data from disc controller
2	WRTCLK	Write Clk	I	A	Write data input clock from disc controller (inversion of RRCLK)
11	NRZI	NRZ data output	O	B	NRZ serial data to disc controller
10	RRCLK	Read Clk	O	B	Multiplexed 2FRCLK / SYNCLK to disc controller
5	RDGATE	Read gate	I	A	Enable read gate during read
41	SPDET	Sector pulse det.	O	B	Sector mark has been detected or end of SM window
40	SYNCDET	Sync detected	O	B	Address mark has been detected
43	FLAGDET	Flag/gap detected	O	B	The WD60C31B has detected the flag field
8	AMENA	Address Mark Enable	I	A	The WD60C31 should write the Data Sync Mark
12	SEQOUT	Window Toggle	I	A	The ADS10C00 indicates the location of the data field

TABLE 3.1

CKT TYP (Refer to Section 6 for more detail)
- A = Input (Section 6.2.1)
- B = Output (Section 6.2.2)



60C31A PINOUT

Figure 3.1

3.2.2 PLL Interface

PIN NO.	PIN NAME	SIG NAME	I/O	CKT TYP	FUNCTION
6	RDATA	Read Data	I	A	Data from the PLL which is synchronized to 2XRCLK
7	SYNCLK	PLL Clk	I	A	This is the PLL clock. It is derived from REFCLK dur- a write operation
33	TTLPWM	Input data	I	A	Raw input from the heads
9	ENCDATA	Output data	O	B	Write data from WD60C31B to read/write heads
37	PHLK	PLL phase lock	O	B	Sets PLL in phase mode
34	2FRCLK	Reference Clock	I	A	This is the PLL reference clock
31	DLYWGT	Delayed Wrt gate	O	B	Buffered write gate to heads
39	DLYRDGT	Delayed Rd Gate	O	B	Buffered read gate to PLL
36	TOFWIN	TOF Window	O	B	Identifies the location of mirror mark. 1 or 2 byte times.
38	PREFMTEN	Preformat enable	O	B	A signal which selects the gain of the read channel. This signal is programmable
32	PLLUNLK	PLL unlock enable	I	C	A signal indicates if the PLL has gone out of lock.

TABLE 3.2

CKT TYP (Refer to Section 6 for more detail)
- A = Input (Section 6.2.1)
- B = Output(Section 6.2.2)

3.2.3 Microprocessor Interface

PIN NO.	PIN NAME	SIG NAME	I/O	CKT TYP	FUNCTION
21-14	D7-D0	Data Bus	I/O	C	8 bit bidirectional data bus for transferring status,data and control of the WD60C31B
26,27 29,30	A3-A0	Addr. Bus	I	A	Nonmultiplexed address bus
25	REB	Read Enable	I	C	Read strobe for the internal registers in PIO.
28	WEB	Wrt Enable	I	C	Write strobe for internal registers during PIO
24	CSB	Chip Select	I	A	CS- is the master chip enable for the WD60C31
42	INTB	Interrupt Request	O	B	Output to uP requesting a status transfer
35	RESETB	Master Reset	I	A	Master resets all internal register and tristate all outputs

TABLE 3.3

CKT TYP (Refer to Section 6 for more detail)
- A = Input (Section 6.2.1)
- B = Output(Section 6.2.2)
- C = Bidirectional (Section 6.2.3)

3.2.4 General Support

PIN NO.	PIN NAME	SIG NAME	FUNCTION
1 22	VDD	+5 Volts	Supply Voltage
13 23 44	VSS	Ground	Digital Ground

TABLE 3.4

SECTION 4 REGISTER ASSIGNMENTS

4.1 General

The WD60C31B has 32 read/write locations.

4.1.1 Register Address Assignments

Address	Write Function	Read Function
X'0'	Configuration Write	Configuration Read
X'1'	Software reset	Operation Error Status
X'2'	Data Resync MSB byte	Data Resync MSB byte
X'3'	Data Resync LSB byte	Data Resync LSB byte
X'4'	ID Address Mark MSB byte	ID Address Mark MSB byte
X'5'	ID Address Mark LSB byte	ID Address Mark LSB byte
X'6'	Data Sync Bytes (6 bytes)	Pointer Counter Status
X'7'	Sync Threshold/TOF Size	Sync.Threshold/TOF Size
X'8'	Data Size/RESYNC Limit	Data Size/RESYNC Error Flag
X'9'	Data Sync Pointer Reset	Future ID Track/Sector (3 Bytes)
X'A'	Phase Lock Delay	Phase Lock Delay
X'B'	Secondary Configuration	Secondary Configuration
X'C'	Third Configuration	Third Configuration
X'D'	ID Preset Track/Sector (3 Bytes)	ID Preset Track/Sector (3 bytes)
X'E'	ID Control	ID Status (3 Bytes)
X'F'	Sector/Track	Sector/Track

TABLE 4.1

4.2 General Control Registers

4.2.1 Primary Configuration : Address X'0'

read/write :

7	6	5	4	3	2	1	0
FF	ID	SS	IE	WT	PE	M1	M0

FF = Enable Flag field detection

Active State = 1

This bit enable the flag detection logic. Eight rising edges of ~~RDATA~~ TTLPOH during an internally created flag window signifies a flag detection, FLGDET goes active. In addition, all write operations are disabled until the next sector mark if a flag is detected . An interrupt is also generated if bit 4 of this register is set.

ID = Enable ID Search Mode

Active state = 1

Normally, during a read operation the WD60C31B sends an AMDET (in the Bit 1 position) with the first byte of decoded RLL data after a ID Address Mark is detected. If the controller is trying to read the ID field the concurrent byte is the *Track High Byte*. The ADS10C00 uses the *Track High byte* as an address mark byte and stores only the subsequent NRZI bytes in its internal register. If the Track High Bytes do not match, the ADS10C00 does not store the subsequent ID field. The programmer can activate this bit and perform another ID read operation. The WD60C31B then moves the AMDET foward by 8 RRCLKs and sends a byte of 0's. The ADS10C00 is then programmed to wait for SYNCDET and expect an address mark byte of zeros. This means that the ADS10C00 will internal store the Track High Byte along with the subsequent bytes. This mode is normally used after a seek operation to determine the head position.

SS = Select sector size

Active State = 1

When this bit is active, a sector size of 1024 data bytes is selected. When inactive a sector size of 512 data bytes is selected. The Secondary Configuration Register further defines the total number of bytes per sector.

SS	SE35	IDW	Bytes/Sector	Mode Definition
0	0	0	746	5.25" - 512 bytes
1	0	0	1360	5.25" - 1024 bytes
0	1	0	725	3.5" - 512 bytes
1	1	0	1394	3.5" - 1024 bytes
0	0	1	746	Aux. Mode - 512
1	0	1	1360	Aux. Mode - 1024

IE = Enable Interrupt

Active State = 1

This is the master interrupt enable bit. An interrupt occurs because of seven possible conditions. They are:

1) Data Read Complete

At the end of each data field read operation an interrupt is generated if interrupts are enabled and bit 5 of ID Control/Status Register is set.

2) Flag Field/WRTGATE Error

This bit is set if a flag field is detected and a write operation was attempted in this sector. An Interrupt is possible if bit 7 of this register are set.

3) Psuedo SPDET/WRTGATE Error

This bit is set if a psuedo SPDET was generated and a write operation was attempted. An interrupt is generated if bit 0 of the Third Configuration Register and bit 4 of this register are set.

4) Resync Threshold Exceeded Error

If the programmed missing RESYNC counter equals or exceeds the programmed limit, this bit is set. An interrupt is generatedif bit 4 of the ID Control/Status Register and bit 4 of this register are set.

5) RDGATE/SPDET Error

This bit is set if if RDGATE is applied and a SPDET is generated. An Interrupt is generated if bit 4 of the Secondary Configuration Register and bit 4 of this register is set.

6) ID Miscompare Error

If the "on the fly" three ID detection logic is unable to met the programmed ID threshold, an interrupt is generated concurrent to the transfer of an invalid ID AM byte transfer on the NRZI pin. Bit 4 of this register must be set.

7) Read Stop Interrupt

This bit is set when RDGATE is applied after the next SPDET. An interrupt is generated Bit 7 of the Sector per Track Register and bit 4 of this register are set.

WT = Internal Test Mode

This is used for IC testing purposes only

PE = Preformat enable control

Active State = 1

When set this permit the PREFMTEN signal to go low 47 bytes after the sector mark. This is used in magneto-optic preformatted media applications.

M1,M0 = Select Data Recovery Mode

M1	M0	MODE
0	0	Normal Data Transfer
0	1	Recovery Mode 1 : Disable Data Sync det During a data field read, a fixed number of data segments are sent as soon as read gate is active without waiting to detect the Data Sync Mark first. This mode is selected when the Sync Mark can't be detected irregardless of the Sync Threshold. The number of data segments are determined by Third Config. Reg.
1	0	Recovery Mode 2 : Invalid Code Bit Map w/sync The NRZ Data that is sent to the ADS10C00 is not the decoded RLL data. Instead, it is a map of the invalid RLL code bit of the data stream An NRZI bit '1' indicates an RLL violation
1	1	Recovery Mode 3 : Invalid Code Bit Map w/resyn This mode performs both RLL code violation mapping (Mode 2) and disabling of Data Sync detection (Mode 1)

The following interrupt functions have individual enables. In order for these interrupt functions to be enabled, BOTH the general enable (bit 4 of the Primary Configuration register) AND the individual enable must be set:

FUNCTION	Individual Interrupt Enable
Data Read Complete	Section 4.2.15, ID Control/Status reg (bit 5)
Resync Threshold Exceed Err	Section 4.2.15, ID Control/Status reg (bit 4)
RDGate/SPDet Error	Section 4.2.13, 3rd Configuration reg (bit 3)
ID Miscompare Error	Section 4.2.15, ID Control/Status reg (bit 6)

The following functions do NOT have individual interrupt masks. The only individual control on them is to disable the function itself:

Function	Function Enable
Flag Field/WRTGate Error	Section 4.2.1, Primary Configuration (bit 7)
Psuedo SPDet/WRTGate Error	Section 4.2.13, 3rd Configuration reg (bit 0)
Read Stop Interrupt	Section 4.2.16, Sector per Track reg (bit 7)

4.2.2 Software Reset : Address X'1'

Operation Error Status : Address X'1'

write :

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

The following status is reset when writing to this loaction.

1) Flag Detect Error Flag
2) Read Complete Flag
3) Psuedo Sector Mark Error Flag
4) Resync Threshold Error Flag
5) Missing Resync Error Flag
6) RDGATE/SPDET Error Flag
7) ID Miscompare Error Flag
8) Read Stop Error Flag

X = not applicable

read :

7	6	5	4	3	2	1	0
IV	RDC	FLE	SE	IP	TE	RS	RD

IV = Invalid RLL Code Detected

RDC = Read Complete
Active State = '1'
This bit is set when a data field read operation has just finished. This bit is cleared at the end of each sector. It is also clear if the programmer writes to address '1'. An interrupt is also generated if enabled and Bit 5 of the ID Control/Status Register is set.

FLE = Flag Detect Error
Active State = '1'
This bit is set if the flag detection logic has been enabled, a flag has been detected, and WRTGATE has been raised. An interrupt is also generated if bit 0 of the Primary Configuration Register is set. This bit is cleared if the programmer writes to address '1'.

SE = Psuedo Sector Mark Error
Active State = '1'
This bit is set when a Sector Mark was not detected for this sector, a psuedo SPDET was generated, and WRTGATE is active during that sector. An interrupt is also generated if bit 0 of the Third Configuration Register is set. This bit is cleared when the programmer writes to address '1'.

IP = Interrupt is pending
Active State = '1'

TE = Resync threshold exceeded
Active State = '1'
The defined number of missing resyncs as defined in the Resync Error Threshold Register has been equaled or exceeded in a single sector data field read. An interrupt is generated if enabled and bit 4 of the ID Control /Status Register bit is set. This bit is cleared when the programmer writes to address '1'.

RS = Missing RESYNC field detected
Active State = '1'
At least one Resync byte was missed. This bit is cleared when the the programmer writes to address '1'.

RD = RDGATE/SPDET Error
Active State = '1'
Read Gate was active when SPDET became active. This error also generates an interrupt if enabled, Third Configuration Register bit 3.

The following status flags are cleared whenever this location is read.

- *IV - Invalid RLL code detected*
- *RDC - Read Complete Interrupt*
- *FLE - Flag error interrupt*
- *SE - Psuedo Sector Mark Error*
- *TE - Resync Threshold Exceeded*
- *RS - Missing Resync field detected*
- *RD - RDGATE/SPDET Error*
- *IP - Interrupt Pending*

After being reset. These status flags are reinitialize.

4.2.3 Resync MSB Byte : Address X'2'

write/read :

7	6	5	4	3	2	1	0	
D15	D14	D13	D12	D11	D10	D9	D8	MSB byte

This register stores the RESYNC MSB value. On write data operations this value is injected into the encoded NRZI bit stream. During read operations, this value is used for the detection of the RESYNC mark within the RLL bit stream.

4.2.4 Resync LSB Byte : address X'3'

write/read :

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	LSB byte

This register stores the RESYNC LSB value. On write data operations this value is injected into the encoded NRZI bit stream. During read operations, this value is used for the detection of the RESYNC mark within the RLL bit stream.

4.2.5 ID Address Mark MSB byte : address x'4'

write/read :

7	6	5	4	3	2	1	0	
D15	D14	D13	D12	D11	D10	D9	D8	MSB byte

The user programs the IDAM MSB by writing to this register.

4.2.6 ID Address Mark LSB byte : address x'5'

write/read :

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	LSB byte

The user programs the IDAM LSB by writing to this register.

4.2.7 Data Sync Bytes (6) : Address X'6'

write :

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	data bytes

The microprocessor must write 6 bytes to fully program the data sync field value. The first byte must be the LSB. After each write to this location a counter is incremented. The counter value can be viewed by reading this location. It is important to maintain 2FRCLKs during the writing of this register. The 2FRCLKs should maintain the minimum pulse widths as defined in section 5.

read :

7	6	5	4	3	2	1	0	
RSE	FID1	FID0	PID1	PID0	C4	C2	C1	data bytes

RSE = Read Stop Interrupt
This bit is set when at the next SPDET. RDGATE is also blocked to the internal device. DLYRDGT is also blocked to the drive electronics.

FID1-0 = Future ID Pointer
This counter is incremented whenever the user reads the Data Sync Pointer/Future ID (address = X'9'). The next expected Track high, Track low, and Sector bytes must be read serially from this location. These bits are reset when the programmer writes to this location (addr = X'9').

PID1-0 = Present ID Pointer
This counter is incremented whenever the user reads the ID Compare Preset Register (addr = X'D'). The pointer is reset when the programmer writes to the location (addr = X'9').

C2-0 = Data Sync Counter

Number of bytes written to Data Sync register. This value is reset on soft reset (addr = '9').

4.2.8 Sync Threshold/TOF Size : Address X'7'

write/read :

7	6	5	4	3	2	1	0
T3	T2	T1	T0	M3	M2	M1	M0

T3-T0 : TOF Window size (increment = one 2FRCLK)

M3-M0 : Sync Field Majority vote Trigger point
(Value range = 0 -> 12 base 10)
The user set the percentage of the Sync Mark that must be found before an AMDET is generated in the Data field. Each incremental value changes the correlation percentage by 8.33 %.

4.2.9 RESYNC Error Threshold/Data Segment Size : Address X'8'

write/read :

7	6	5	4	3	2	1	0
DS16	DS8	DS4	DS2	DS1	TD4	TD2	TD1

DS16-DS1 = Data Segment length
Value Range = 0 - 31 base 10
This field sets the quantity of data bytes between RESYNCs within the data field. (The present formats define this field to be 14_{10} or 19_{10}.
(DS16-DS1 = # of byte between resyncs - 1)

TD4 -TD1 = Resync Error Threshold
Value range = 1 - 7 base 10
This field sets the quantity of RESYNCS that aren't detected within a single sector. When this value is reached or exceeded, the RESYNC error flag in the Status register is set.

4.2.10 Data Sync Pointer Reset / ID Read Status : Address X'9'

write :

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

X = irrelevant

Writing to this address location resets all internal pointers which are used for multiple write operation. The pointers that are effected are the 1) Data Sync Write Pointer, 2) Present ID write/read pointers, and 3) Future ID read pointer. The Data Sync Pointer selects which register is to be written when writing to location '06'. The Present ID write/read pointers are two independent counter which steer the location of the initial ID compare values. The Future ID read pointer identifies which byte of the expected

ID counter is being read. The 2FRCLK should be operating at this time.

read :

7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0

If the auto-increment functions are enabled, the WD60C31B can perform ID compare operations for ID field bytes other than the original bytes. the user can read the internal counter which predicts the next ID field to be verified. To read all three bytes, Sector byte, Track low byte, and track high, the user must perform repeated reads of this location. The byte that is will be read is identified in the Data Sync Status register (addr = X'9'.

4.2.11 Phase Lock Delay : Address X'A'

write/read :

7	6	5	4	3	2	1	0
FS	IDS	P5	P4	P3	P2	P1	P0

FS = Flag Window Select
This bit defines the placement of the internal flag window for flag field detection. The flag window, nominally 6 bytes, is placed with reference to the last ID read. This bit is "0" if the last ID read is predicted to be ID number 3. This bit is "1" if the last ID read is predicted to be ID number 2. During the ID read operation, the ADS10C00 should generate an AMENA during the last byte of the last ID that is read, normally the second CRC byte. Generally, the AMENA should not be generated unless the ID field passes a bit for bit comparision. The WD60C31 then delays the appropriate number of byte times and opens the flag window.

IDS = ID Window Enable
Active State = '1'
When active, the detection of the ID Address Marks with be limited to three small windows, +/- 8 2FRCLKs. This reduces the probability of false ID AM detection.

P5-P0 = Programmble Phase Lock delay from DLYRGT
Value Range = 0 - 63
The user can set the time difference betweeen the Delayed Read Gate and the PHASELK output signal.

4.2.12 Secondary Configuration : Address X'B'

write/read :

7	6	5	4	3	2	1	0
FMT	SE35	IDW	XX	RGH	SP0	RS1	RS0

FMT = Format Enable
Active State = 1
When active the WD60C31B is set in a format track mode when the WRTGATE is received. Refer to Section 2.2.2.3 for more details.

SE35 = Media Select (3.5 inch)
Active State = 1
When active the WD60C31B sets the internal operation for the 3.5 inch ANSI continuous composite format sector sizes.

IDW = Disable Internal ID and Data Window Generator
Active State = 1
Normally, the WD60C31B generates internal window for predicting the location of the ID and Data fields. When this bit is active the internal window generator for ID and Data is defeated. Instead the WD60C31B relies on an external signal,SEQOUT, from the ADS10C00. SEQOUT along with RDGATE selects the type of field the WD60C31B is expecting to be reading. (The default sector size is 746 and 1360 bytes). A typical situation is as follows. The ADS10C00 first waits for a SPDET. The ADS10C00 raises read gate. The WD60C31B goes in search of an address mark. The WD60C31B then send the ID field to the ADS10C00. When the ADS10C00 finds the appropriate number of IDs, read gate is dropped. SEQOUT is set to the WD60C31B to identify the next read operation as a search for a data sync mark. This feature is primarily used with soft sectored media.

RGH = Read Gate Hold
Active State = 1
When active, the DLYRGT signal is extended to the read channel by 9 RRCLKs. This occurs only if READGATE is raised and lowered in the ID field. This is useful when maintaining the PLL phase mode between consecutive ID fields. The Read Gate signal from the ADS10C00 must be dropped after each ID field.

SP0 = Speed tolerance Selection (5.25 inch only)
The programmer sets the expected spindle motor tolerance. This tolerance changes sector mark detection windows. When bit = '0', the sector mark window is set for a .5 % speed tolerance. When bit = '1', the window is set to a 1 % speed tolerance.

RS1-RS0 = Resync Window Selection

RS1	RS0	Mode
0	0	Fixed Window - 12 clks (.5% speed tolerance)
0	1	Fixed Window - 18 clks (1% speed tolerance)
1	0	Progressive Windows The resync window is intially set to a minimum value (6 2FRCLKs). If a resync is not found, the resync window is increased by 4 clocks for each resync that is not found.
1	1	Progressive Windows The resync window is intially set to a minimum value (8 2FRCLKs) Window increases by 8 clocks for each resync that is not found. Max Window = 24 clocks

4.2.13 Third Configuration : Address X'C'

write/read :

7	6	5	4	3	2	1	0
ID1	ID0	SMS	T4	RDI	DC1	DC0	SME

ID1,0 = ID Status Select Bits

These bits select which status byte of 4 possible bytes to be read from addr 'E'.

ID1	ID0	
0	0	Control Register
0	1	ID Error Status
1	0	Present ID / Data Sync Read
1	1	Reserved

SMS = Small SYNCDET Enable
Active State = '1'
This bit when enabled reduces the size of the SYNCDET to one NRZI bit. Normally the SYNCDET signal is set during bit 1 of the Address mark byte and remains set until RDGATE is dropped. IF this mode is enable the SYNCDET is only a pulse. During the reading of the ID fields, the READGATE can remain on over all the ID fields. The SYNCDET will be raised for each ID Address Mark that is found. However, in both cases, READGATE must be dropped before the reading of the data field is attempted.

T4 = TOFWIN Window Size MSB
Active State = '1'
This bit is used in conjunction with T3-T0 of the Sync Threshold/Size register. This bit extends the size of TOFWIN byte for 0 to 31 2FRCLKs. This is the MSb of the count value.

RDI = Read Gate/SPDET interrupt Mask
Active State = '1'
When this bit is set, an interrupt is generated if Read gate is active when the SPDET is sent.

DC1,0 = Data Segment Transfer Count (used in Mode 2 and 3 operations)
If a Data Sync is not detected given a minimum threshold, the programmer can select to use a RESYNC as the synchronization mark for the data field. DC1 and DC0 define the quantity of data segments that are sent to the ADS10C00 before the RESYNC detection logic is enabled. A data segment is the quantity of data bytes between RESYNC marks as defined in the RSYNC Error Threshold/Data Segment Size Register, address X'8'.

DC1	DC0	Data Segments
0	0	1
0	1	2
1	0	3
1	1	4

SME = Psuedo Sector Mark Error Enable
Active State = '1'
When active, a psuedo sector mark error flag is set and an interrupt is generated (if bit 4 of the Primary Configuration is set). This error occurs if a sector mark is not detected, an SMDET is generated due to a timeout, and a write operation is attempted. In addition, the DLYWGT signal is disabled to the drive.

4.2.14 ID Compare Preset Register : Address X'D'

write/read:

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

The microprocessor must load the ID field: Sector byte, Track Low byte, Track high byte, which is used during the ID "on the fly" comparision. The Sector byte must be loaded first, then track low byte, track high byte. The contents of these values must be performed used repeated reads of this location. The ID status register, addr 'E', contains a value which states which value is being read.

4.2.15 ID Control/Status Register : Address X'E'

write:

7	6	5	4	3	2	1	0
3ID	IDE	RCM	REM	TAE	SAE	IT1	IT0

3ID = 3 ID Enable
Active State = '1'
When this bit is set, the special 3 ID "on the fly" mode is enabled. In this mode, the WD60C31B will read the IDs for the ADS10C00 and inform the ADS10C00 of its conclusion.

IDE = ID Error Interrupt Enable
Active State ='1'
When this bit is set, an interrupt is generated whenever the ID compare is completed and an error was detected.

RCM = Read Complete Interrupt Mask
Active State = '1'
When this bit is set, an interrupt is generated whenever the end of a data field read operation is reached.

REM = Resync Threshold Error Interrupt Mask
Active State = '1'
When this bit is set, an interrupt is generated whenever the RESYNC error counter is reached.

TAE = Track Auto-Increment Enable
Active State ='1'
When this bit is active the track high and low bytes can be incremented whenever the maximum sector is detected and the last ID comparison was good.

SAE = Sector Auto-increment Enable
Active State ='1'
When this bit is active, the expected sector value can be incremented after a good ID comparision.

IT1,0 = ID Compare Threshold Bits
These bits define the quantity of good ID field(s) which must be detected before the WD60C31B flags the ADS10C00 of a good operation. IT1 is the MSb.

IT1	IT0	Good IDs Detected
0	0	not valid
0	1	1
1	0	2
1	1	3

Read:

This address location can contain three possible status bytes. The third configuration register, ID1(bits 7) and ID0(bit 6), select what status is read.

Control Register (ID1 = 0, ID0 = 0)

7	6	5	4	3	2	1	0
3ID	IDE	RCM	REM	TAE	SAE	IT1	IT0

ID Compare Error Status (ID1 = 0, ID0 = 1)

7	6	5	4	3	2	1	0
SP	C3	C2	C1	I3	I2	I1	ICE

SP = Psuedo Sector Mark Detect
Active State = '1'
When active, no sector mark was detected within the internal sector mark window. A psuedo SPDET was generated. This bit is cleared when a real sector mark is detected.

C3-C1 = ID CRC Error

These bits identify which met the following conditions; ID AM was detected, ID track and sector bytes compared, but a CRC fault occurred. C3 is status for the third ID. C2 is the second's ID status. This status is only valid if its corresponding ID was detected.

I3-I1 = ID AM and ID field Match

These status bits are active whenever an ID AM is found and the ID field track and sector bytes match. This status is valid up to the limit set by the ID Threshold limit set in the ID Control Register.

ICE = ID Compare Error
Active State ='1'

This bit is set whenever the ID Threshold as set by the Control Register is not met by the end of the ID zone. An interrupt can also be generated if enabled in the ID Control Register.

Present ID / Data Sync Status (ID1 = 1, ID0 = 0)

7	6	5	4	3	2	1	0
DS3	*DS2*	*DS1*	*DS0*	*PIR1*	*PIR0*	*DR*	*XX*

DS3-0 = Reserved

DR = Data RDGATE / SPDET Error
Active State = '1'
When this bit is active. RDGATE was active when SPDET was generated. RDGATE was active due to an extended data field read operation. This bit is cleared when writing to address '1'.

PIR1.0 = Reserved

4.2.16 Sector per Track : Address X'F'

write/read:

7	6	5	4	3	2	1	0
RSP	SC6	SC5	SC4	SC3	SC2	SC1	SC0

RSP = Read Stop Enable
Active State = '1'

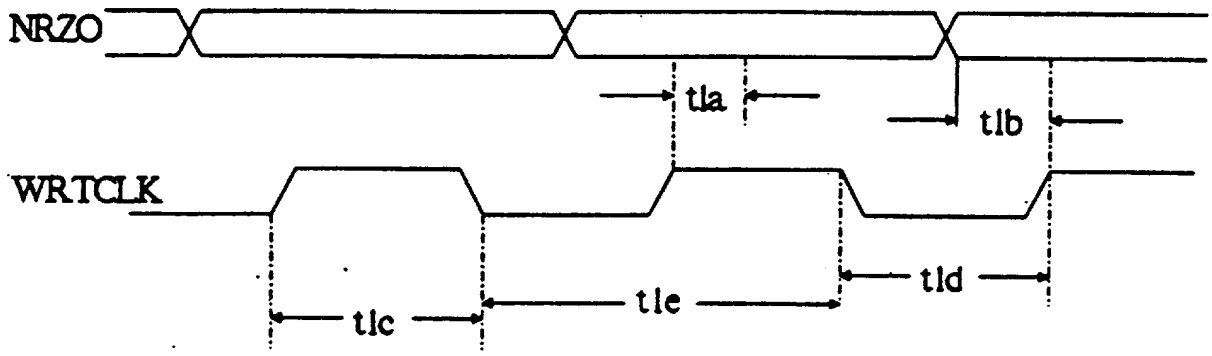
SC6-SC0 = Sector per Track

The user defines the quantity of sector per track. This register is important whenever the auto-increment function is enabled in the ID Control-register. Whenever the predicted ID field matches the maximum sectors per track, the end of the ID field is reached, and the ID Threshold has been met or excessed , the internal sector counter sets the sector byte to zero.

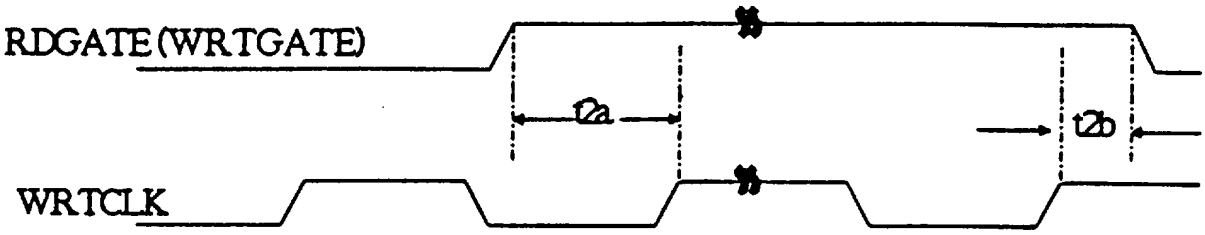
5 CRITICAL TIMING

5.1 Disc Controller Timing

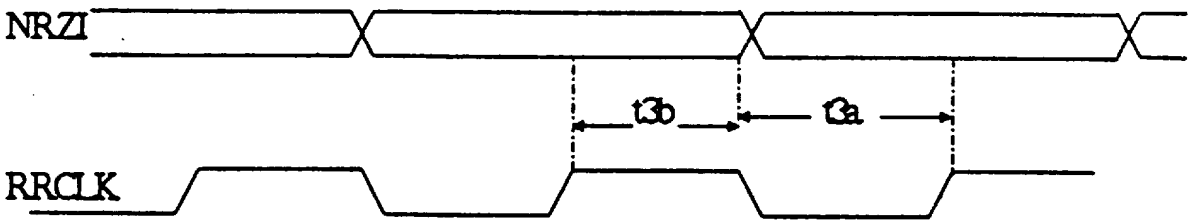
5.1.1 NRZO to WRTCLK Timing



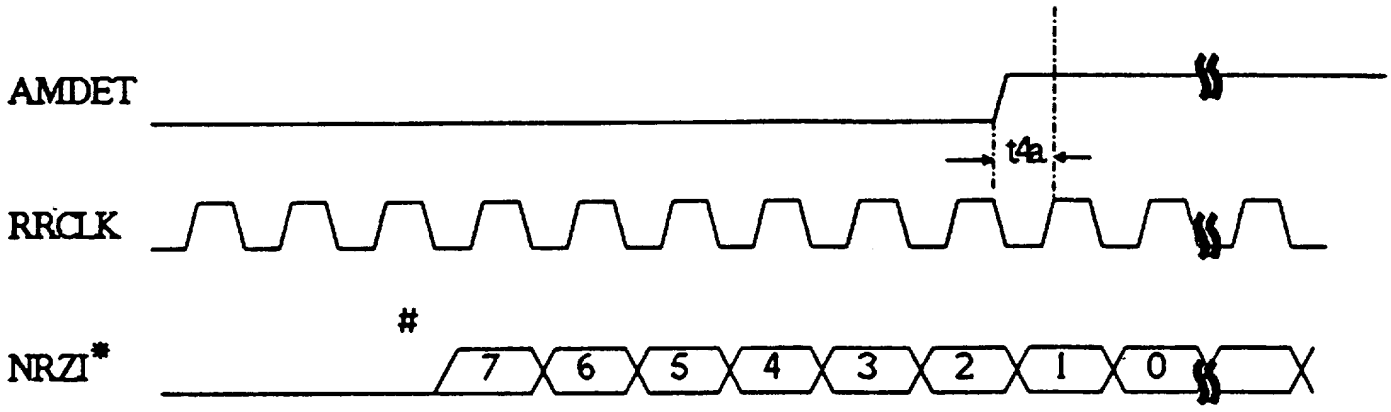
5.1.2 WRTGATE / RDGATE Timing



5.1.3 NRZI to RRCLK Timing



.4 SYNCDET Timing



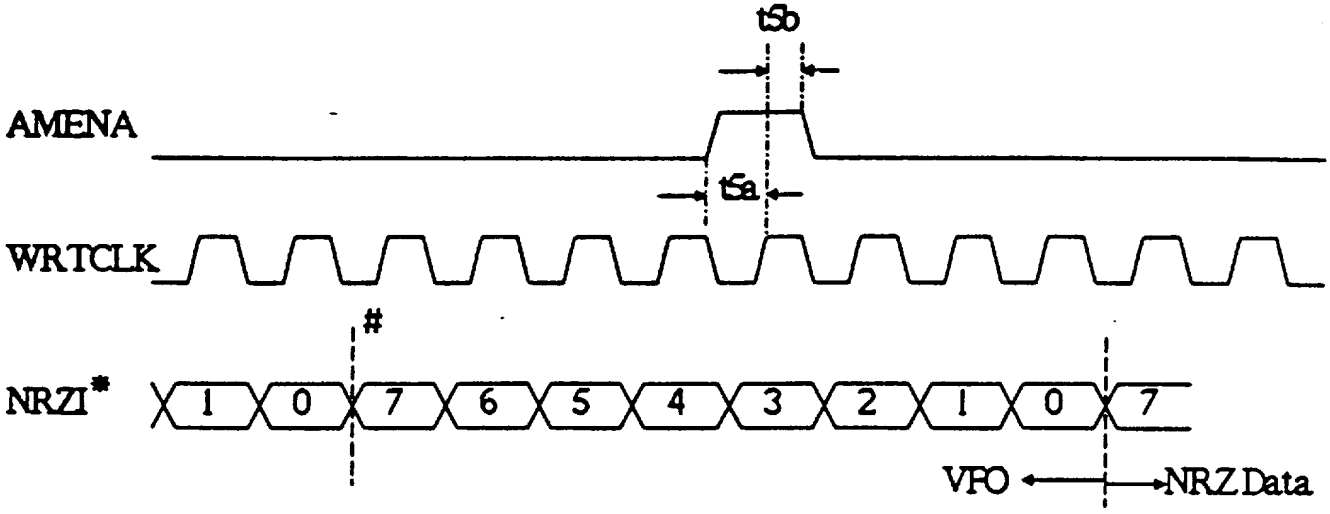
* = number indicates the data bit position within a byte
bit 7 is the most significant bit

\# = byte of zeros is sent before SYNCDET if ID address mark detection

Note:

SYNCDET is generated whenever RDGATE is active and either the ID Address Mark or Data Address Mark is detected. Whenever an ID Address Mark is detected the SYNCDET is sent concurrently with the first byte of the five byte ID Address field. The five byte ID field is preceded by a NRZI byte of zeroes. During ID search the SYNCDET is sent concurrently with this byte of zeroes. Whenever a Data Address Mark is detected the SYNCDET is sent one before the first byte of the data field. A full byte of zeros is sent concurrently with the SYNCDET. This byte of zeros is handled in the ADS10C00 as an address mark. SYNCDET, once active, remains active until Read gate is dropped.

5.1.5 AMENA Timing



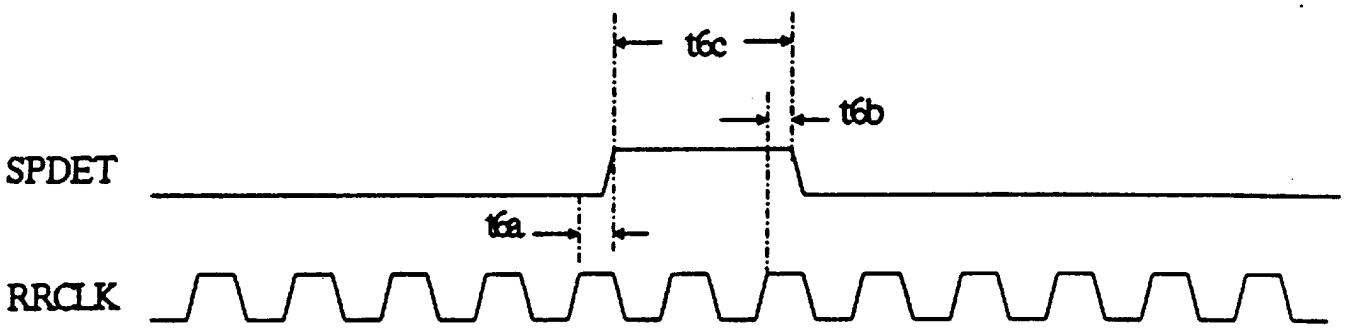
* = number indicates the data bit position within a byte
bit 7 is the most significant bit

\# = last 'dummy' VFO byte

Note:

The data field of an optical drive contains primarily four unique types of information. They are : 1) the VFO field, 2) the Data Address Mark, 3) the encoded user data, and 4) the Resync Marks. The ADS10C00 and the WD60C31A share the responsiblity of defining the type and quantity of information to be written on the media. In the cause of the VFO field, the ADS10C00 specifies the size of the VFO field and the WD60C31A creates the unique high frequency pattern. First, the ADS10C00 raises WRTGATE. Then an all ones NRZ data pattern is sent to the WD60C31A. This specifies the beginning of the VFO field. The WD60C31A writes a fixed RLL pattern, 100100, on the disc. The ADS10C00 must indicate the end of the VFO field. This is performed by sending the AMENA signal during the last byte. This signal then initiates the writing of the previously programmed Data Address Mark (3 Bytes). The WD60C31A then encodes the incoming NRZ data from the ADS10C00. The WD60C31A then injects the Data Resync Mark, another previously programmed pattern, into the encoded write data path. This operation continues for as long as WRTGATE is active or the end of sector is detected.

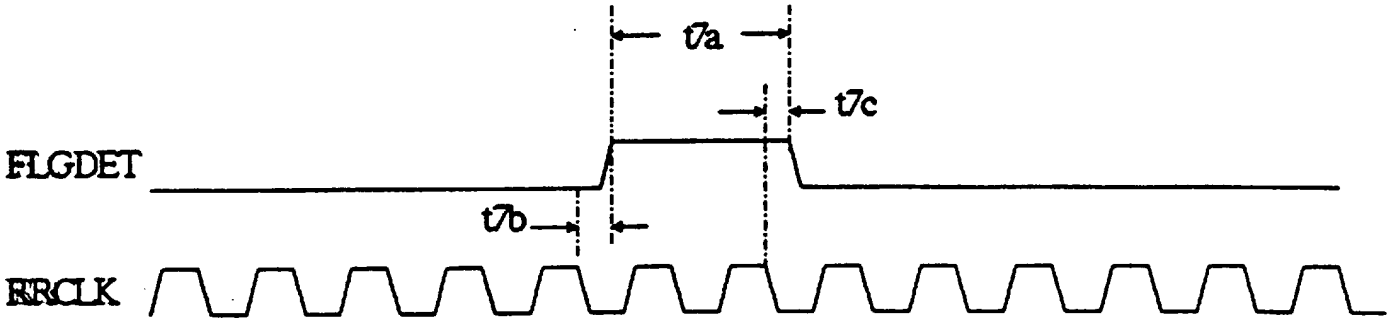
5.1.6 SPDET Timing



Note :

The SPDET signal is sent whenever a sector mark is detected. An SPDET is also sent whenever a sector mark has not been detected by a defined time.

5.1.7 FLGDET Timing

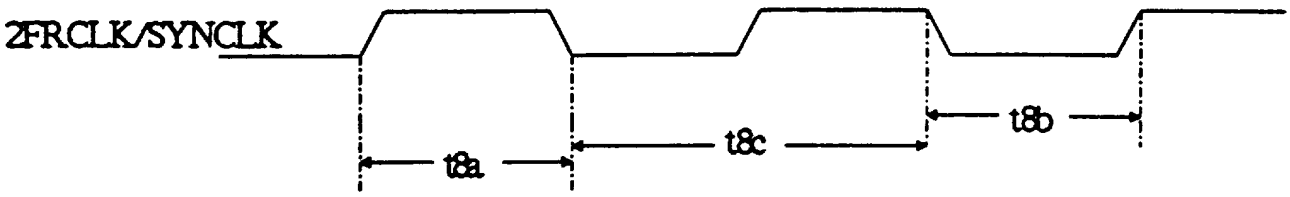


Note:

A FLGDET pulse is generated if FLGEN is active and one and a half bytes of the Flag pattern (high frequency '100') is detected.

5.2 PLL Timing

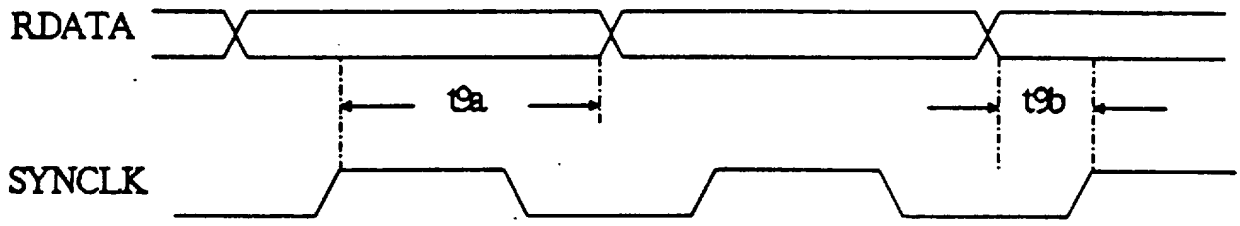
5.2.1 2FRCLK / SYNCLK Timing



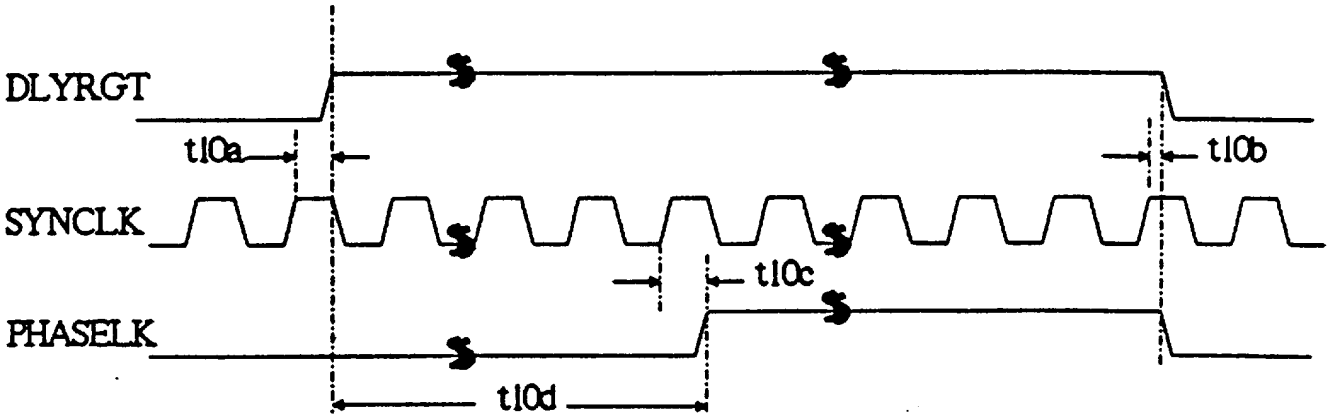
Note:

Both clocks must be glitch free. The PLL must deliver a clock which does not violate the above timing. The is especially true of the SYNCLK which changes between the reference clock and the internally generated PLL clock when read gate is applied.

5.2.2 NRZI to RRCLK Timing



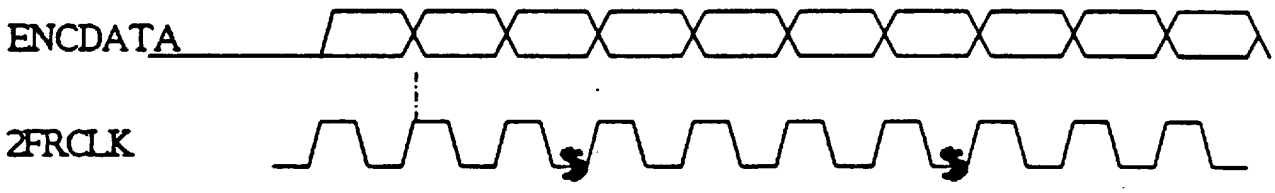
5.2.3 DLYRGT / PHASELK Timing



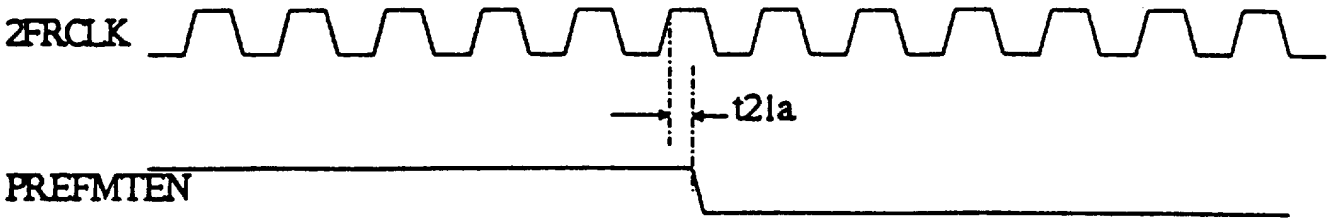
Note:

The PHASELK signal is intended for controlling the PLL modes. Whenever PHASELK is low the PLL should be in high gain (or phase/frequency mode). Whenever PHASELK is high, the PLL should be in low gain (or phase mode). There is a delay of 1 to 64 2FRCLKs(+/-1 2FRCLK) from DLYRGT to PHASELK.

5.2.4 ENCDATA Output Timing



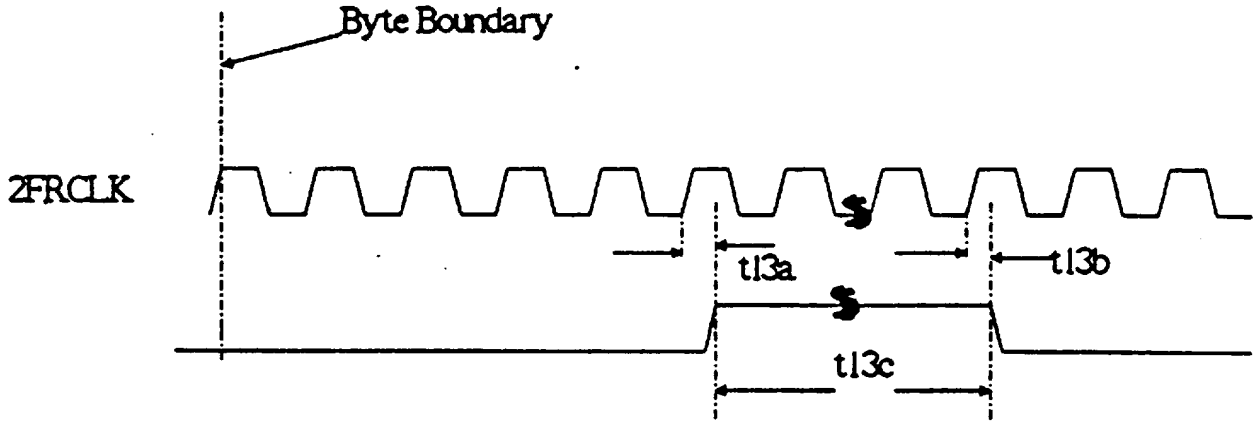
5.2.5 PREFMTEN Timing



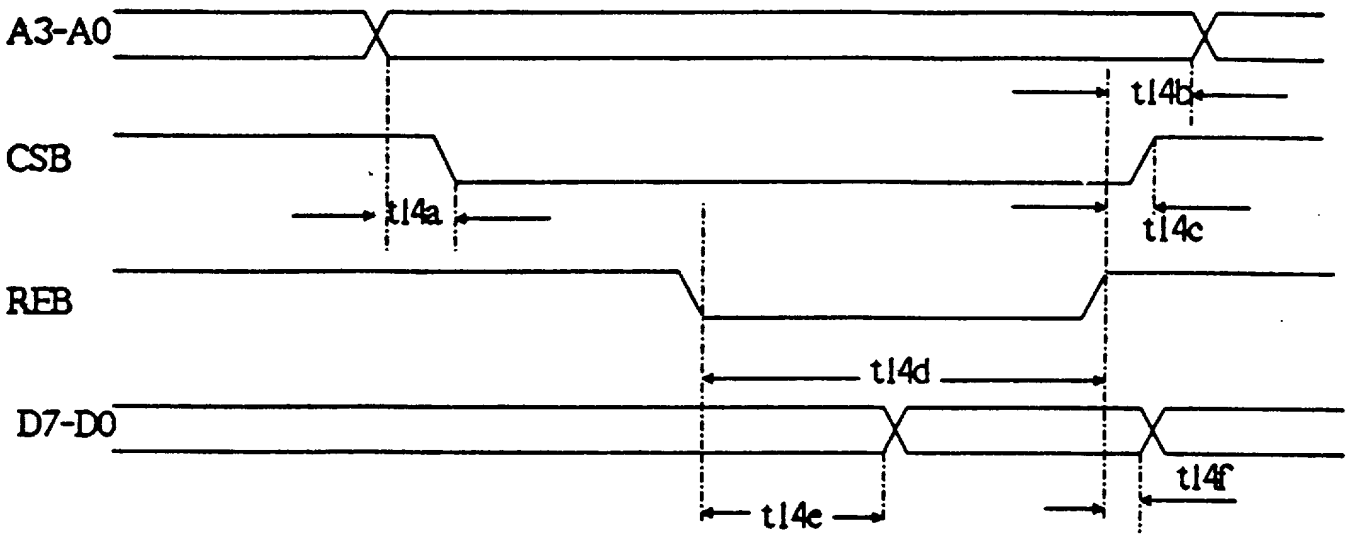
Note :

The PREFMTEN signal is intended for use as a read channel control line. This signal is whenever the drive is expecting to read the preformatted data (ID fields) . This signal is continuosly high for WORM drive applications. This output is enabled when the set the configuration register. This signal when enabled is low 47 bytes from SPDET.

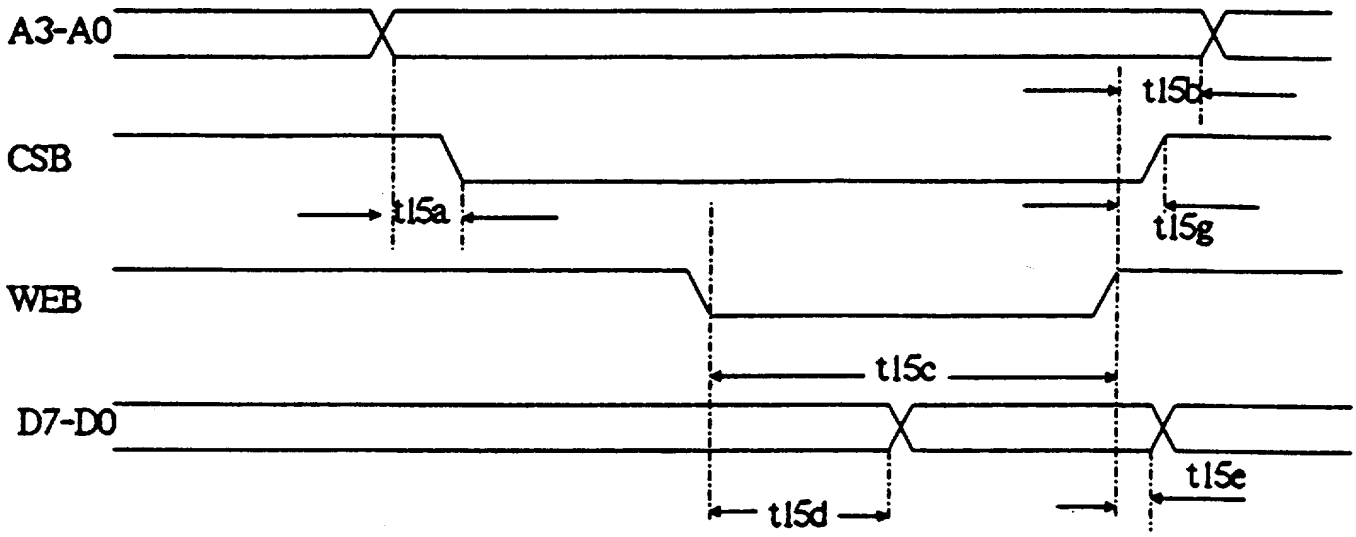
5.2.6 TOFWIN Timing



5.3.1 Microprocessor Read Timing



5.3.2 Microprocessor Write Timing



Timing	Description	BIN 03		BIN 04	
		MIN	MAX	MIN	MAX
tla	NRZO setup	10		13	
tlb	NRZO hold	10		10	
tlc	WRTCLK high	trlo-4.5		trlo-4.5	
tld	WRTCLK low	trhi-4.5		trhi-4.5	
tle	WRTCLK period	trp-4.5		trp-4.5	
t2a	WRTGTE/RDGTE	10		13	
t2b	WTGTE/RDGTE hold	10		10	
t3a	NRZI setup	trhi-4.5		trhi-4.5	
t3b	NRZI hold	trlo-4.5		trlo-4.5	
t4a	SYNCDET setup	trlo-4.5		trlo-4.5	
t4b	SYNCDET hold	trhi-4.5		trhi-4.5	
t5a	AMENA setup	10		10	
t5b	AMENA hold	10		10	
t6a	SPDET pulse width	2trp-4.5		2trp-4.5	
t6b	SPDET high delay	10		10	
t6c	SPDET low delay	10		10	
t7a	FLGDET pulse width	4trp-4.5		4trp-4.5	
t7b	FLGDET setup	trlo-4.5		trlo-4.5	
t7c	FLGDET hold	trhi-4.5		trhi-4.5	
t8a	Clock high	13		10[a]	
t8b	Clock low	13		10[a]	
t8c	Clock Period	tclk		tclk	
t9a	RDATA setup	7		9[b]	
t9b	RDATA hold	7		9[b]	
t10a	DLYRGT low delay	12	40	12	40
t10b	DLYRGT high delay	12	40	12	40
t10c	TBD	TBD	TBD	TBD	TBD
t10d	TBD	TBD		TBD	
t11a	ENCDATA low delay	12	20	12	20
t11b	ENCDATA high delay	12	20	12	20
t12a	TBD	TBD	TBD	TBD	TBD
t13a	TBD	TBD	TBD	TBD	TBD
t13b	TBD	TBD	TBD	TBD	TBD
t13c	TBD	(0-15)2FRCLK		(0-15)2FRCLK	

trhi = clock high for RRCLK output
trlo = clock low for RRCLK output
trp = clock period for RRCLK output
tclk = 2FRCLK clock input
[a] = Bin 04 guaranteed for t8a, t8b = 9ns but will be tested at 10ns
[b] = Bin 04 guaranteed for t9a, t9b = 7ns but will be tested at 9ns.

TABLE 5.1 DISC CONTROLLER AND PLL TIMING

PARAMETER	DESCRIPTION	MIN	MAX
t14a	Address valid to REB	20	
t14b	REB high to Addr. Change	0	
t14c	REB false to CSB false	0	
t14d	REB Pulse Width	100	
t14e	REB true to data valid		80
t14f	REB false to data hold	10	
t15a	Addr Valid to WEB true	20	
t15b	WEB high to Addr Change	0	
t15c	WEB pulse width	100	
t15d	Data setup to WEB false	80	
t15e	WEB false to Data hold	00	
t15f	WEB false output change		80
t15g	WEB false to CSB false	10	

TABLE 5.2 MICROPROCESSOR TIMING

SECTION 6 D.C ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS (non-operational)

V_{DD} ..... 7.0 V
Voltage on any pin
with respect to Vss
--- Minimum -.3 v
--- Maximum V_{DD} + .3 V

Storage Temperature ..... -55 to 150 deg C

6.1.1 OPERATING CONDITIONS

V_{DD} ..... 5.0 +/- 0.5 V
I_{DD}(max.) ..... 150 ma @ 30 Mhz
Ambient Temperature ..... 0 to 70 deg C

6.2 CIRCUIT OPERATING CHARACTERISTICS

6.2.1 INPUTS - CIRCUIT A

SYM	PARAM	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Vih	HIGH LEVEL INPUT VOLT	2.0		V_{DD} + 0.3	V	
Vil	LOW LEVEL INPUT VOLTAGE	-0.3		.8	V	
Vi	INPUT CLAMP VOLTAGE(low)	-0.5				
Ilh	LEAKAGE CURR HIGH	-10		+10	uA	2.0 <= Vi <= V_{DD}
Ill	LEAKAGE CURR LOW	-10		+10	uA	0.0 <= Vi <= 0.8
Iluh	LATCHUP CURR HIGH	-40			uA	
Ilul	LATCHUP CURR LOW			40	uA	

Note: Positive current is taken as current flow into the pin.

TABLE 6.1

6.2.2 TRI-STATE OUTPUT - CIRCUIT B

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITION
Ioh	HIGH LEVEL OUTPUT CURRENT			-400	uA	Vo = 2.8 V
Iol	LOW LEVEL OUTPUT CURRENT	2.0			mA	Vo = 0.3 V
Voh	HIGH LEVEL OUTPUT VOLTAGE	2.8			V	Io = -400 uA
Vol	LOW LEVEL OUTPUT VOLTAGE			0.3	V	Io = 2.0 mA
Iozh	OFF STATE OUTPUT CURRENT HIGH LEVEL	-10		+10	uA	2.0 <= Vo <= V_{DD}
Iozl	OFF STATE OUTPUT CURRENT LOW LEVEL	-10		+10	uA	0.0 <= Vo <= 0.8 V

Note: Positive current is taken as current flow into the pin.

TABLE 6.2

6.2.3 BI-DIRECTIONAL - CIRCUIT C

SYM	PARAM	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Ioh	HIGH LEVEL OUTPUT CURRENT			-2.5	mA	Vo = 2.8 V
Iol	LOW LEVEL OUTPUT CURRENT	4.0			mA	Vo = 0.3 V
Vih	HIGH LEVEL INPUT VOLTAGE	2.4		V_{DD} + 0.3	V	
Vil	LOW LEVEL INPUT VOLTAGE	-0.3		0.8	V	
Vik	INPUT CLAMP VOLTAGE (low)			-0.5	V	
Voh	HIGH LEVEL OUTPUT VOLTAGE	2.8			V	Ioh= -2.5 mA
Vol	LOW LEVEL OUTPUT VOLTAGE			0.4	V	Iol= 6.0 ma
Iozh	OFF STATE OUTPUT CURRENT HIGH LEVEL	-10		+10	uA	Vcc=MAX Vo=2.8 V
Iozl	OFF STATE OUTPUT CURRENT LOW LEVEL	-10		+10	uA	Vcc=MAX 0.0 <= Vo <= 0.8
Iluh	LATCHUP CURR. HIGH	-40			mA	
Ilul	LATCHUP CURR. LOW			40	mA	
Iih	HIGH LEVEL INPUT CURRENT	-10		+10	uA	VCC=MAX Vih=2.8V
Iil	LOW LEVEL INPUT CURRENT	-10		+10	uA	VCC=MAX Vil=.4V

Note: Positive current is taken as current flow into the pin.

TABLE 6.3