

MOSEL VITELIC**V53C316540500****3.3 VOLT 16M X 4 EDO PAGE MODE
CMOS DYNAMIC RAM**

V53C316540500	40	50	60
Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC})	40 ns	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	20 ns	25 ns	30 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	16 ns	20 ns	25 ns
Min. Read/Write Cycle Time, (t_{RC})	69 ns	84 ns	104 ns

- 16M x 4-bit organization
- EDO Page Mode for a sustained data rate of 63 MHz
- $\overline{\text{RAS}}$ access time: 40, 50, 60 ns
- Low power dissipation
- Read-Modify-Write, $\overline{\text{RAS}}$ -Only Refresh, CAS-Before- $\overline{\text{RAS}}$ Refresh, Hidden Refresh
- Self Refresh (L-version only)
- Refresh Interval: 4096 cycles/64 ms
- Available in 32-pin 400 mil SOJ, and 32-pin 400 mil TSOP-II
- Single +3.3 V ± 0.3 V Power Supply
- TTL Interface

Description

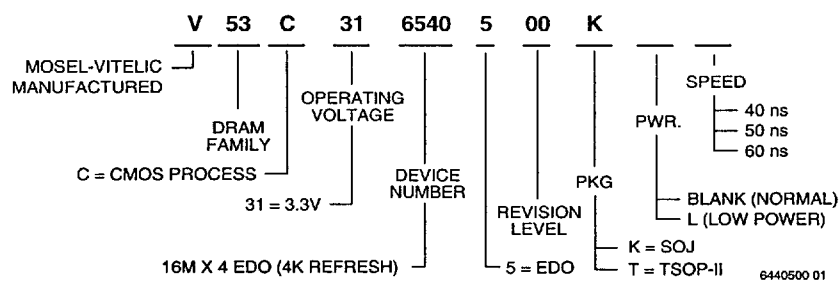
The V53C316540500 is a 16,777,216 x 4 bit high-performance CMOS dynamic random access memory. The V53C316540500 offers Page mode operation with Extended Data Output. The V53C316540500 has an symmetric address, 12-bit row and 12-bit column.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 4096 x 4 bits, within a page, with cycle times as short as 16 ns.

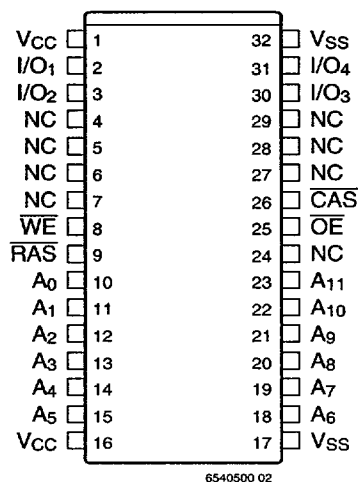
These features make the V53C316540500 ideally suited for a wide variety of high performance computer systems and peripheral applications.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	K	T	40	50	60	Std.	L	
0°C to 70 °C	•	•	•	•	•	•	•	Blank



32 Pin Plastic SOJ /TSOP-II
PIN CONFIGURATION
Top View



Description	Pkg.	Pin Count
SOJ	K	32
TSOP-II	T	32

Pin Names

A ₀ -A ₁₁	Row, Column Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
I/O ₁ -I/O ₄	Data Input, Output
V _{CC}	+3.3V Supply
V _{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Operating temperature range 0 to 70 °C
 Storage temperature range -55 to 150 °C
 Soldering temperature 260 °C
 Soldering time 10 s
 Input/output voltage -0.5 to min ($V_{CC}+0.5$, 4.6) V
 Power supply voltage -0.5V to 4.6 V
 Power dissipation 1.0 W
 Data out current (short circuit) 50 mA

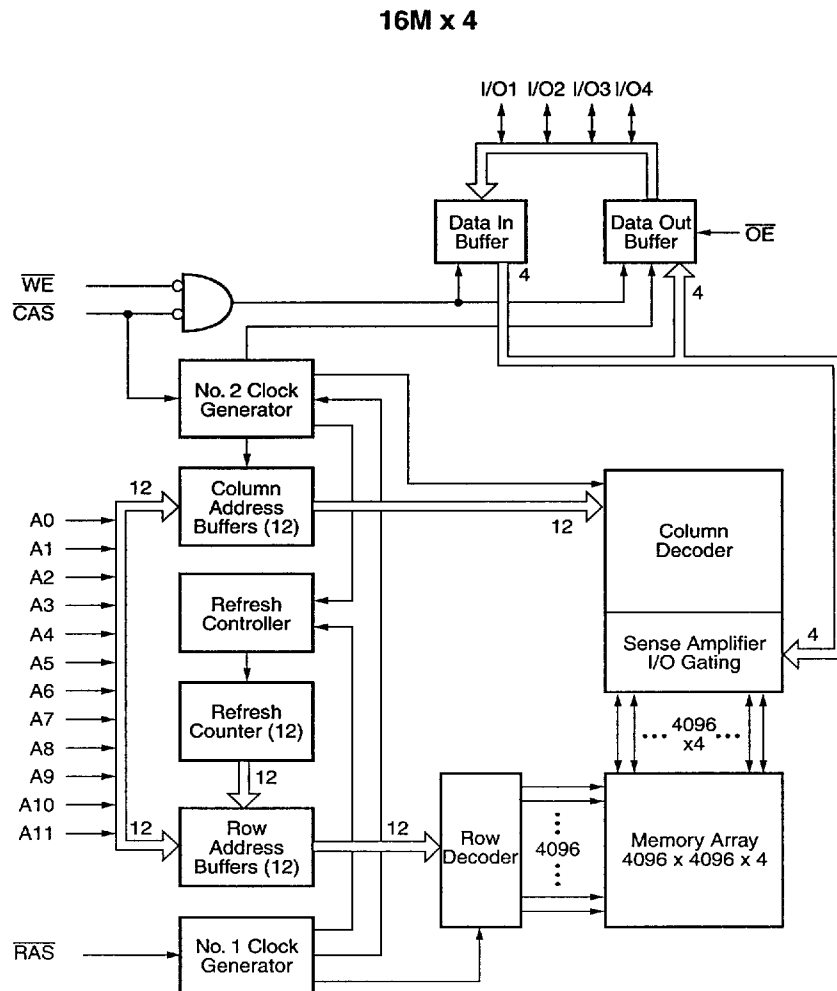
*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

$T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $f = 1\text{ Mhz}$

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Address Input	—	5	pF
C_{IN2}	RAS, CAS, WE, OE	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

*Note: Capacitance is sampled and not 100% tested.

Block Diagram

DC and Operating Characteristics^(1, 2)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, unless otherwise specified.

Symbol	Parameter	Access Time	V53C316540500			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		-2		2	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		-2		2	μA	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	40			170	mA	$t_{RC} = t_{RC}(\text{min.})$	2, 3, 4
		50			140			
		60			115			
I_{CC2}	V_{CC} Supply Current, TTL Standby				1	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at V_{IH} other inputs $\geq V_{SS}$	
I_{CC3}	V_{CC} Supply Current, $\overline{\text{RAS}}$ -Only Refresh	40			170	mA	$t_{RC} = t_{RC}(\text{min.})$	2, 4
		50			140			
		60			115			
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	40			140	mA	Minimum Cycle	2, 3, 4
		50			105			
		60			85			
I_{CC5}	V_{CC} Supply Current, CMOS Standby				500	μA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$	
I_{CC5}	V_{CC} Supply Current, CMOS Standby (L-Version)				100	μA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$	
I_{CC6}	Average Self Refresh Current CBR cycle with $t_{RAS} > t_{RAS} \text{ min.}$, (L-version) $\overline{\text{CAS}}$ held low, $\overline{\text{WE}} =$ $V_{CC} - 0.2\text{ V}$, Address and $D_{IN} = V_{CC} - 0.2\text{ V}$ or 0.2 V				400	μA		
I_{CC7}	V_{CC} Supply Current, during $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh	40			170	mA		2, 4
		50			140			
		60			115			
V_{IL}	Input Low Voltage		-0.3		0.8	V		1
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.3$	V		1
V_{OL}	Output Low Voltage				0.4	V	$I_{OL} = 2\text{ mA}$	1
V_{OH}	Output High Voltage		2.4			V	$I_{OH} = -2\text{ mA}$	1

TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ROW ADDR	COL ADDR	I/O1-I/O4
Standby		H	H $\rightarrow$ X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Delayed-Write		L	L	H $\rightarrow$ L	H	ROW	COL	Data In
Read-Modify-Write		L	L	H $\rightarrow$ L	L $\rightarrow$ H	ROW	COL	Data Out, Data In
EDO Page Mode Read	1st Cycle	L	H $\rightarrow$ L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H $\rightarrow$ L	H	L	N/A	COL	Data Out
EDO Page Mode Write	1st Cycle	L	H $\rightarrow$ L	L	X	ROW	COL	Data In
	2nd Cycle	L	H $\rightarrow$ L	L	X	N/A	COL	Data In
EDO Page Mode RMW	1st Cycle	L	H $\rightarrow$ L	H $\rightarrow$ L	L $\rightarrow$ H	ROW	COL	Data Out, Data In
	2nd Cycle	L	H $\rightarrow$ L	H $\rightarrow$ L	L $\rightarrow$ H	N/A	COL	Data Out, Data In
RAS only refresh		L	H	X	X	ROW	N/A	High Impedance
CAS-before-RAS refresh		H $\rightarrow$ L	L	H	X	X	N/A	High Impedance
Test Mode Entry		H $\rightarrow$ L	L	L	X	X	N/A	High Impedance
Hidden Refresh	READ	L $\rightarrow$ H $\rightarrow$ L	L	H	L	ROW	COL	Data Out
	WRITE	L $\rightarrow$ H $\rightarrow$ L	L	L	X	ROW	COL	Data In
Self Refresh (L-version only)		H $\rightarrow$ L	L	H	X	X	X	High Impedance

AC Characteristics (5,6) $T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3\text{V}$, $t_T = 2 \text{ ns}$

#	Symbol	Parameter	-40		- 50		- 60		Unit	Note
			min.	max.	min.	max.	min.	max.		
	Common Parameters									
1	t _{RC}	Random read or write cycle time	69	—	84	—	104	—	ns	
2	t _{RAS}	RAS pulse width	40	100k	50	100k	60	100k	ns	
3	t _{CAS}	CAS pulse width	6	10k	8	10k	10	10k	ns	
4	t _{RP}	RAS precharge time	25	—	30	—	40	—	ns	
5	t _{CP}	CAS precharge time	6	—	8	—	10	—	ns	
6	t _{ASR}	Row address setup time	0	—	0	—	0	—	ns	
7	t _{RAH}	Row address hold time	5	—	7	—	10	—	ns	
8	t _{ASC}	Column address setup time	0	—	0	—	0	—	ns	
9	t _{CAH}	Column address hold time	5	—	7	—	10	—	ns	
10	t _{RCD}	RAS to CAS delay time	9	30	11	37	14	45	ns	
11	t _{RAD}	RAS to column address delay time	7	20	9	25	12	30	ns	
12	t _{RSH}	RAS hold time	6	—	8		10	—	ns	
13	t _{CSH}	CAS hold time	32	—	40		48	—	ns	
14	t _{CRP}	CAS to RAS precharge time	5	—	5	—	5	—	ns	
15	t _T	Transition time (rise and fall)	1	50	1	50	1	50	ns	7
16	t _{REF}	Refresh period	—	64	—	64	—	64	ms	
17	t _{REF}	Refresh period for L-versions	—	256	—	256	—	256	ms	

Read Cycle

18	t_{RAC}	Access time from $\overline{RAS}$	—	40	—	50	—	60	ns	8, 9
19	t_{CAC}	Access time from $\overline{CAS}$	—	10	—	13	—	15	ns	8, 9
20	t_{CAA}	Access time from column address	—	20	—	25	—	30	ns	8,10
21	t_{OEA}	$\overline{OE}$ access time	—	10	—	13	—	15	ns	
22	t_{RAL}	Column address to $\overline{RAS}$ lead time	20	—	25	—	30	—	ns	
23	t_{RCS}	Read command setup time	0	—	0	—	0	—	ns	
24	t_{RCH}	Read command hold time	0	—	0	—	0	—	ns	11
25	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	11
26	t_{CLZ}	$\overline{CAS}$ to output in low-Z	0	—	0	—	0	—	ns	8
27	t_{OFF}	Output buffer turn-off delay	0	10	0	13	0	15	ns	12
28	t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$	0	10	0	13	0	15	ns	12
29	t_{DZC}	Data to $\overline{CAS}$ low delay	0	—	0	—	0	—	ns	13
30	t_{DZO}	Data to $\overline{OE}$ low delay	0	—	0	—	0	—	ns	13

AC Characteristics ^(5,6) (Continued) $T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3\text{V}$, $t_T = 2 \text{ ns}$

#	Symbol	Parameter	-40		- 50		- 60		Unit	Note
			min.	max.	min.	max.	min.	max.		
31	t_{CDD}	$\overline{\text{CAS}}$ high to data delay	10	—	13	—	15	—	ns	14
32	t_{ODD}	$\overline{\text{OE}}$ high to data delay	10	—	13	—	15	—	ns	14

Write Cycle

33	t_{WCH}	Write command hold time	5	—	7	—	10	—	ns	
34	t_{WP}	Write command pulse width	5	—	7	—	10	—	ns	
35	t_{WCS}	Write command setup time	0	—	0	—	0	—	ns	15
36	t_{RWL}	Write command to $\overline{\text{RAS}}$ lead time	6	—	8	—	10	—	ns	
37	t_{CWL}	Write command to $\overline{\text{CAS}}$ lead time	6	—	8	—	10	—	ns	
38	t_{DS}	Data setup time	0	—	0	—	0	—	ns	16
39	t_{DH}	Data hold time	5	—	7	—	10	—	ns	16

Read-modify-Write Cycle

40	t_{RWC}	Read-write cycle time	89	—	109	—	133	—	ns	
41	t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	52	—	65	—	77	—	ns	15
42	t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	22	—	28	—	32	—	ns	15
43	t_{AWD}	Column address to $\overline{\text{WE}}$ delay time	32	—	40	—	47	—	ns	15
44	t_{OEHL}	$\overline{\text{OE}}$ command hold time	5	—	7	—	10	—	ns	

EDO Page Mode Cycle

45	t_{PC}	EDO Page Mode cycle time	16	—	20	—	24	—	ns	
46	t_{CPA}	Access time from $\overline{\text{CAS}}$ precharge	—	22	—	28	—	34	ns	7
47	t_{COH}	Output data hold time	5	—	5	—	5	—	ns	
48	t_{RAS}	$\overline{\text{RAS}}$ pulse width in EDO page mode	40	200k	50	200k	60	200k	ns	
49	t_{RHPC}	$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	22	—	28	—	34	—	ns	
50	t_{OEP}	$\overline{\text{OE}}$ pulse width	5	—	5	—	5	—	ns	
51	t_{OEHC}	$\overline{\text{OE}}$ hold time from $\overline{\text{CAS}}$ high	5	—	5	—	5	—	ns	
52	t_{WEZ}	Output buffer turn-off delay from $\overline{\text{WE}}$	0	10	0	13	0	15	ns	

EDO Page Mode Read-modify-Write Cycle

53	t_{PRWC}	EDO page mode read-write cycle time	42	—	54	—	63	—	ns	
54	t_{CPWD}	$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$	32	—	41	—	49	—	ns	

AC Characteristics ^(5,6) (Continued) $T_A = 0 \text{ to } 70^\circ\text{C}, V_{CC} = 3.3 \text{ V} \pm 0.3\text{V}, t_T = 2 \text{ ns}$

#	Symbol	Parameter	-40		- 50		- 60		Unit	Note
			min.	max.	min.	max.	min.	max.		
CAS before RAS Refresh Cycle										
55	t _{CSR}	CAS setup time	5	—	5	—	5	—	ns	
56	t _{CHR}	CAS hold time	5	—	5	—	10	—	ns	
57	t _{RPC}	RAS to CAS precharge time	5	—	5	—	5	—	ns	
58	t _{WRP}	Write to RAS precharge time	5	—	5	—	10	—	ns	
59	t _{WRH}	Write hold time referenced to RAS	5	—	5	—	10	—	ns	
Self Refresh Cycle (L-versions only)										
60	t _{RASS}	RAS pulse width	100k		100k	—	100k	—	ns	17
61	t _{RPS}	RAS precharge time	69	—	84	—	104	—	ns	17
62	t _{CHS}	CAS hold time	-50	—	-50	—	-50	—	ns	17
Test Mode Cycle										
63	t _{WTS}	Write command setup time	5	—	5	—	5	—	ns	18
64	t _{WTH}	Write command hold time	5	—	5	—	5	—	ns	18

Notes:

- 1) All voltages are referenced to VSS.
 V_{IH} may overshoot to $V_{CC} + 0.2V$ for pulse widths of $< 4ns$ with 3.3V. V_{IL} may undershoot to $-2.0V$ for pulse width $< 4.0 ns$ with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.
- 2) I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} and I_{CC7} depend on cycle rate.
- 3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while $\overline{RAS} = V_{IL}$. In the case of I_{CC4} it can be changed once or less during a EDO page mode cycle (t_{PC}).
- 5) An initial pause of 100 μs is required after power-up followed by 8 $\overline{RAS}$ -only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before- $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
- 6) AC measurements assume $t_f = 2 ns$.
- 7) $V_{IH (min.)}$ and $V_{IL (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- 8) Measured with the specified current load and 100 pF at $V_{OH} = 2.0 V$ and $V_{OL} = 0.8 V$.
- 9) Operation within the $t_{RCD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RCD (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD (max.)}$ limit, then access time is controlled by t_{AC} .
- 10) Operation within the $t_{RAD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RAD (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD (max.)}$ limit, then access time is controlled by t_{AA} .
- 11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 12) $t_{OFF (max.)}$ and $t_{OEZ (max.)}$ define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
- 13) Either t_{DZC} or t_{DZO} must be satisfied.
- 14) Either t_{CDD} or t_{ODD} must be satisfied.
- 15) t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS (min.)}$, the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD (min.)}$, $t_{CWD} > t_{CWD (min.)}$, $t_{AWD} > t_{AWD (min.)}$ and $t_{CPWD} > t_{CPWD (min.)}$, the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 16) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
- 17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
 If row addresses are being refresh in an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.
 If row addresses are being refresh in any other manner (ROR - Distributed/Burst or CBR-Burst) over the refresh interval, then a full set of row refreshed must be performed immediately before entry to and immediately after exit from Self Refresh
- 18) In a Test Mode Read Cycle, the value of t_{rac} , t_{CAC} and t_{CPA} are delayed by 5 ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must be adjusted by 5 ns.

The diagram illustrates the timing relationships between several control and data signals during memory access operations. The signals shown are:

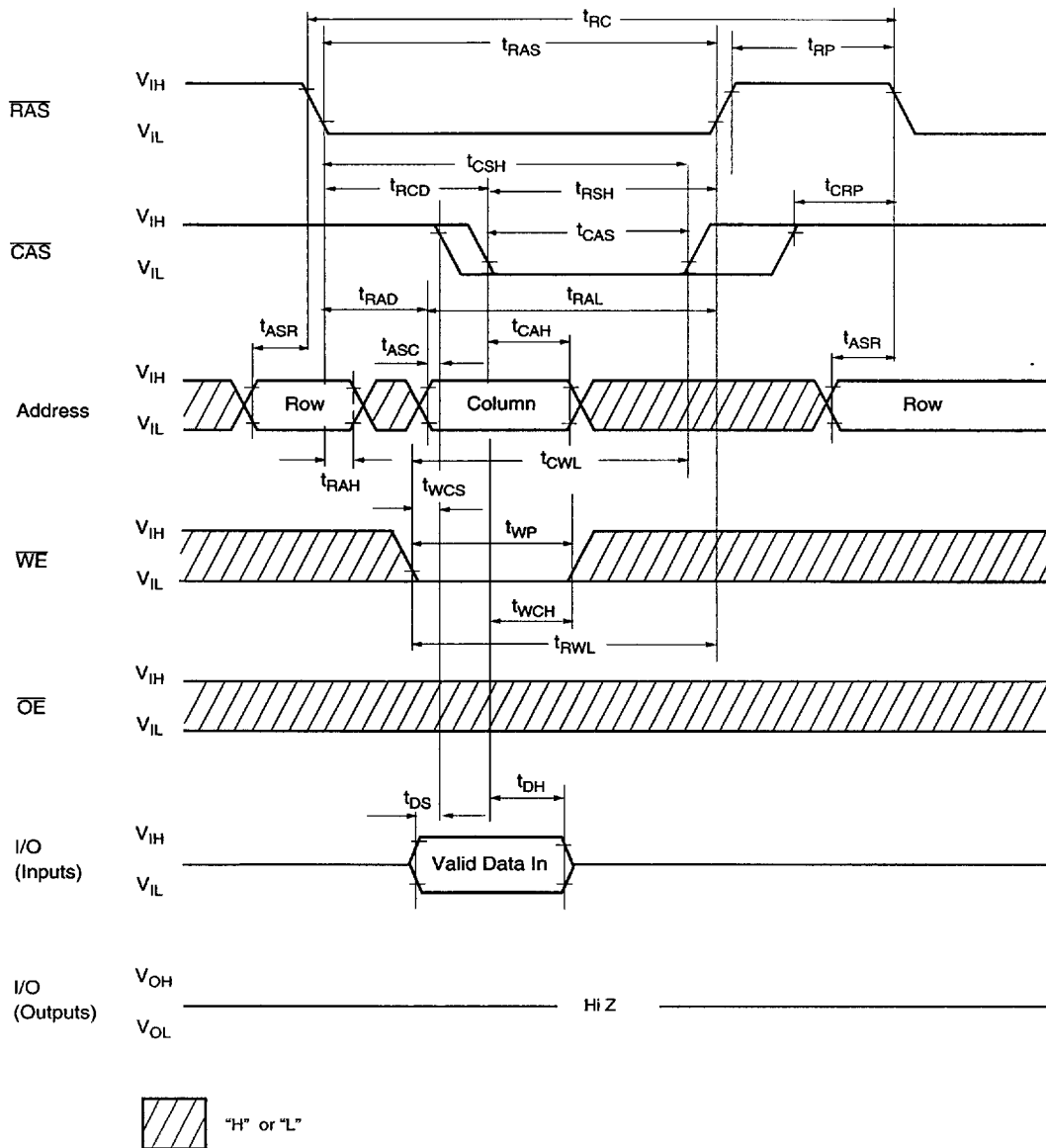
- RAS**: Row Address Strobe, active low.
- CAS**: Column Address Strobe, active low.
- Address**: Bus address signal, alternating between Row and Column phases.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- I/O (Inputs)**: Data bus inputs.
- I/O (Outputs)**: Data bus outputs, transitioning from High Impedance (Hi Z) to Valid Data Out.

Key timing parameters labeled include:

- t_{RAS} , t_{RC} , t_{RP}
- t_{CSH} , t_{RSH} , t_{CRP}
- t_{RCD} , t_{CAS}
- t_{RAD} , t_{RAL}
- t_{ASR} , t_{ASC} , t_{CAH}
- t_{RAH} , t_{RCS} , t_{RRH}
- t_{CAA} , t_{OEA}
- t_{DZC} , t_{DZO} , t_{DD} , t_{CDD}
- t_{CAC} , t_{CLZ} , t_{OFF} , t_{OEZ}
- t_{RAC}

A legend indicates that hatched areas represent "H" or "L" levels.

WL1

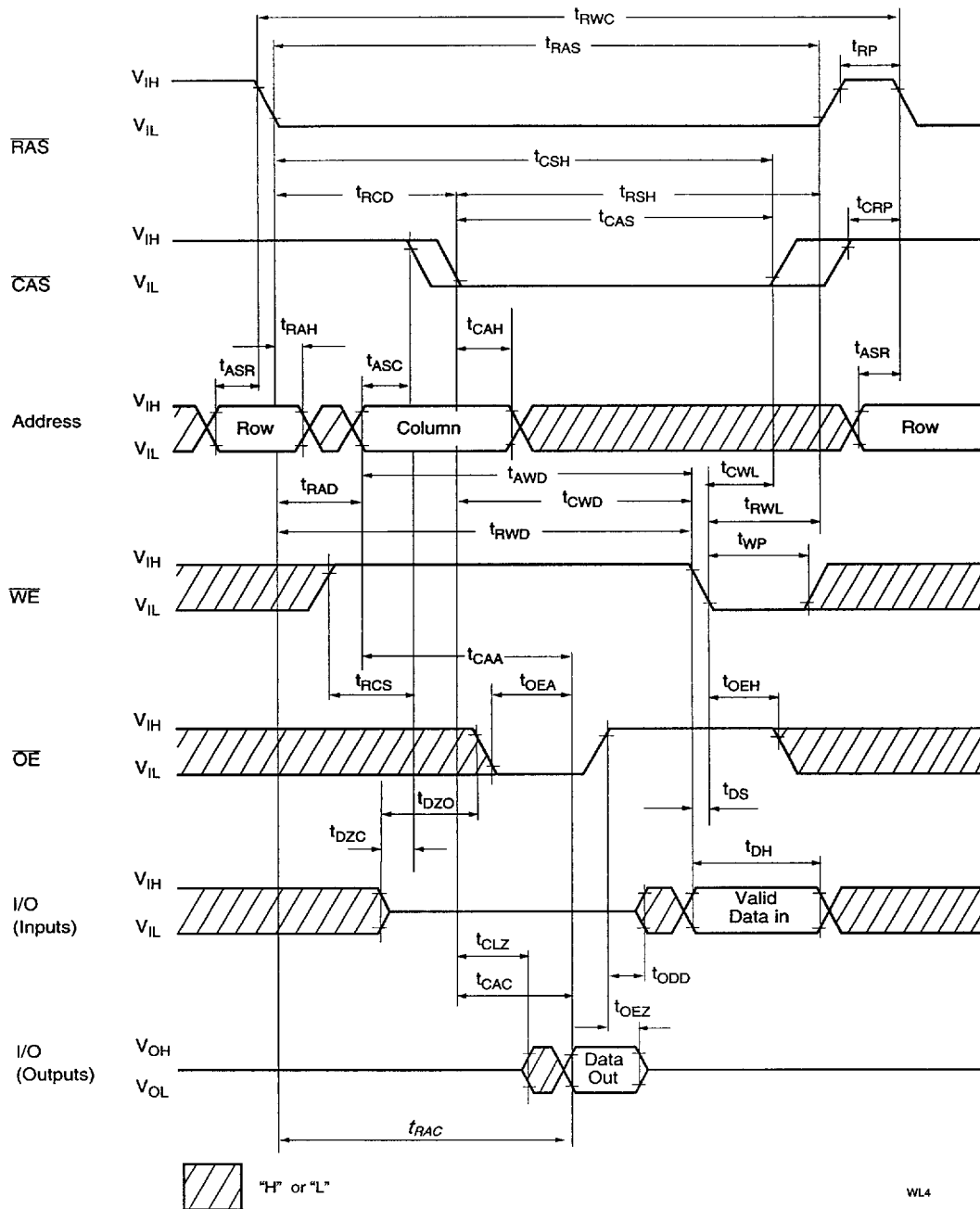
Waveforms of Write Cycle (Early Write)

WL2

[illegible]

 "H" or "L"

WL3

Waveforms of Read-Write (Read-Modify-Write) Cycle

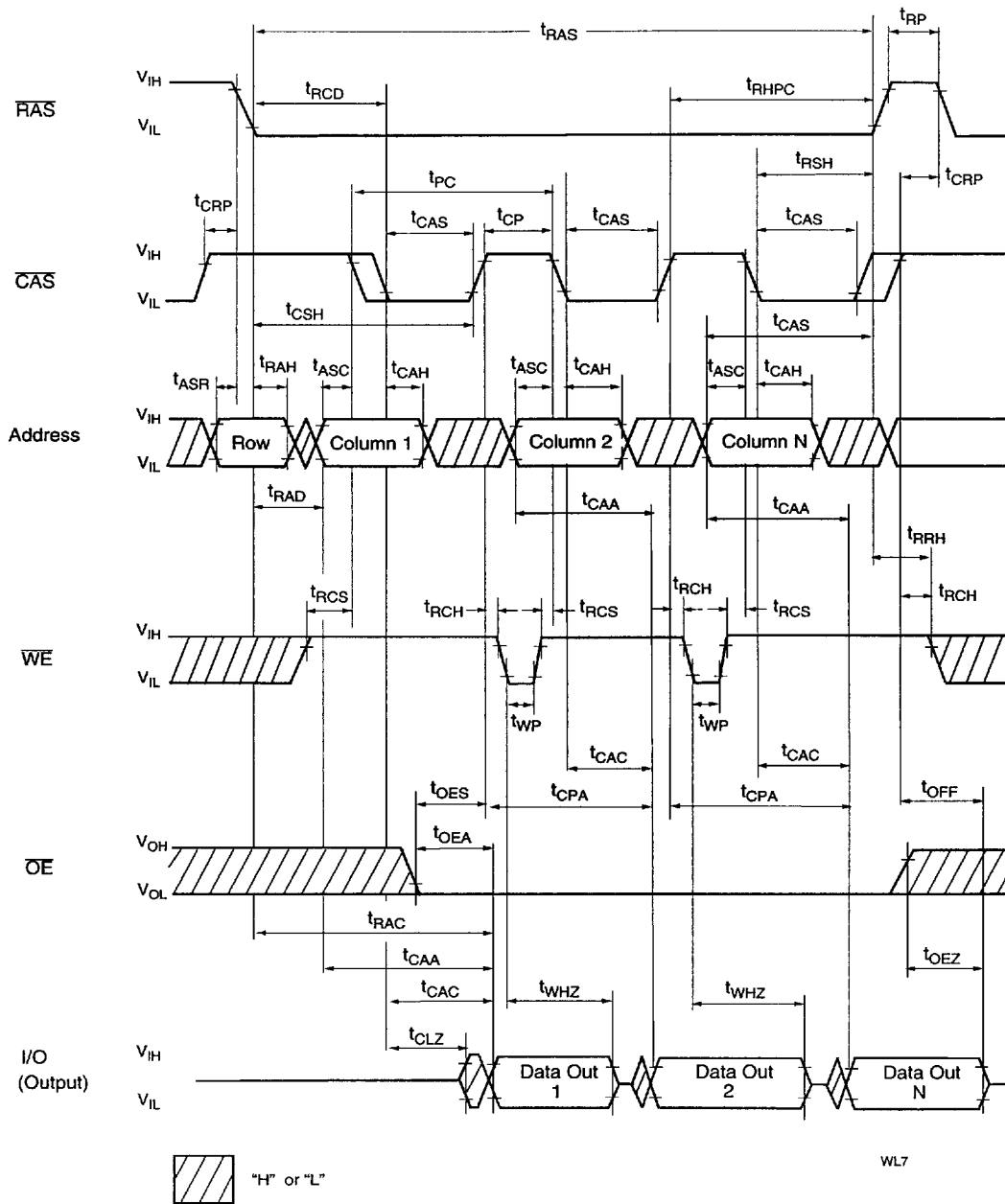
WL4

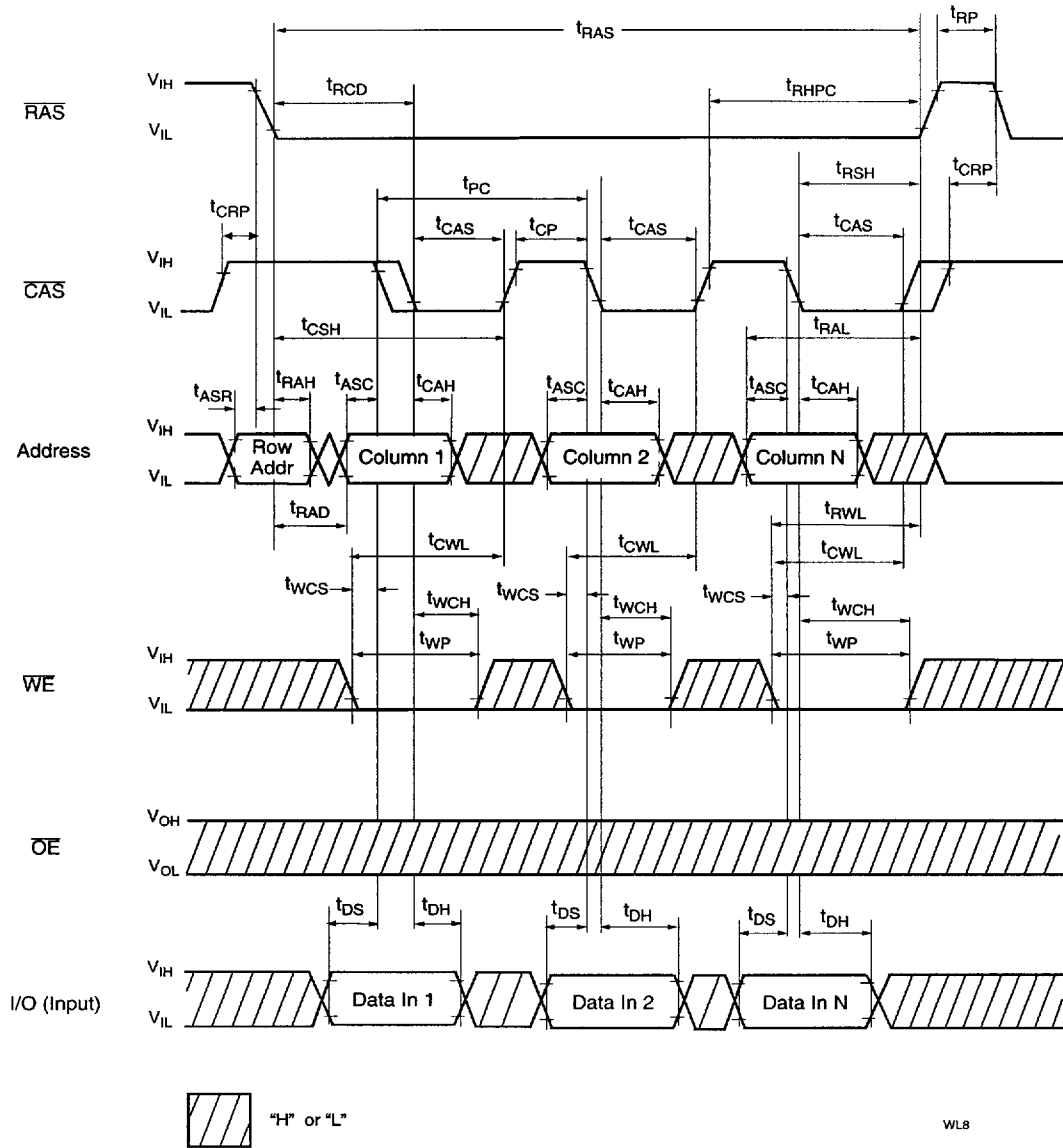
Timing diagram for a 64K16 asynchronous DRAM. The diagram illustrates the relationship between various control signals and data output over time. The signals shown are:

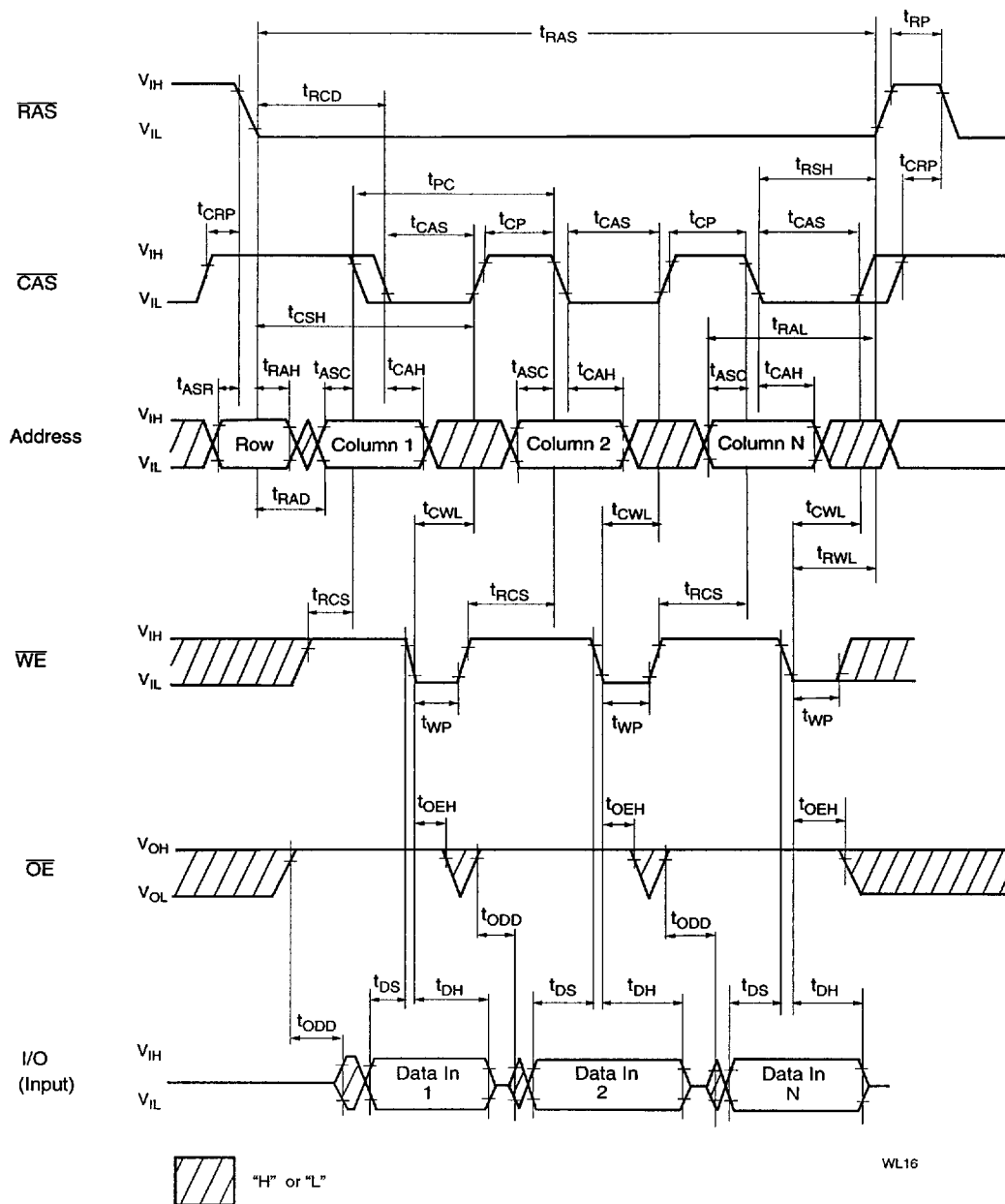
- RAS**: Row Address Strobe. Parameters include t_{RCD} (RAS to CAS delay), t_{RAS} (RAS pulse width), t_{RHPC} (RAS to next RAS delay), and t_{RP} (RAS precharge time).
- CAS**: Column Address Strobe. Parameters include t_{CRP} (CAS precharge time), t_{PC} (CAS pulse width), t_{CAS} (CAS to data delay), t_{CP} (CAS to next CAS delay), t_{CRH} (CAS to next RAS delay), t_{RSH} (CAS to next RAS delay), and t_{RAL} (CAS to next RAS delay).
- Address**: Row and Column addresses. Parameters include t_{ASR} (Address Strobe to RAS delay), t_{RAH} (Row Address High to RAS delay), t_{ASC} (Address Strobe to CAS delay), t_{CAH} (Column Address High to CAS delay), t_{RAD} (Row Address Delay), t_{RCS} (Row Address Strobe to CAS delay), t_{CAC} (Column Address High to CAS delay), t_{CAA} (Column Address High to CAS delay), t_{CPA} (Column Address High to CAS delay), t_{OES} (Output Enable Strobe to CAS delay), t_{OEA} (Output Enable Strobe to CAS delay), t_{RAC} (Row Address High to CAS delay), t_{COH} (Column Address High to CAS delay), t_{CLZ} (Column Address High to CAS delay), t_{RRH} (Row Address High to RAS delay), t_{RCH} (Row Address High to RAS delay), t_{OFF} (Output Enable Strobe to RAS delay), and t_{OEZ} (Output Enable Strobe to RAS delay).
- WE**: Write Enable. Parameters include t_{CAC} (Write Enable High to CAS delay), t_{CAA} (Write Enable High to CAS delay), t_{CPA} (Write Enable High to CAS delay), t_{OES} (Write Enable Strobe to CAS delay), t_{OEA} (Write Enable Strobe to CAS delay), t_{RAC} (Write Enable High to CAS delay), t_{COH} (Write Enable High to CAS delay), t_{CLZ} (Write Enable High to CAS delay), t_{RRH} (Write Enable High to RAS delay), t_{RCH} (Write Enable High to RAS delay), t_{OFF} (Write Enable Strobe to RAS delay), and t_{OEZ} (Write Enable Strobe to RAS delay).
- OE**: Output Enable. Parameters include t_{CAC} (Output Enable High to CAS delay), t_{CAA} (Output Enable High to CAS delay), t_{CPA} (Output Enable High to CAS delay), t_{OES} (Output Enable Strobe to CAS delay), t_{OEA} (Output Enable Strobe to CAS delay), t_{RAC} (Output Enable High to CAS delay), t_{COH} (Output Enable High to CAS delay), t_{CLZ} (Output Enable High to CAS delay), t_{RRH} (Output Enable High to RAS delay), t_{RCH} (Output Enable High to RAS delay), t_{OFF} (Output Enable Strobe to RAS delay), and t_{OEZ} (Output Enable Strobe to RAS delay).
- I/O (Output)**: Data output. Parameters include t_{CAC} (Data Output High to CAS delay), t_{CAA} (Data Output High to CAS delay), t_{CPA} (Data Output High to CAS delay), t_{OES} (Data Output Strobe to CAS delay), t_{OEA} (Data Output Strobe to CAS delay), t_{RAC} (Data Output High to CAS delay), t_{COH} (Data Output High to CAS delay), t_{CLZ} (Data Output High to CAS delay), t_{RRH} (Data Output High to RAS delay), t_{RCH} (Data Output High to RAS delay), t_{OFF} (Data Output Strobe to RAS delay), and t_{OEZ} (Data Output Strobe to RAS delay).

The diagram also shows the data output sequence: Data Out 1, Data Out 2, and Data Out N. A legend indicates that hatched areas represent 'H' or 'L' levels.

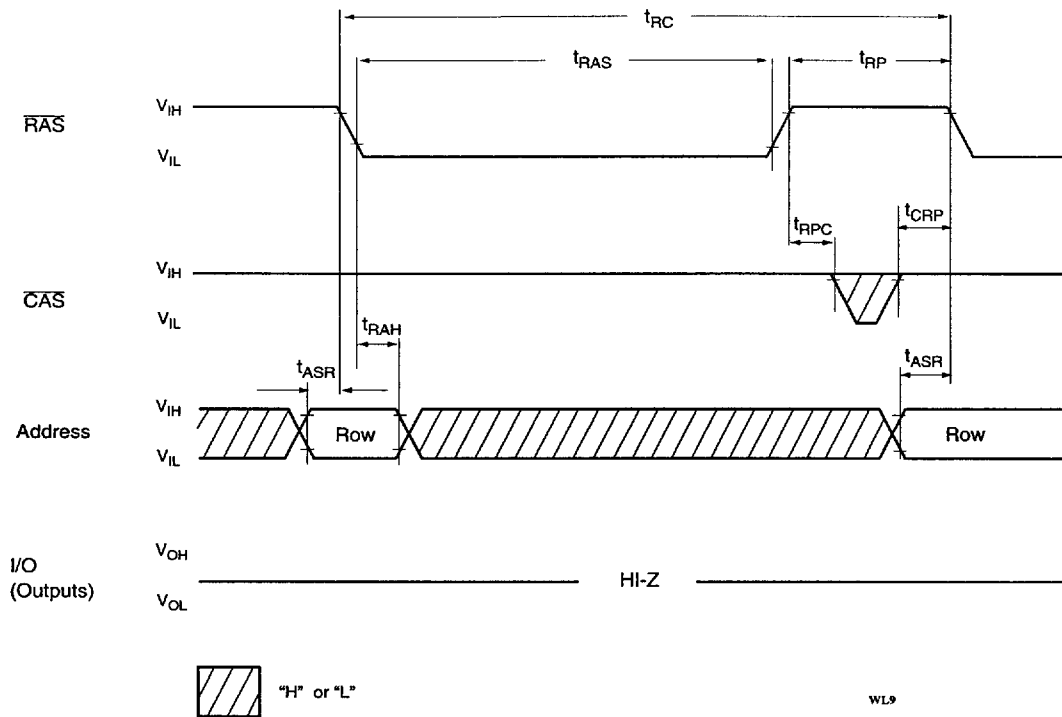
[illegible]

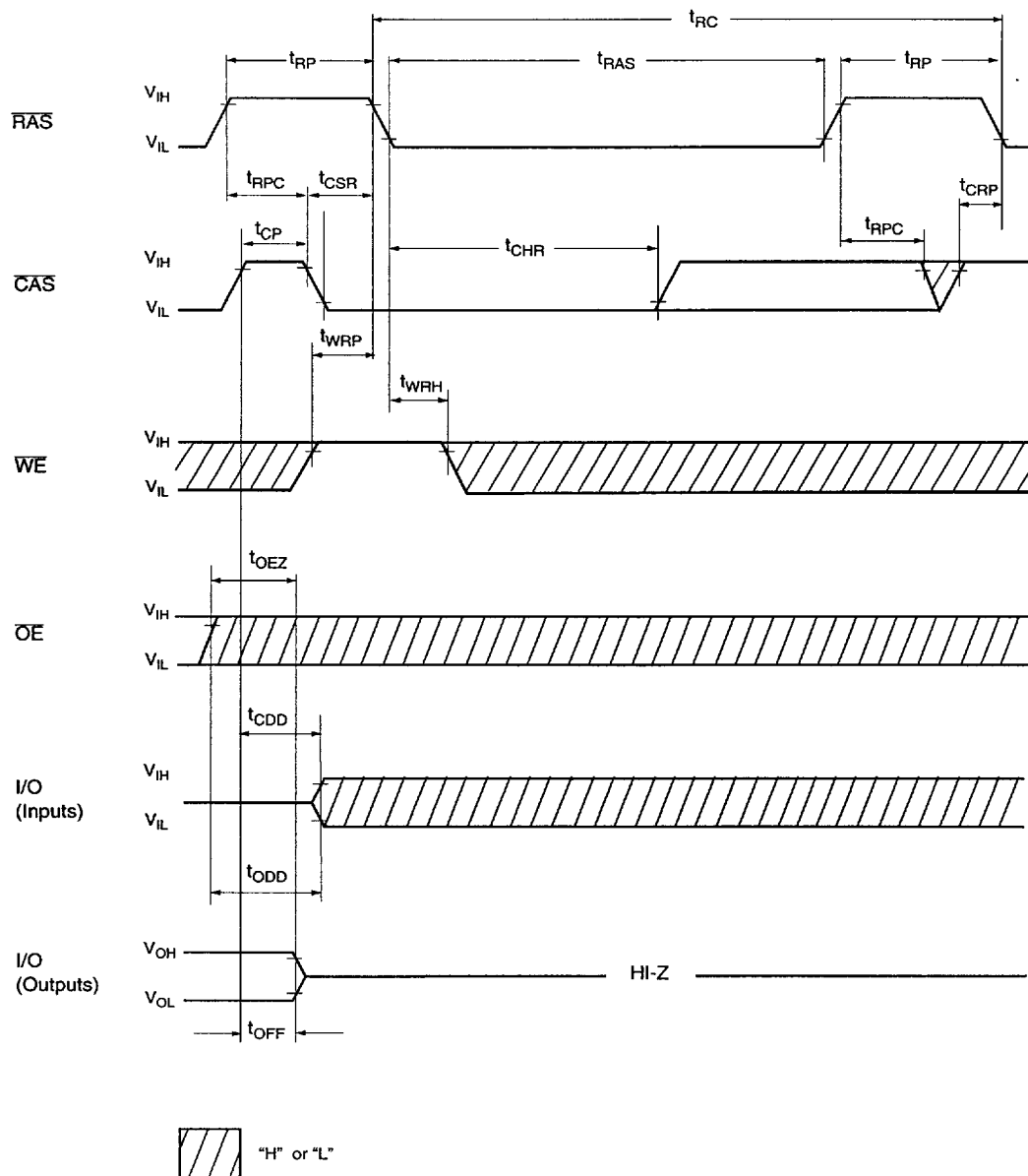
Waveforms of EDO Page Mode Read Cycle ($\overline{WE}$ Control)

Waveforms of EDO Page Mode Early Write Cycle

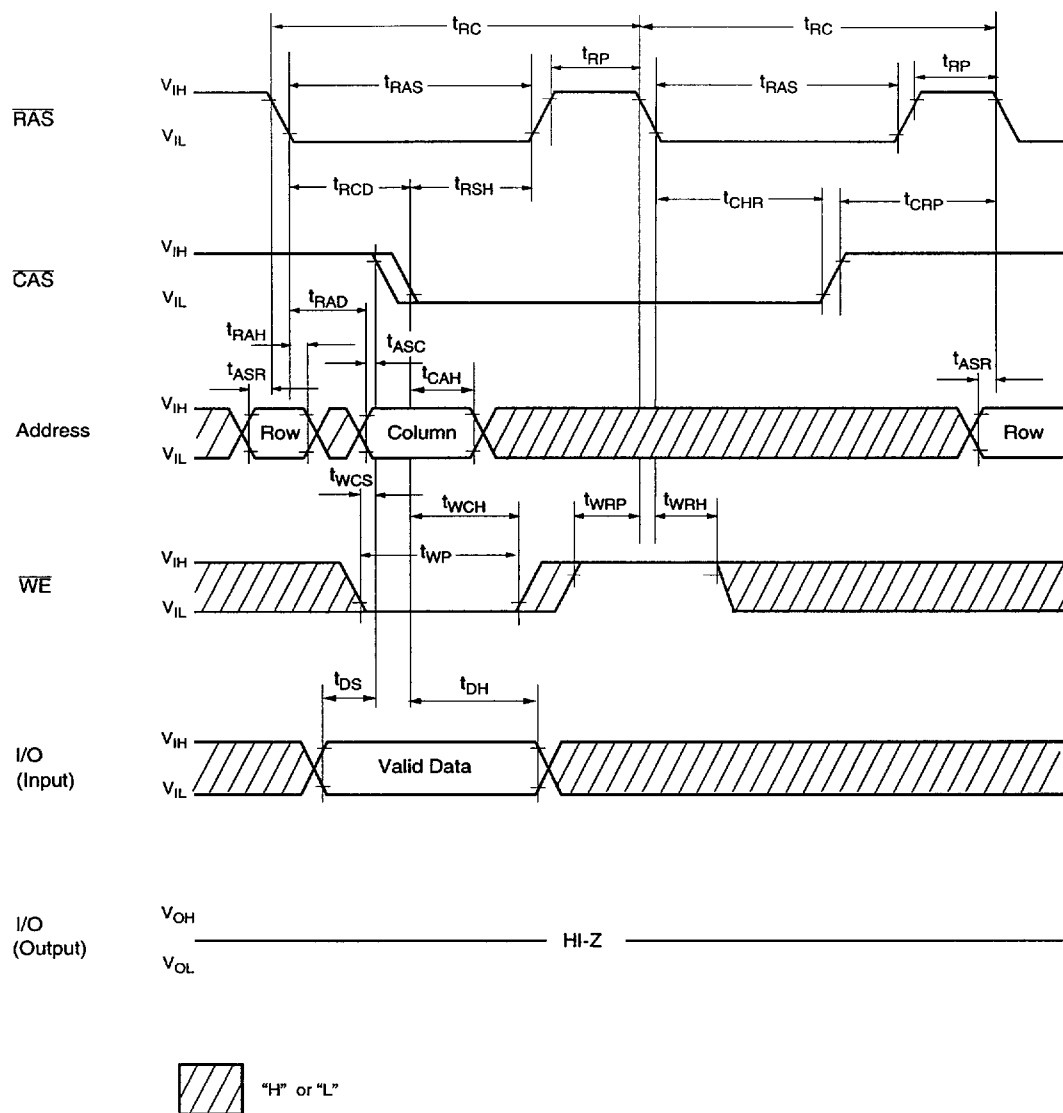
Waveforms of EDO Page Mode Late Write Cycle

WL17

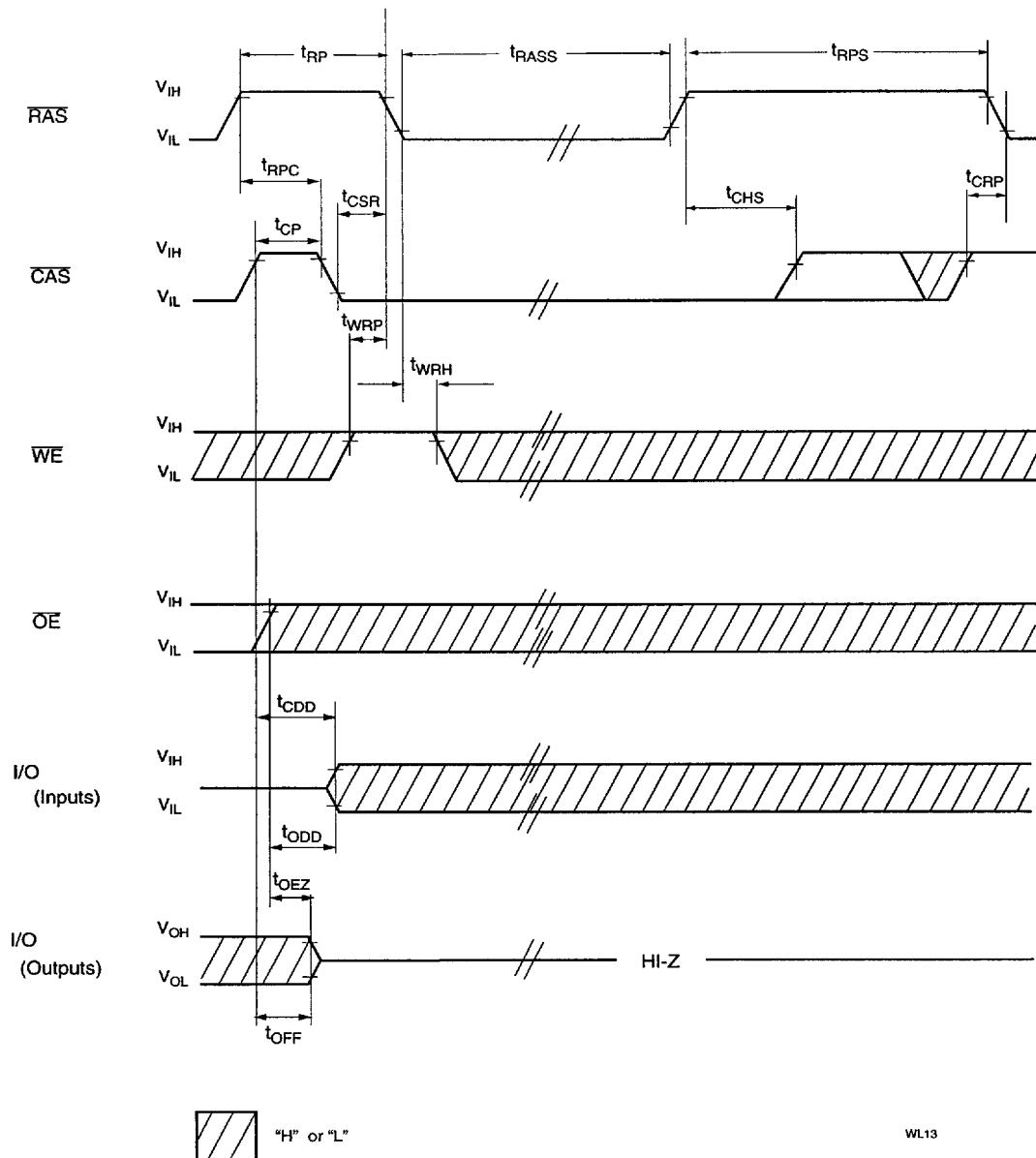
Waveforms of $\overline{\text{RAS}}$ Only Refresh Cycle


Waveforms of $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

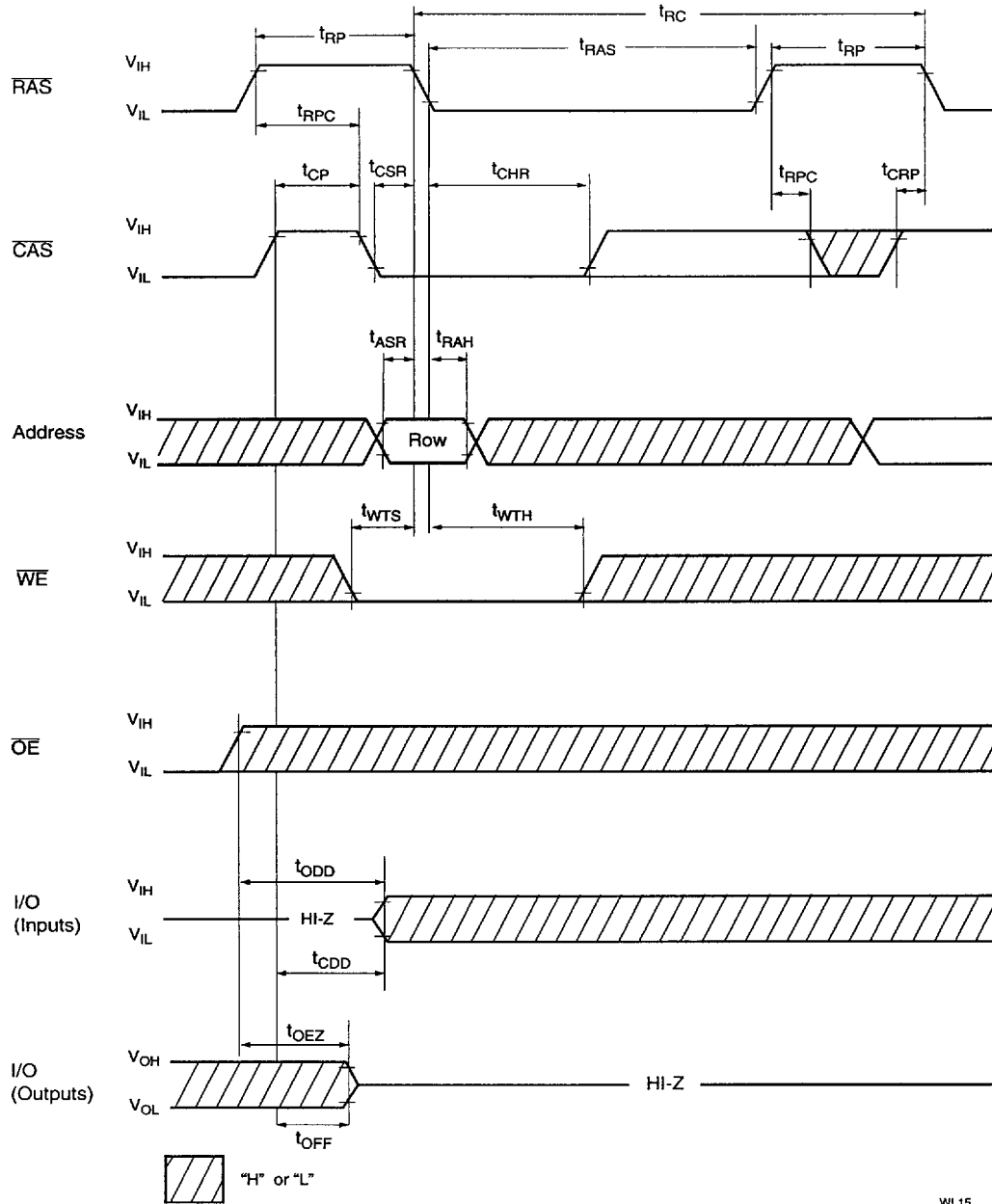
WL10

Waveforms of Hidden Refresh Early Write Cycle

WL12

Waveforms of Self Refresh (Sleep Mode)

WL13

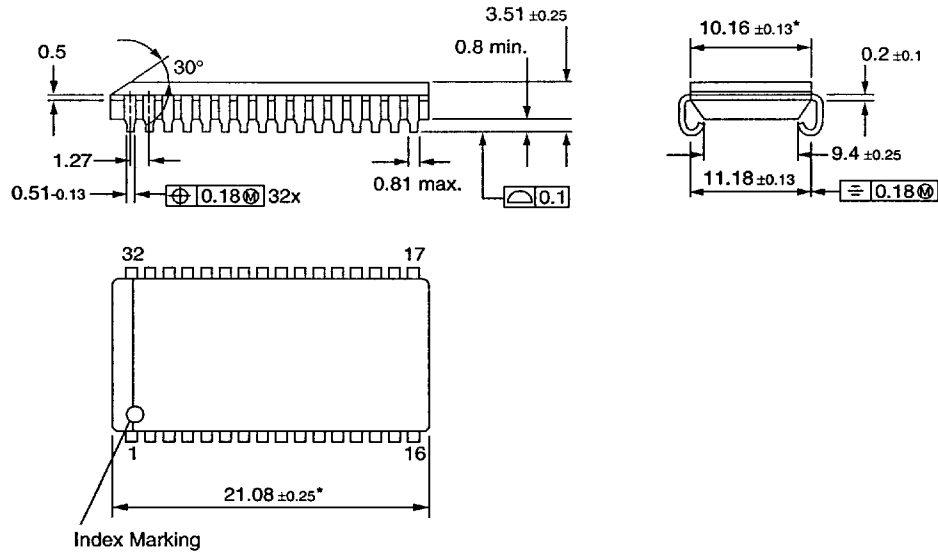
Waveforms of Test Mode Entry Cycle

WL15

Package Diagrams

32-pin 400 mil SOJ

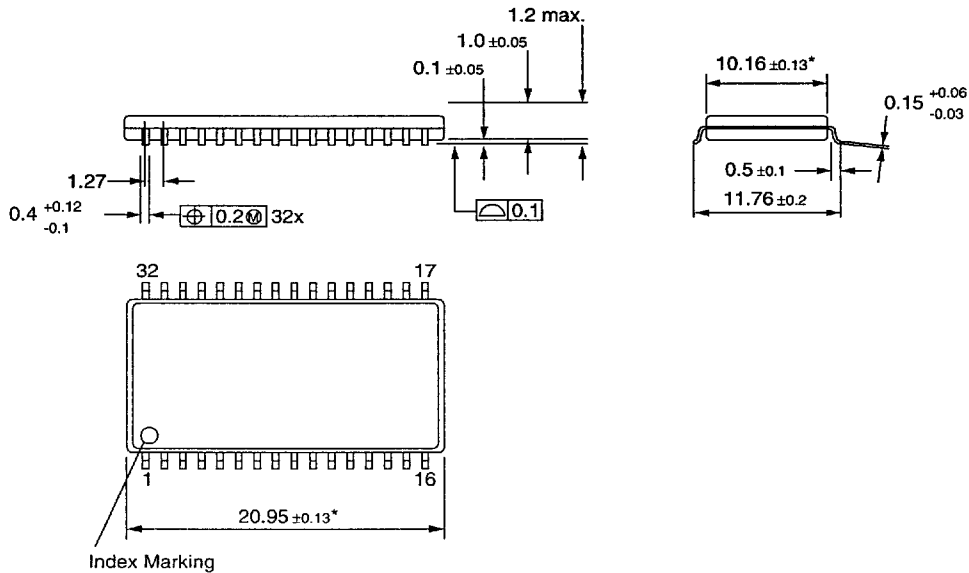
Units in mm



* Does not include plastic or metal protrusion of 0.15 max. per side

32-pin 400 mil TSOP-II

Units in mm



* Does not include plastic or metal protrusion of 0.25 max. per side