WD83C805

Token Ring

Interface Device

WESTERN DIGITAL

17

17

T-75-49

TABLE OF CONTENTS

T-75-49

LIST OF ILLUSTRATIONS

LIST OF TABLES

T-75-49

1.0 INTRODUCTION

This document describes the Western Digital WD83C805 Token Ring interface (TRI) CMOS LSI integrated circuit. The TRI is an analog device which provides line-interface and clock/data recovery functions in the IBM 802.5 Token Ring LAN environment. See Appendix A for an overview of the 802.5 physical-layer environment.

The WD83C805 is a single chip Token Ring interface that can operate at 4 and 16 Mbps data rates and is interoperable with other 4 Mbps and 16 Mbps Token Ring network equipment.

The WD83C805 TRI is parametrically compatible with existing designs in key respects, such as signal coding, levels, timing, and timing recovery jitter bandwidth in the PLL.

The TRI operates in the star-wired, logical ring token-passing LAN environment as standardized by the IEEE 802.5 standards committee and offered commercially by IBM and other companies. The current revision of the standard, IEEE Std 802.5-1989, defines the requirements for Token Ring.

The WD83C805 architecture is compatible with applications that operate at either a 4 or 16 Mbps transmission rate. Some circuit parameters differ for the two rates. In this document, the requirements for the 4 and 16 Mbps versions are called out separately only where they differ. When this is done, the 16 Mbps specification is enclosed within square brackets: [ ]. Where only one requirement is given, the document is the same for both 4 and 16 Mbps.

The WD83C805 TRI operates as a companion to the WD83C825 token-ring controller (TRC). Together they form a two-chip hardware-level line interface and media access control (MAC) subsystem. The TRC implements MAC functions such as the token-ring protocol, encoding/decoding of data to and from the TRI, frame address recognition, cyclic redundancy check (CRC) generation and checking, DMA to shared memory (host interface), detection of ring errors, transmit output driver, and lobe insertion circuitry. The TRC is a full-custom design, implemented in a 1.75 micron analog CMOS process.

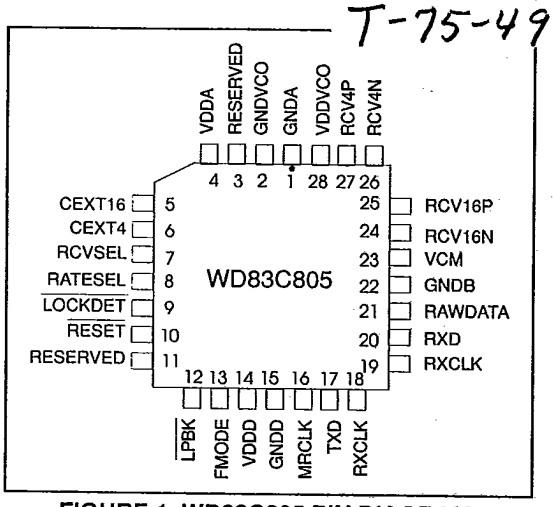


FIGURE 1. WD83C805 PIN DIAGRAM

1.1 Features

- Line interface to the IBM 802.5 Token Ring LAN
- 4 or 16 Mbps transmission rate
- 8 or 32 MHz clock rate
- Meets IEEE 802.5-1989
- Single chip 1.75 micron CMOS device
- 28-pin PLCC package
- Interfaces with Western Digital's WD83C825 Token Ring controller device to form a 2-chip hardware-level line interface and media access control subsystem
- Interfaces with the Texas Instruments 802.5 controller TMS 380C16 using a minimum number of external components

T-75-49

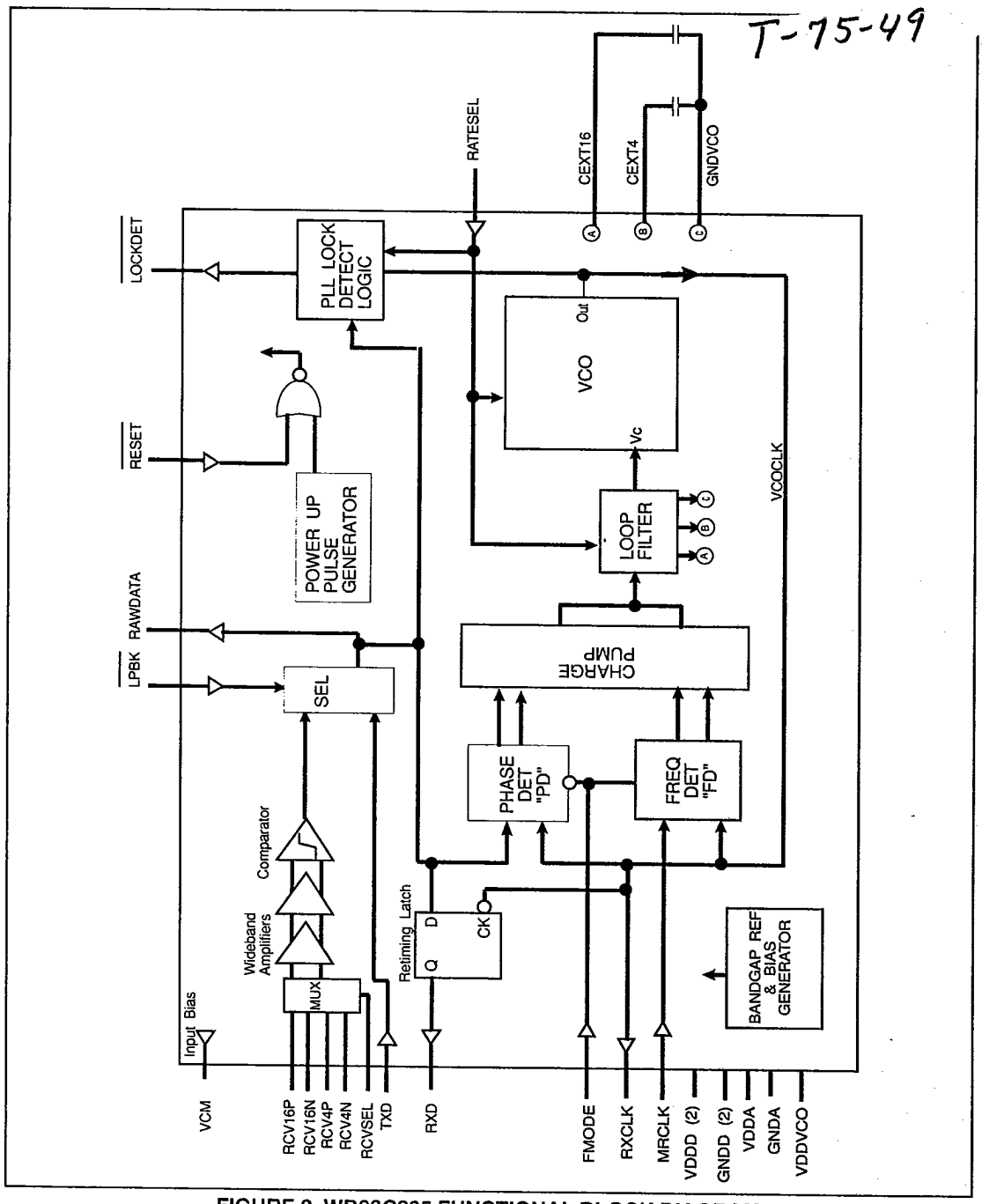


FIGURE 2. WD83C805 FUNCTIONAL BLOCK DIAGRAM

T-75-49

2.0 WD83C805 ARCHITECTURE

2.1 Phase-Locked Loop

The functional elements of the phase-locked loop are the phase/frequency detector (PFD), charge pump, loop filter, and VCO.

The PLL is a classic charge-pump analog architecture, implemented with state-of-the art linear CMOS technology. A block diagram of the PLL is included in Figure 2.

The dynamics of the PLL were carefully optimized to provide high-performance operation in the token-ring environment as defined by the IEEE standard. The PLL is designed to be interoperable in an environment with Token Ring equipment from other manufacturers.

2.2 Analog Front-End

The typical Token Ring transmission link consists of the transmit output driver, coupling transformers, transmission cable, receive equalization network, amplifiers, and slicing comparator.

The signal undergoes distortion as it propagates through the transmission line, due to variation with frequency of the line characteristics. This distortion is caused largely by a physical mechanism known as "skin effect."

Therefore, data equalization is employed before actual data recovery. The equalizer design is a tradeoff of jitter and eye opening at the extremes of the cable length. The WD83C805 is designed for use with an external equalizer, for compatibility with different media.

The WD83C805 analog front-end consists of two wideband gain stages, and a high-speed comparator. For specialized applications, the front-end may be bypassed by applying a preequalized and sliced (digital) input directly to the PLL, via the TXD input pin.

2.3 System Block Diagram

Figure 3 illustrates the WD83C805 in a system application with a host microprocessor and the WD83C825 Token Ring controller.

T-75-49

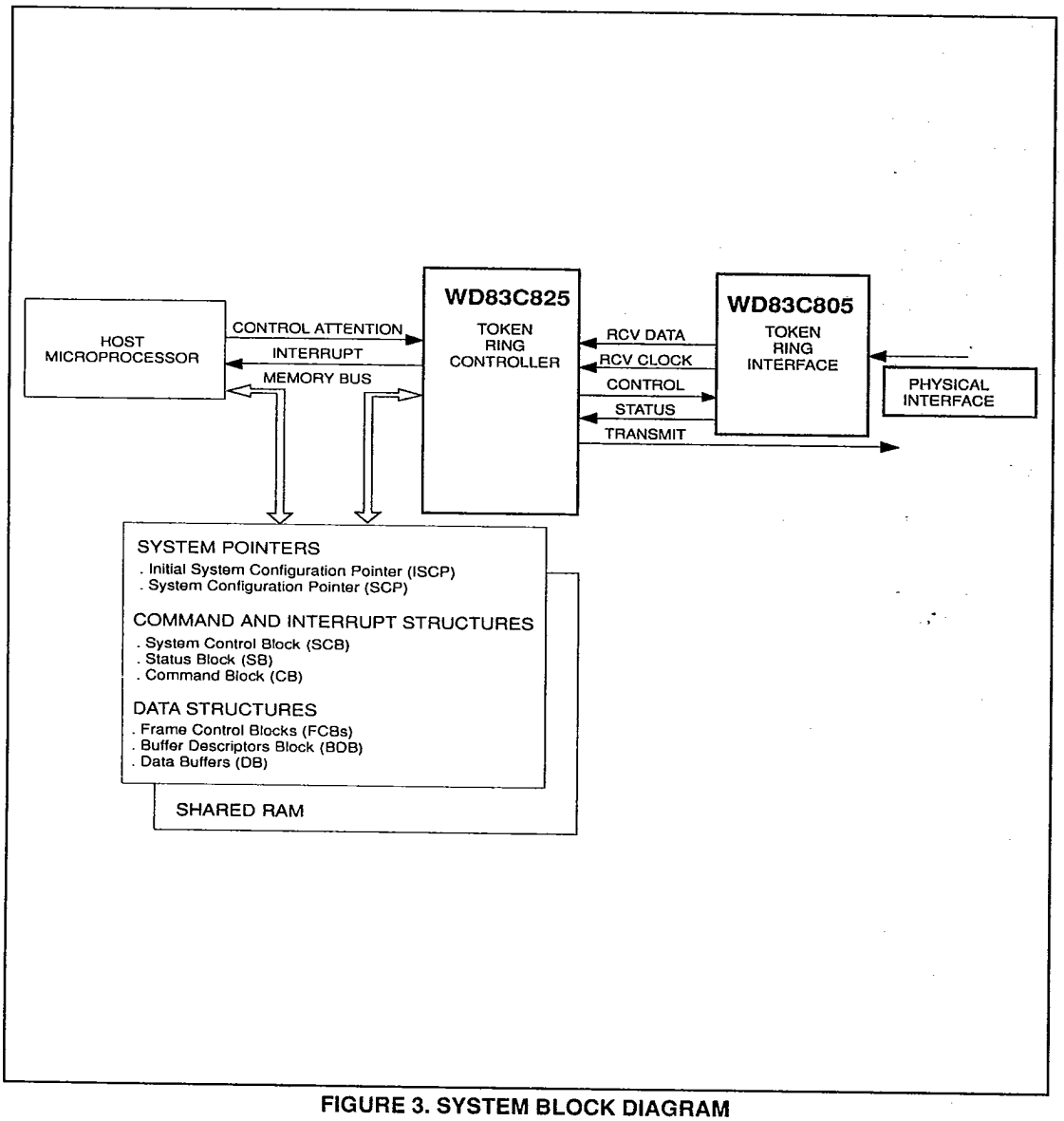


FIGURE 3. SYSTEM BLOCK DIAGRAM

3.0 PIN DESCRIPTION

T-75-49

The following table provides pin definitions for the 28-pin WD83C805 package.

PIN NO.	PIN SYMBOL	I/O	TYPE	DESCRIPTION
1	GNDA	---	S	Analog Ground/Substrate
2	GNDVCO	---	S	Analog VCO Ground
3	Reserved	---	---	Leave unconnected
4	VDDA	---	S	Analog 5V supply
5	CEXT16	I/O	A	External loop capacitor for 16 Mbps
6	CEXT4	I/O	A	Ext. cap for 4 Mbps (pins 5 & 6 may be connected together to one external cap)
7	RCVSEL	I	D	Select RCV inputs: High=RCV16x/Low=RCV4x (may be set independently from RATESEL, each pair of inputs can operate at 4 or 16 Mbps).
8	RATESEL	I	D	Select data rate: High for 16M/Low for 4 Mbps (sets RXCLK to 32 M or 8M, sets internal PLL rate/filter, and lock detect circuit parameters.)
9	$\overline{\text{LOCKDET}}$	O	D	Output low during phase lock to RCV data if edge density is correct. Also output low when the PLL is locked to the local oscillator (FMODE=1).
10	$\overline{\text{RESET}}$	I	D	Input low to reset internal logic and set VCO to center frequency.
11	Reserved	---	---	Connect to logic low or to ground.
12	$\overline{\text{LPBK}}$	I	D	Input low for loopback test (TXD input to PLL in place of RCV inputs data), high for normal use.
13	FMODE	I	D	Input high to select lock to local oscillator, low to select phase lock to data input. This is used to hold the PLL frequency close to the baud rate before acquiring the RCV data phase.
14	VDDD	---	S	Digital 5V supply.
15	GNDD	---	S	Digital Ground.
16	MRCLK	I	D	Local oscillator input - 32 MHz digital for 16 Mbps operation or 8 MHz for 4 Mbps operation. (Normally provided by WD83C825.)
17	TXD	I	D	Data input for loopback test.

TABLE 1. PIN DESCRIPTION

T-75-49

PIN NO.	PIN SYMBOL	I/O	TYPE	DESCRIPTION
18	VDDB	---	S	Digital 5V supply
19	RXCLK	O	D	Receive clock recovered from RCV data input signal (or from local oscillator if FMODE=1).
20	RXD	O	D	Receive data sampled with RXCLK. No decoding is done in TRI, so this output is Manchester symbols. The output changes on RXCLK falling edge.
21	RAWDATA	O	D	Receive data from comparator output, not sampled by RXCLK. Delay from RCVxx is 25 ns nominal.
22	GNDB	---	S	Digital Ground
23	VCM	O	A	Bias level for small-signal RCV inputs (DC voltage for center tap in transformer-coupled input circuits).
24	RCV16N	I	A	Receive input: High level=RXD/RAWDATA low
25	RCV16P	I	A	Receive input: High level=RXD/RAWDATA high
26	RCV4N	I	A	Receive input: High level=RXD/RAWDATA low
27	RCV4P	I	A	Receive input: High level=RXD/RAWDATA high
28	VDDVCO	---	S	VCO 5V supply

TABLE 1. PIN DESCRIPTION (CONT)

NOTE:
A= analog
D= digital
S= supply

T-75-49

4.0 ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	6 Volts
Digital input voltage	0 to 5.5 Volts
Differential input voltage	-5.5 to 16 Volts
Storage temperature	-65° C (-85°F) to 150° C (302°F)

NOTE
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

4.1 RECOMMENDED OPERATING CONDITIONS

The characteristics below apply for the following conditions, unless otherwise noted.

Operating temperature range	0° (32°F) to 70° C (158°F)
Supply voltage (V_{DD})	5 ± 5% Volts

T-75-49

4.2 D.C . CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input High Voltage	2.0	---	V	
V_{IL}	Input Low Voltage	---	0.8	V	
I_{IH}	Input High Current	---	50	µA	$V_{IN} = V_{DD}$
I_{IL}	Input Low Current	---	-300	µA	$V_{IN} = 0.5V$
V_{CLD}	V_{DD} Diode Clamp Voltage	400	900	mV	$I_{IN} = 1.0$ mA
V_{CLS}	V_{SS} Diode Clamp Voltage	-400	-900	mV	$I_{IN} = -1.0$ mA
V_{OH}	Output High Voltage	2.4	---	V	$I_{OH} = -20$ mA
V_{OL}	Output Low Voltage	---	0.4	V	$I_{OL} = 20$ mA
I_{OS}	Output Short Circuit Current	-40	-200	mA	
V_{CM}	Common Mode Voltage	TBD	TBD	V	$R_{LOAD} > 100K$
I_{DD}	Dynamic Supply Current	---	65	mA	

TABLE 2. DC CHARACTERISTICS

NOTE:
The following conditions apply, unless otherwise noted: Ta = 0°C (32°F) to 70°C (158°F), V_{DD} = +5V ±5%

5.0 AC TIMING CHARACTERISTICS

T-75-49

The following notes apply to all of the parameters presented in this section:

All units are in nanoseconds

NUMBER	PARAMETER	MIN	TYPICAL	MAX
	RXCLK TIMING			
1	RXCLK period		125	
2	RXCLK high time	TBD		
3	RXCLK low time	TBD		
4	RXCLK rise time			TBD
5	RXCLK fall time			TBD
	MRCLK TIMING			
6	MRCLK period	TBD	125	TBD
7	MRCLK high time	TBD	62.5	
8	MRCLK low time	TBD	62.5	
9	MRCLK rise time			TBD
10	MRCLK fall time			TBD
	SERIAL DATA TIMING			
11	MCSEL low or high delay			TBD
12	RXD stable before RXCLK rising edge	TBD		
13	RXD stable after RXCLK falling edge	TBD		
14	RCV transition to RXCLK	TBD		
15	TXD transition to transition period		125	
	LOCK DETECT TIMING			
16	$\overline{\text{LOCKDET}}$ false after FMODE false (with valid data)	TBD		
17	$\overline{\text{LOCKDET}}$ true after FMODE false (with valid data)			TBD
18	$\overline{\text{LOCKDET}}$ false with loss of data			TBD

TABLE 3. 4 Mbps TIMING CHARACTERISTICS

T-75-49

NUMBER	PARAMETER	MIN	TYPICAL	MAX
	RXCLK TIMING			
1	RXCLK period		31.25	
2	RXCLK high time	TBD		
3	RXCLK low time	TBD		
4	RXCLK rise time			TBD
5	RXCLK fall time			TBD
	MRCLK TIMING			
6	MRCLK period	TBD	31.25	TBD
7	MRCLK high time	TBD	15.125	
8	MRCLK low time	TBD	15.125	
9	MRCLK rise time			TBD
10	MRCLK fall time			TBD
	SERIAL DATA TIMING			
11	MCSEL low or high delay			TBD
12	RXD stable before RXCLK rising edge	TBD		
13	RXD stable after RXCLK falling edge	TBD		
14	RCV transition to RXCLK	TBD		
15	TXD transition to transition period		31.25	
	LOCK DETECT TIMING			
16	$\overline{\text{LOCKDET}}$ false after FMODE false (with valid data)	TBD		
17	$\overline{\text{LOCKDET}}$ true after FMODE false (with valid data)			TBD
18	$\overline{\text{LOCKDET}}$ false with loss of data			TBD

TABLE 4. 16 Mbps TIMING CHARACTERISTICS

T-75-49

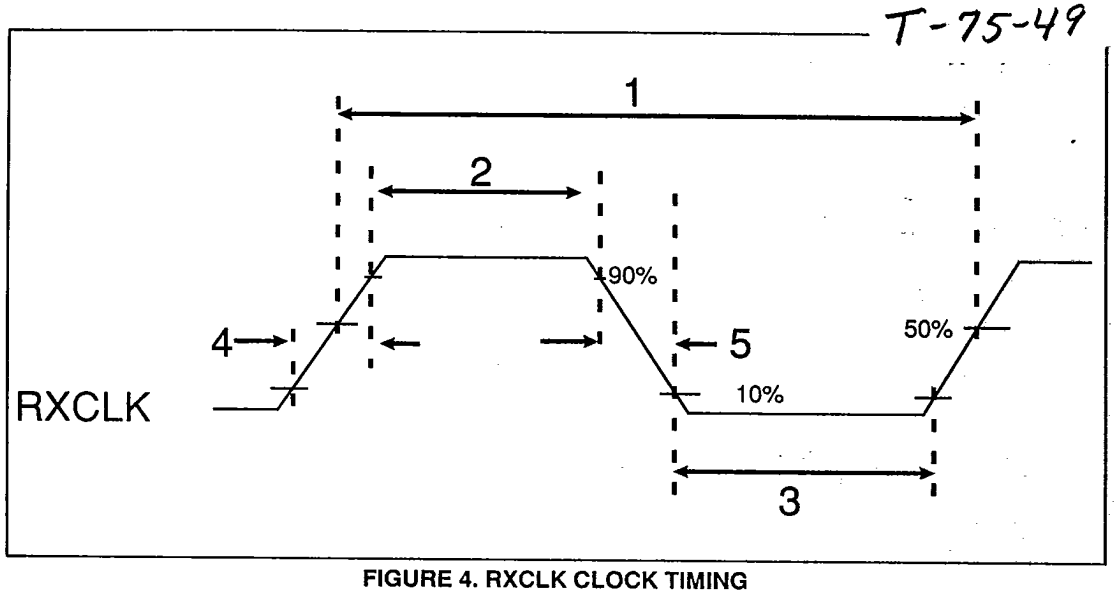


FIGURE 4. RXCLK CLOCK TIMING

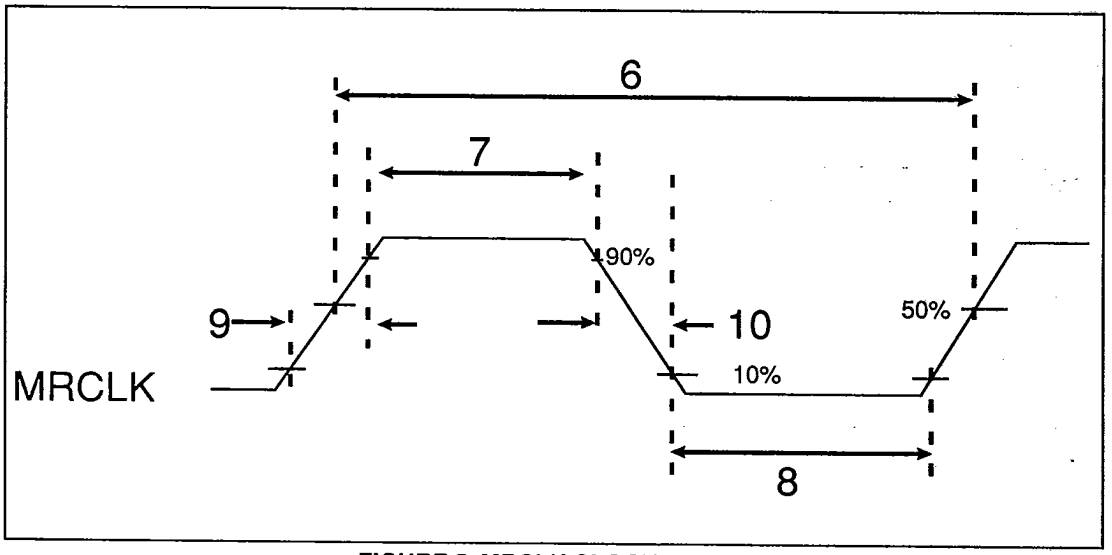
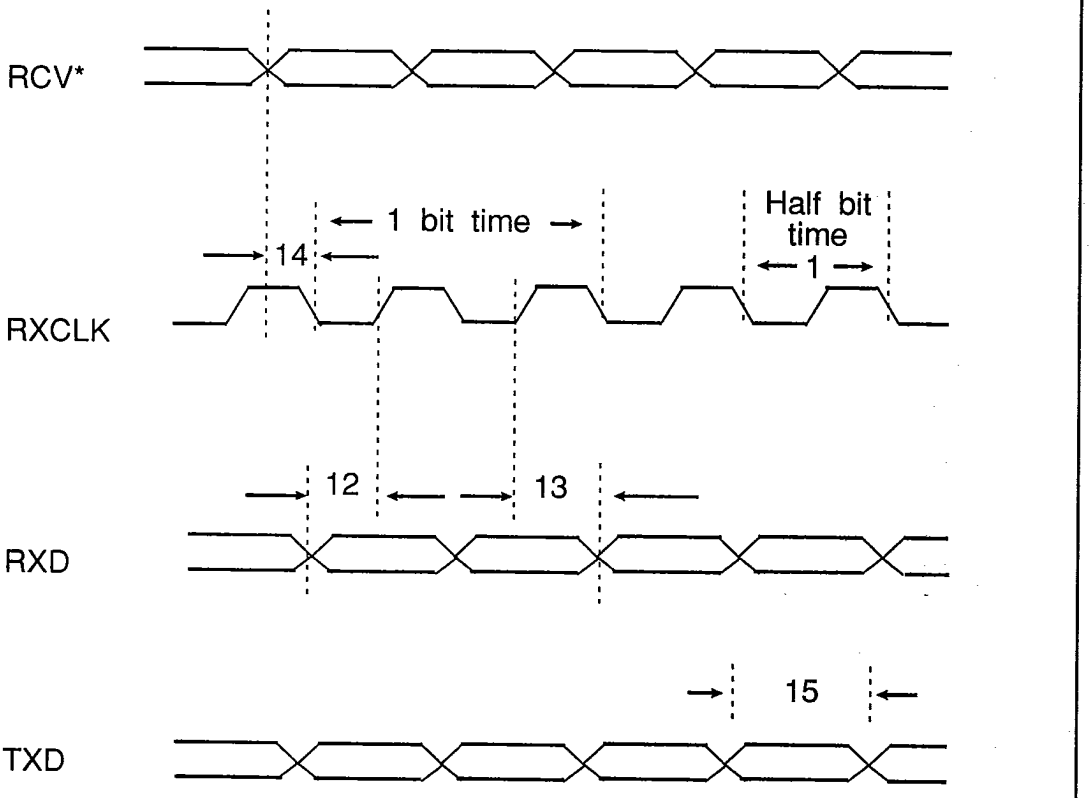


FIGURE 5. MRCLK CLOCK TIMING



*RCV is the differential signal (RCV16P-RCV16N) or (RCV4P-RCV4N).

FIGURE 6. SERIAL DATA TIMING

T-75-49

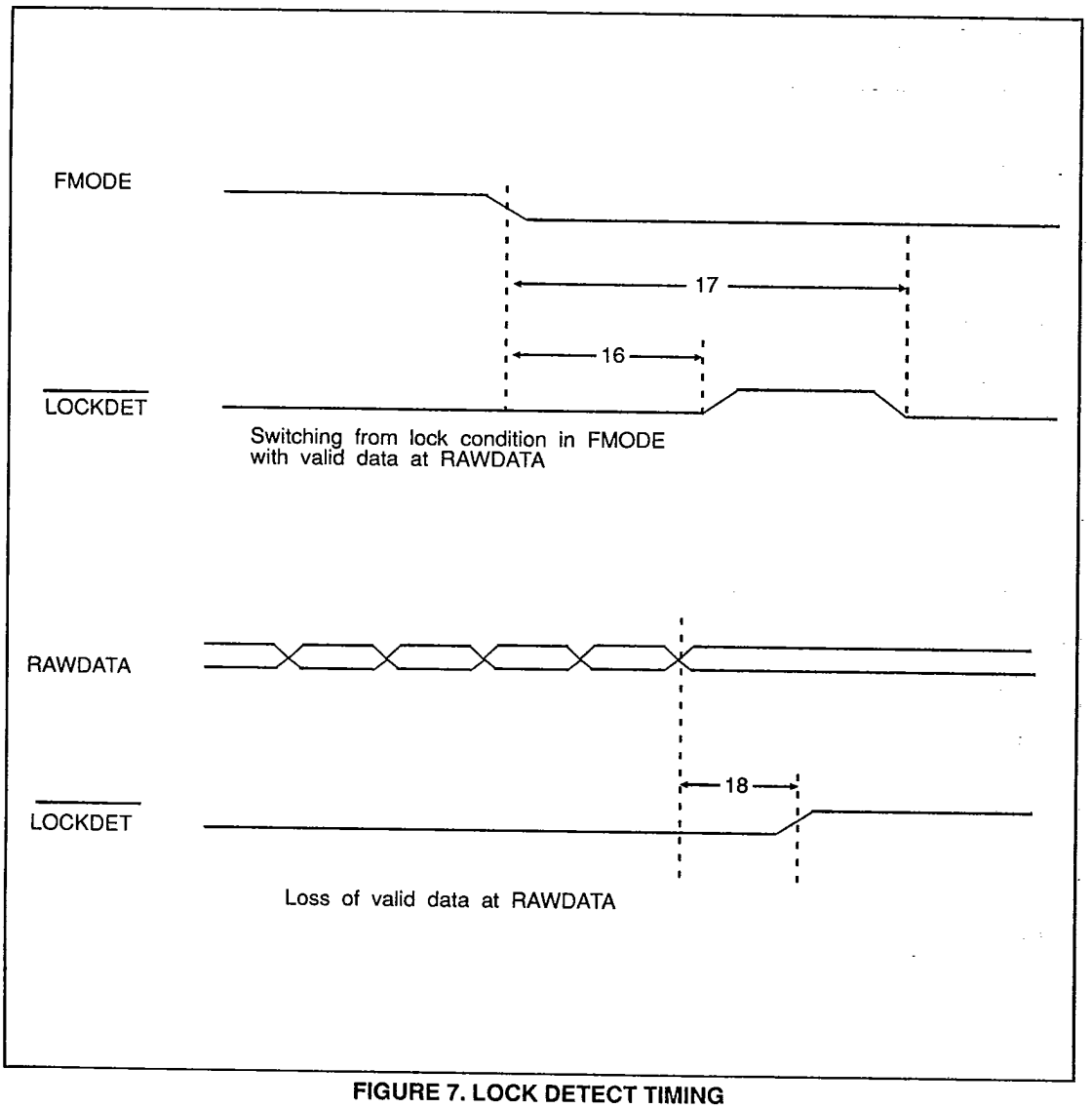


FIGURE 7. LOCK DETECT TIMING

T-75-49

6.0 ORDERING INFORMATION

Package Type: 28-Pin PLCC

Part Number: WD83C805JH00 02

6.1 PACKAGE DIMENSIONS

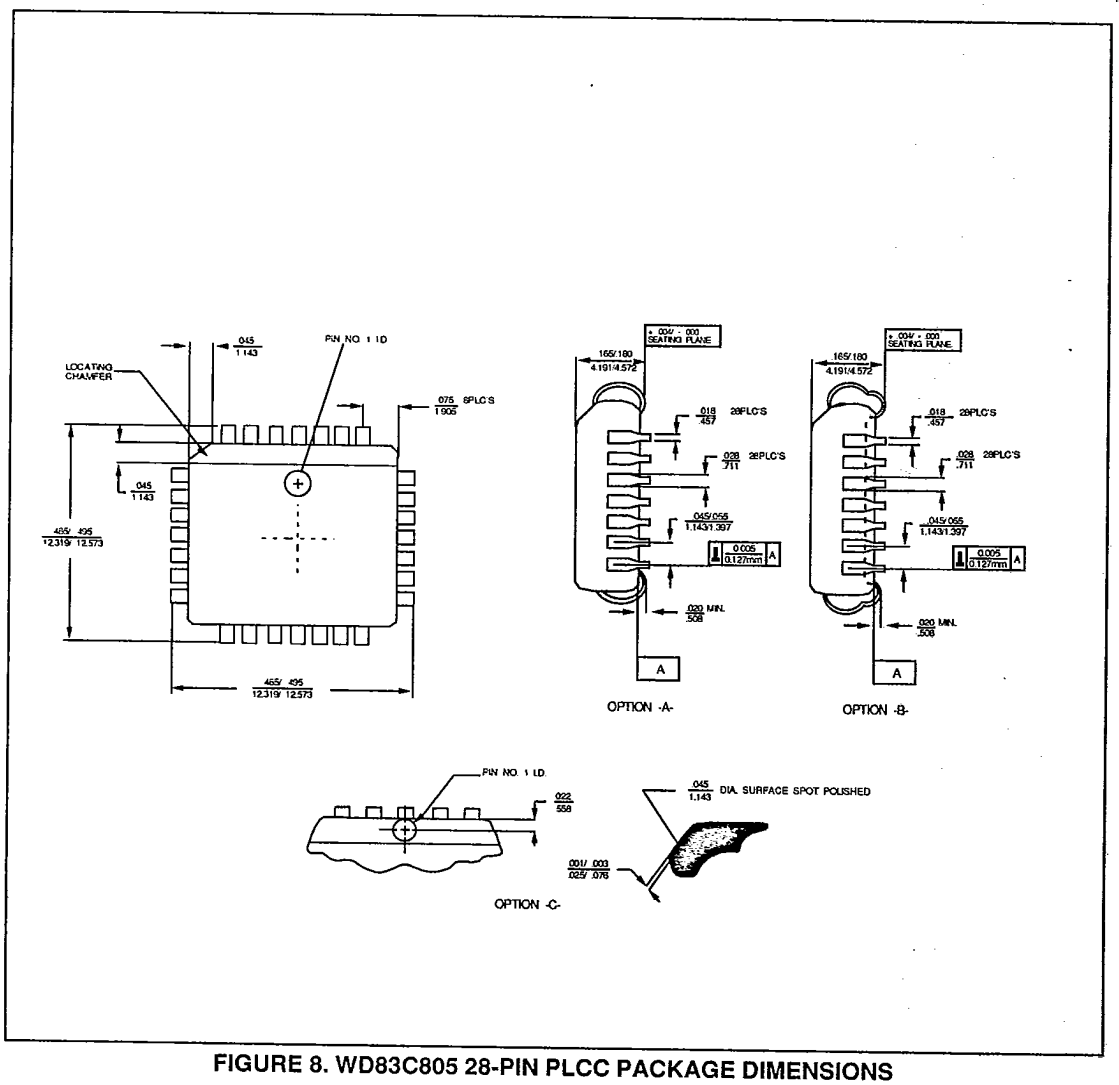


FIGURE 8. WD83C805 28-PIN PLCC PACKAGE DIMENSIONS

T-75-49

A APPENDIX 802.5 OVERVIEW

A.1 802.5 LAN Architecture

A Token Ring LAN consists of a set of stations connected serially by twisted pair transmission media, in which information is transferred bit by bit from one active station to the next. A station regenerates and repeats each bit, thus acting as a repeater when active. A station that has access to the media transfers information onto the ring where it circulates serially from one station to the next. A station recognizes its address and copies the information as it passes through the station. The source station is responsible for removing the information from the ring, preventing further circulation of the packet.

A.2 Signaling

The physical layer uses differential Manchester encoding to transmit and detect four different symbols: a binary 0, a binary 1, a nondata J, and a nondata K. The J and K symbols are violations of Manchester coding which are used for frame synchronization. The encoding of 0 or 1 is represented by the presence or absence of a transition at the beginning of the bit period, as opposed to the midbit transition, as is used in standard (nondifferential) Manchester encoding. A "1" is represented by the absence of a transition at the beginning of the interval. A "0" is represented with a transition at the beginning of the interval, ensuring sufficient zero-crossings for timing recovery. There is always a transition in the middle of the interval. The Manchester encoder/decoder logic is implemented on the TRC (WD83C825) device, so the TRI handles differential Manchester data (not NRZ data).

There is always one station on the ring which is designated as the "active monitor." Signal timing for the entire ring is provided by the active monitor; all other stations track the frequency and phase of this station. The token-ring protocol includes a mechanism for reconfiguring the ring to change the active monitor to another station, when required. Although the average signaling rate is controlled by the monitor, segments of the ring can instantly operate at speeds slightly higher or lower than the frequency of the monitor because of jitter. The active monitor includes a time delay mechanism called a latency buffer. This ±20 bit buffer compensates for the frequency and phase variations introduced into the ring by jitter.

The same generalized frame format is used for transmitting both MAC and LLC messages to the destination stations. The information field is optional and contains arbitrary binary data. The frame includes fields for a preamble, start delimiter, access and frame control, destination address, source address, data, frame check sequence (CRC), end delimiter, and frame status. The start and end delimiters are unique sequences (utilizing Manchester code violations) which provide frame synchronization. The token bit provides a mechanism by which access (transmission) to the ring is passed from one station to another. The token bit is imbedded in the access control octet. When a "free" token is recognized by the station, it inverts the token bit and modifies the rest of the packet, appending appropriate control and data fields to the bitstream "on the fly."

A.3 Wiring Scheme

Although the Token Ring is configured logically as a ring, it is wired physically in a hybrid ring/star configuration. This wiring configuration addresses an inherent flaw with the "ring" LAN topology. The flaw is that a single point of failure (a shorted or open wire anywhere) will bring the entire network down. With a star wired ring, the wiring to individual stations can be monitored for faults (shorts or opens) and dropped off the ring in the event of trouble. This wiring configuration makes the ring much more reliable.

The "ring" part ot the star/ring topology is comprised of the interconnections between the wiring closets on the network. Redundant links may be routed between the wiring closets to protect for failures of wiring on the main ring. The terminals are wired to the wiring closets in a "star" configuration. Relays in the wiring closet can "deinsert" (disconnect) individual stations from the logical ring merely by bypassing the station wiring.

A line interface unit (LIU) serves to interface each workstation to the network. A DC signaling scheme is used to allow the LIU host to attach and remove each station and its associated lobe wiring from the network, via electrical signaling

which is implemented in the WD83C825. The WD83C825 also serves to monitor for fault conditions on the local "lobe" of the network, and signals the host in the event of a wire fault condition. In the absence of a signal, the WD83C805 is switched to a "frequency reference" signal (MRCLK) to lock it to a local crystal oscillator. In the presence of a valid input signal, the internal PLL is switched to the incoming differential Manchester data and the PLL and phase-locks to the data waveform. The stable retimed clock from the PLL is used to recover incoming data and clock it off-chip to the companion WD83C825 token ring controller (TRC) device.

A.4 Station Attachment Scheme

A station is connected into the media via a local line interface unit (LIU) which consists of the hardware-level interface (TRI+TRC+host), a medium interface connector (MIC), and a medium interface cable. The 150 foot (average) media interface cable connects in the wiring closet to a trunk coupling unit (TCU). The TCU contains the relays and associated circuitry to couple the individual media interface cable in and out of the main ring.

The relay arrangement in the TCU is referred to as an "insertion/bypass mechanism." The relay is energized upon command from the TRI phantom drive signals "PHA and PHB" via a DC phantom drive technique. The connector that attaches the station hardware to the lobe is referred to as the Medium Interface Connector (MIC). The MIC provides a convenient reference point for signal levels, timing, etc. and is referred to often in the standards document. Physically the MIC may take the form of a 9-pin "D" connector or modular jack.

The TCU and MIC connectors and relays may contribute flat (non-distorting) attentuation to the medium between the TCU and the station.

A.5 Application Notes

See the figure on the next page for an application schematic diagram using the WD83C805 token-ring interface and the WD83C825 token-ring controller.

The receive path in the WD83C805 does not include equalization or multi-pole low pass filtering. These functions need to be provided external to the WD83C805 and can be optimized for a particular application. T-75-49

The inputs to pins 24-25 and 26-27 are normally biased to be centered around the voltage of the VCM pin. This voltage varies with changes of the internal circuit parameters. If the input differential voltage is greater than 100 to 200 mV worst case, it may be possible to set the DC level of the inputs to a fixed voltage between 2V and 4V. For best performance, the DC input level should be set to VCM. One method for doing this is to connect VCM to the center tap of a receive signal transformer and balance the DC load of any circuits between the transformer and WD83C805 receive inputs.

Pins 5-6 may be connected together to a single capacitor of 0.1μF. The tolerance is not critical to the PLL operation, as the high frequency filter capacitor of the PLL is internal to the TRI. If the loop damping characteristics need to be adjusted independently for each data rate, then two separate capacitors may be used. (If the cost and board area is not high, then this is the better alternative.) The other end of the capacitor(s) should be connected to the ground plane.

The printed circuit board must include separate ground and power planes with low inductance connections to the TRI pins or decoupling components. The planes should not be segmented near the token-ring interface unless necessary for FCC compliance. The MRCLK and control lines should be kept short and be kept separate from the receive input signal lines. Low ESR chip capacitors should be used for decoupling of +5V close to any noise sources. In general, good high frequency and digital printed circuit board design practices should be followed.

If the ground plane is low inductance and has good decoupling to the +5V supply (i.e., no long digital AC current paths), pins 1, 2, 15, and 22 may all be connected to the ground plane.

Pins 14 and 18 may be connected together with a decoupling capacitor placed close to the pins.

If the lowest jitter is needed, then pins 4 and 28 should not be connected together to +5V. Each

T-75-49

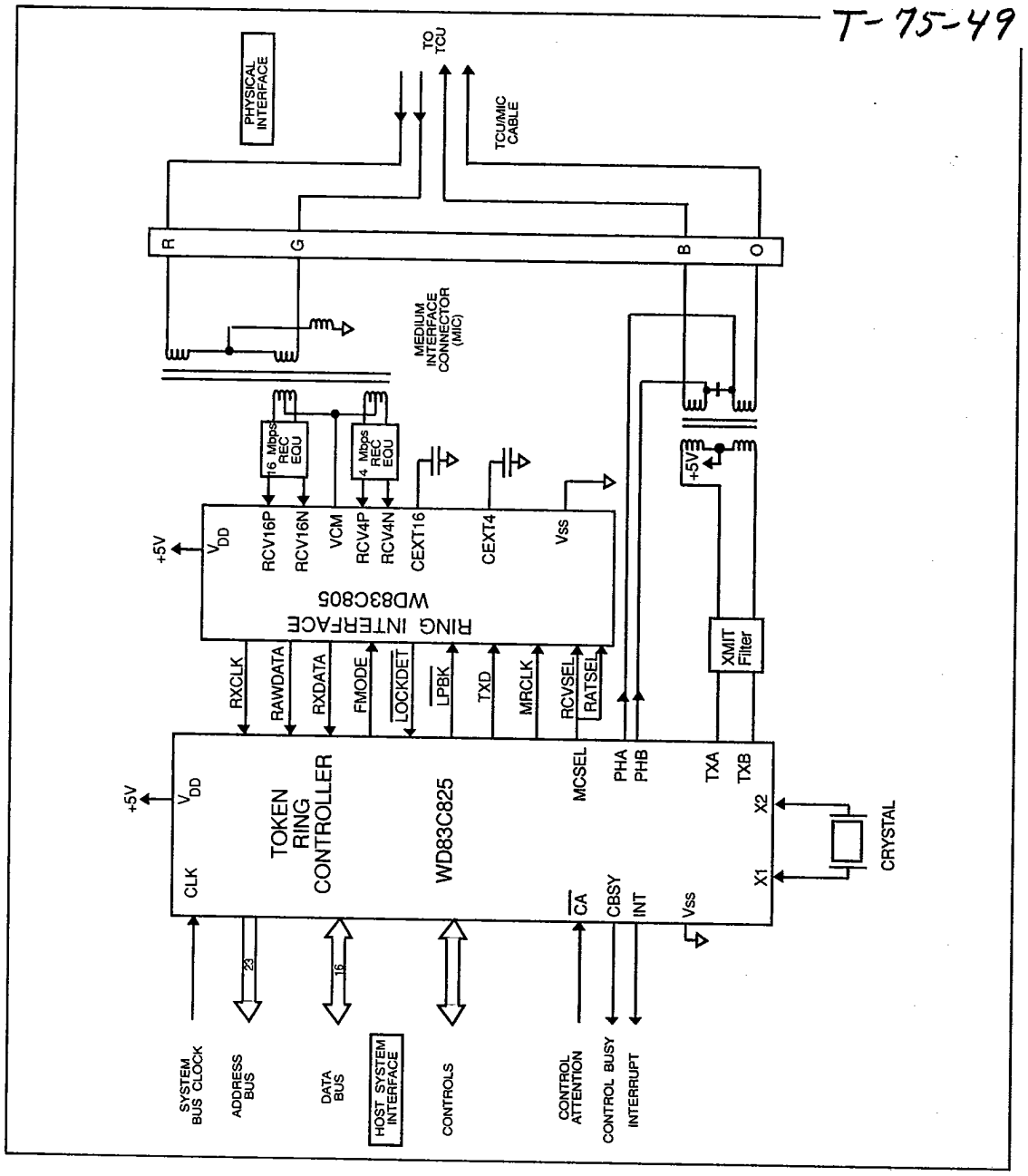


FIGURE 9. APPLICATION SCHEMATIC DIAGRAM

pin should connect to a separate 100 nF decoupling capacitor with a series impedance to the +5V. If the noise on the power supply is of high frequency only (approximately 10 MHz and greater), then a lossy ferrite bead inductor may be the best for a series impedance. If lower frequencies are present, then a small (approximately 10 Ohm) series resistor with a higher value capacitor is better.

See the WD83C805 pin description list for the use of other pin functions not covered in these notes.

A.6 Jitter

There are two types of jitter which occur on the network:

- systematic (data-correlated)
- random (non data-correlated)

Systematic jitter is dependent upon the data pattern. Systematic jitter grows roughly linearly around the token ring, while random jitter grows much more slowly. Random jitter grows roughly with the square root of the number of stations, because the random signal tends to cancel out as it accumulates.

Systematic jitter has been demonstrated to be the predominant problem. The major sources of systematic jitter include intersymbol interference in the transmission media, VCO output symmetry, and static phase offset in the PLL due to mismatches in the charge pump amplitude and timing.

The worst case phase tracking situation occurs when a long string of ones is followed by a long string of zeroes. Accumulated jitter is compensated by an elastic buffer in the active monitor. The buffer can only accommodate a limited amount of jitter. Jitter growth depends strongly on the damping parameter. If the damping parameter is not well-controlled, the cycle-slip rate will increase and the elastic buffer will overflow. The result will be an increase in bit errors (at best) and loss of ring synchronization (at worst). Factors which enter into control of the damping parameter include charge pump current, VCO gain, loop filter capacitance, and loop filter resistence.

The IEEE standard for the 4 Mbps ring requires a PLL acquisition time of 1.5 milliseconds maximum, which is 12,000 half-bit times. The acquisition process around the entire token ring is a non-linear phenomenon, which does not scale linearly with the number of stations. The individual stations must meet the required acquisition time, so that the token ring does not take an excessively long time to re-acquire after a station inserts or de-inserts on the ring.

A.7 Intersymbol Interference (ISI)

The twisted pair transmission medium is dispersive. As pulses travel through the medium they are not only attenuated, but also the higher frequency components of the signal are delayed less relative to the lower-frequency components. Thus, the pulses are spread over several signaling intervals. The function of the equalizer is to compensate for the distortion introduced by the transmission medium and shape the pulses into a form suitable for regeneration. It is impractical to restore the pulse to its original shape.