1.0 INTRODUCTION

The WD90C55 Color Interface Device provides the RGB data exchange interface between the Western Digital family of VGA flat-panel display controllers and a variety of LCD color display panels. The WD90C55 also acts as a pass-through buffer for LCD monochrome data.

This section provides an introduction to the WD90C55 and a list of features.

To order the WD90C55 Color Interface Device, use the following number:

90C55WM00

1.1 GENERAL DESCRIPTION

The WD90C55 supports laptop computers that use color or monochrome LCD panels. The WD90C55 interfaces with the following VGA flat-panel display controllers:

- WD90C20/WD90C20A
- WD90C22
- WD90C26/WD90C26A

With a VGA flat-panel display controller interface, the WD90C55 provides complete display support for laptop computers with either monochrome or color LCD displays (refer to Tables 1-1 and 1-2).The WD90C55 drives color LCD panels directly, without requiring additional buffers. Also, it can be used as output buffers to drive monochrome LCD panels.

Tables 1-1 and 1-2 show typical color LCD applications and number of colors available for each type.

1.2 FEATURES

The major features of the WD90C55 are listed below.

- Direct interface with WD90C20, WD90C22, WD90C20A, WD90C26, and WD9026A VGA Flat-Panel Display Controllers
- Power down mode control to reduce power consumption
- I/O pin mapping to improve board level testability
- 8-bit (2 and 2/3 pixels) STN color LCD interface
- 16-bit (5 and 1/3 pixels) STN color LCD interface
- Timing adjustment for TFT color LCD panel
- Uses a 44-pin MQFP package

CONTROLLER TYPE PANEL TYPE	WD90C20	WD90C22	WD90C20A	WD90C26/ WD90C26A
STN Color LCD	with WD90C55	with WD90C55	with WD90C55	with WD90C55
Hitachi TFT	with WD90C55	with WD90C55	direct	direct
Sharp TFT	N/A	direct	direct	direct

TABLE 1-1 COLOR LCD IMPLEMENTATION

CONTROLLER TYPE PANEL TYPE	WD90C20	WD90C22	WD90C20A	WD90C26/ WD90C26A
STN Color LCD	512	4K or 256K	4K	4K or 256K
TFT Color LCD	512	512	512	512 or 27K

TABLE 1-2 COLOR CAPABILITY

2.0 ARCHITECTURE

The WD90C55 Color Interface Device provides the RGB data exchange between the Western Digital family of VGA flat-panel display controllers and a variety of LCD panels, including TFT and STN color panels. It also acts as a pass-through buffer for LCD monochrome data. The buffered LCD monochrome data and control signals from the VGA flat-panel display controllers are passed along to LCD monochrome panels. These interface functions are supported for the following five modes:

- STN 8-bit Color LCD mode
- STN 16-bit Color LCD mode
- TFT Color LCD for WD90C20
- TFT Color LCD mode for WD90C22
- LCD Monochrome mode

The following additional modes are also provided:

- Pin scan mode
- Output tri-state mode

The WD90C55 turns off any logic that is not required by the current mode, which is selected with the SEL[2:0] inputs.

The WD90C55 contains the following eight major functional modules:

- Sequencer - STN Interface
- Data Conversion Control - STN Interface
- Bi-Phase Clock Generator - STN Interface
- Power Down Control
- I/O Pin Mapping Control
- TFT Timing Control - TFT Interface
- Color Panel Interface
- Monochrome LCD Interface

Each of these modules is described in the following subsections and are illustrated in the functional block diagram provided in Figure 2-1.

2.1 SEQUENCER - STN INTERFACE

The sequencer provides the key timing control between a VGA flat-panel display controller and a color LCD panel. In STN color-LCD mode, the VGA flat-panel display controller sends out 6-bits (2-pixels) every shift clock. The shift clock (SCLK) is not free-running but toggling. It toggles only when the video data is valid. The WGTCLK line is used to qualify the valid data and to start the state machine in the sequencer.

2.2 DATA CONVERSION CONTROL - STN INTERFACE

Data Conversion Control provides both 6-bit to 8-bit and 6-bit to 16-bit data conversion.

Only one type of color LCD panel is enabled during the operation.

Unused logic is automatically turned off.

2.3 BI-PHASE CLOCK GENERATOR - STN INTERFACE

The Bi-phase Clock Generator is used to generate two-phase clock outputs XUCLK and XLCLK. These outputs are used in the 8-bit STN color LCD interface.

Eight-bit data is latched on the falling edges of XUCLK and XLCLK. Sixteen-bit data is latched on the falling edge of XLCLK.

2.4 POWER DOWN CONTROL

Power Down Control accepts the $\overline{\text{PDOWN}}$ input and generates the control signals to turn off the WD90C55 PCLK when the system goes into power down mode.

2.5 I/O MAPPING CONTROL

I/O Mapping Control allows the WD90C55 to enter a test mode where its pins are divided into logically connected groups of input and output pins. Each group can then be treated as a separate resistive path to check for open and shorted circuits within the group and between groups. For additional I/O Mapping information, refer to Section 4.

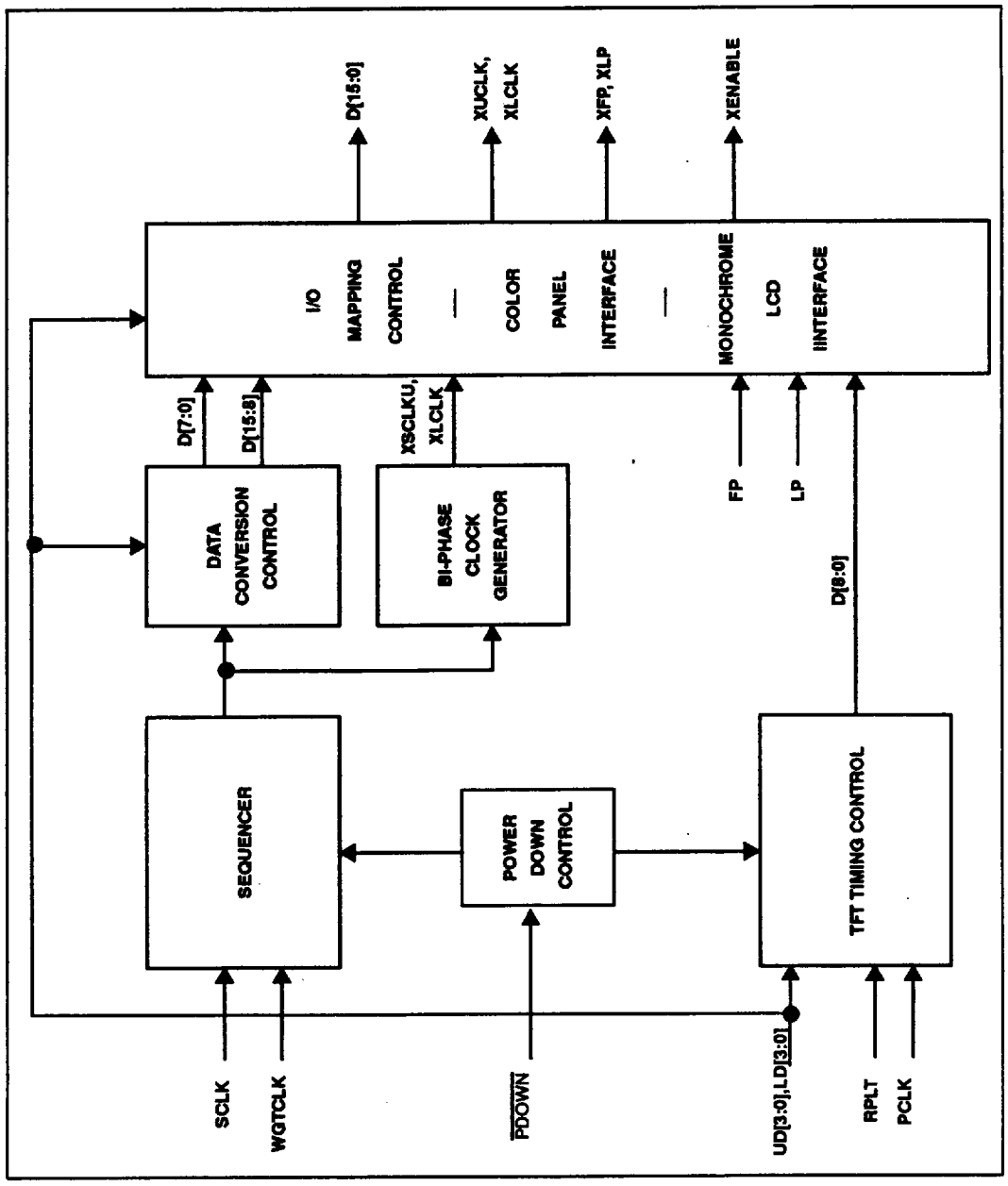

FIGURE 2-1 WD90C55 FUNCTIONAL BLOCK DIAGRAM

2.6 TFT TIMING CONTROL - TFT INTERFACE

Because the WD90C20 and WD90C22 controllers require different timing, the function of the TFT Timing Control is to adjust the timing to meet the Hitachi TFT Color LCD Panel specification. This adjustment consists of a 7 PCLK delay for the WD90C20 and 2 PCLK delay for the WD90C22.

The WD90C20A, WD90C26, and WD90C26A can drive the Hitachi TFT color LCD directly, without a WD90C55 interface.

Also, the WD90C22, WD90C20A, WD90C26, and WD90C26A can drive the Sharp TFT color LCD panel directly.

2.7 COLOR PANEL INTERFACE

The Color Panel Interface supports multiplexing of data onto the external data bus. The 8-bit STN data signals are multiplexed onto external data bus pins D[7:0], or the 16-bit STN data signals are multiplexed onto external data bus pins D[15:0].

The nine-bit TFT data signals R[2:0], G[2:0], and B[2:0] are multiplexed onto external data bus pins D[8:0], and the 8-bit monochrome LCD data signals are multiplexed onto external data bus pins D[7:0].

2.8 MONOCHROME LCD INTERFACE

In Monochrome LCD mode, input data UD[3:0], LD[3:0], and control signals for FP, LP, and SCLK, are multiplexed onto the color interface bus. These input data and control signals are buffered by the WD90C55 and passed through to a monochrome LCD panel. See Figure 2-2.

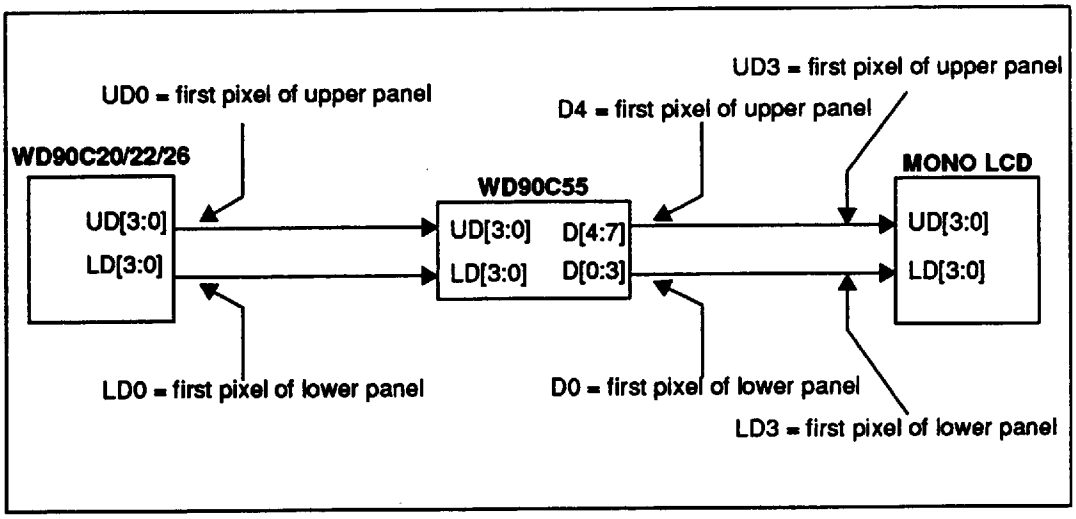

FIGURE 2-2 WD90C55 MONO LCD INTERFACE BLOCK DIAGRAM

3.0 SIGNAL DESCRIPTION

This section contains pin configuration information for the 44-pin WD90C55 device. Pin assignment tables and pin diagrams are provided.

- Pinout diagram
- Pin Number to Signal list
- Pin/Package Descriptions
- Bus Definition
- LCD Panel Pinout Specification

3.1 WD90C55 PINOUT

This section contains the following information:

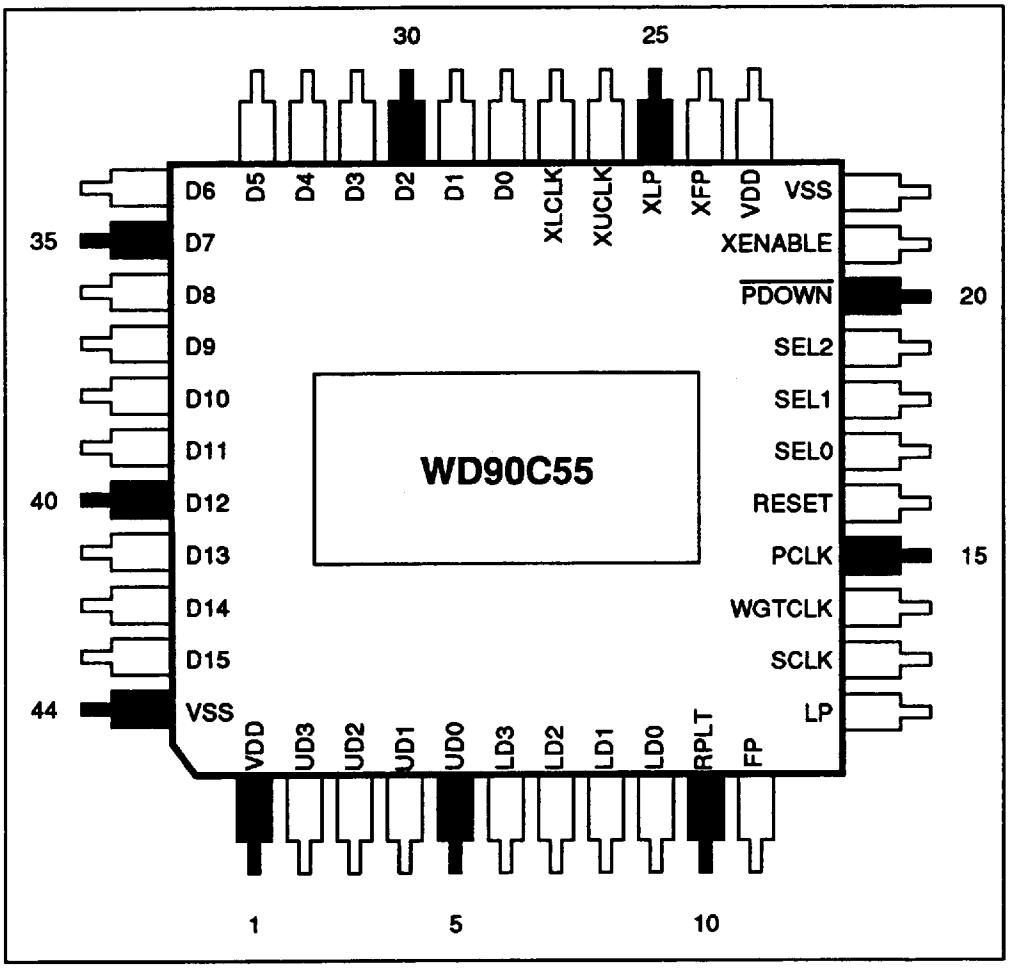

FIGURE 3-1 44-PIN MQFP PACKAGE PINOUT DIAGRAM

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	VDD	16	RESET	31	D3
2	UD3	17	SEL0	32	D4
3	UD2	18	SEL1	33	D5
4	UD1	19	SEL2	34	D6
5	UD0	20	$\overline{\text{PDOWN}}$	35	D7
6	LD3	21	XENABLE	36	D8
7	LD2	22	VSS	37	D9
8	LD1	23	VDD	38	D10
9	LD0	24	XFP	39	D11
10	RPLT	25	XLP	40	D12
11	FP	26	XUCLK	41	D13
12	LP	27	XLCLK	42	D14
13	SCLK	28	D0	43	D15
14	WGTCLK	29	D1	44	VSS
15	PCLK	30	D2	---	---

TABLE 3-1 WD90C55 PIN NUMBER TO SIGNAL LIST

PIN #	SIGNAL NAME	I/O	DESCRIPTION
1	VDD	I	Power (also pin 23)
2-5	UD[3:0]	I	Upper Panel Output data
6-9	LD[3:0]	I	Lower Panel Output data
10	RPLT	I	Data bit which is used for TFT interface
11	FP	I	Frame pulse
12	LP	I	Line Pulse
13	SCLK	I	Shift Clock
14	WGTCLK	I	Data enable
15	PCLK	I	Pixel Clock (free running)
16	RESET	I	System Reset
17-19	SEL[2:0]	I	WD90C55 Selection Bus (Refer to Section 3.2)
20	$\overline{\text{PDOWN}}$	I	Power Down Mode Control, active low
21	XENABLE	O	Data Enable
22	VSS		Power Return Ground (also pin 44)
23	VDD		Power (also pin 1)
24	XFP	O	Frame Pulse
25	XLP	O	Line Pulse
26	XUCLK	O	Upper Data Shift Clock
27	XLCLK	O	Lower Data Shift Clock
28-43	D[15:0]	O	LCD Panel Data Output
44	VSS		Power Return Ground (also pin 22)

TABLE 3-2 WD90C55 PIN/SIGNAL DESCRIPTIONS

3.2 SELECTION BUS

The logic level of each Selection Bus line is determined by an external resistor connected between its connector pin and VDD (pull up), or between its connector pin and VSS (pull down). At power-on, a pull up resistor causes the line to be read as a logic 1, and a pull down resistor causes the line to be read as a logic 0. For example, to select the 16-bit STN panel operation as listed in Table 3-3, pins 17 and 19 would be connected to pull down resistors, and pin 18 would be connected to a pull up resistor. All three pins must be connected to either an pull up or pull down resistor to select the operating mode. A typical value for either pull up or pull down resistors is 15 Kohms.

The Selection Bus is typically implemented through external switches or switching logic so that any logical combination can be easily selected. Although switching between operating modes may not be required in most applications, it is useful to switch between the normal operating mode and Test Mode 1 for test purposes (refer to Section 4-2).

SEL			OPERATING MODES
2	1	0	
0	0	0	Test Mode 1 I/O pin mapping, ICT test
0	0	1	8-Bit STN Panels (Sharp, Seiko)
0	1	0	16-Bit STN Panels (Sanyo)
0	1	1	Invalid. This logical combination is not used.
1	0	0	Monochrome LCD Panels
1	0	1	Hitachi TFT Color Panel (WD90C20)
1	1	0	Hitachi TFT Color Panel (WD90C22)
1	1	1	Test Mode 2, Output buffer tristate test
NOTE: The WD90C22 controller can drive the Sharp TFT color LCD directly without the WD90C55 device.			

TABLE 3-3 WD90C55 SELECTION BUS DEFINITION

WD90C55		LCD PANELS AND ASSOCIATED SIGNAL NAMES				
		MONO LCD	8-BIT STN (Seiko)	8-BIT STN (Sharp)	16-BIT STN (Sanyo/ Matsushita)	9-BIT TFT (Hitachi/ Sharp)
PIN NO.	SIGNAL NAME	SEL[2:0] =100	SEL[2:0] =001	SEL[2:0] =001	SEL[2:0] =010	SEL[2:0] =101 OR 110*
24	XFP	FP	DIN	YD	FLM	VSYNC
25	XLP	LP	LP	LP	CL1	HSYNC
21	XENABLE	UNUSED	UNUSED	UNUSED	UNUSED	DEN
11	FR	FR	UNUSED	UNUSED	M	UNUSED
26	XUCLK	XSCLK	XSCLU	XCKL	UNUSED	CLK
27	XLCLK	UNUSED	XCKLL	XCKU	CL2	UNUSED
43	D15	UNUSED	UNUSED	UNUSED	UD7	UNUSED
42	D14	UNUSED	UNUSED	UNUSED	UD6	UNUSED
41	D13	UNUSED	UNUSED	UNUSED	UD5	UNUSED
40	D12	UNUSED	UNUSED	UNUSED	UD4	UNUSED
39	D11	UNUSED	UNUSED	UNUSED	UD3	UNUSED
38	D10	UNUSED	UNUSED	UNUSED	UD2	UNUSED
37	D9	UNUSED	UNUSED	UNUSED	UD1	UNUSED
36	D8	UNUSED	UNUSED	UNUSED	UD0	B0
35	D7	UD3	D7	D0	LD7	R2
34	D6	UD2	D6	D1	LD6	R1
33	D5	UD1	D5	D2	LD5	R0
32	D4	UD0	D4	D3	LD4	G2
31	D3	LD3	D3	D4	LD3	G1
30	D2	LD2	D2	D5	LD2	G0
29	D1	LD1	D1	D6	LD1	B2
28	D0	LD0	D0	D7	LD0	B1
NOTE: SEL[2:0] = 101 for the WD90C20 and 110 for the WD90C22						

TABLE 3-4 WD90C55 TO LCD PANEL PINOUT SPECIFICATION

4.0 I/O MAPPING

This section provides the following information:

- A Description of WD90C55 I/O Mapping
- A list of I/O Mapping groups (Table 4-1)
- An I/O Mapping Group Diagram (Figure 4-2)

4.1 DESCRIPTION

The I/O Mapping allows the WD90C55 to enter a test mode where its pins are divided into groups of logically connected inputs and outputs. The path for each group goes from the input pin, through the WD90C55, and to the output pin. Each group can be treated as a separate resistive path to check for open and shorted circuits within the group and between groups. Table 4-1 lists each group (path) with its corresponding input and output pins.

Figure 4-1 provides a diagram of the I/O mapping groups (paths).

4.2 I/O MAPPING ENABLE

The I/O Mapping mode is enabled when the WD90C55 enters Test Mode 1. To enter Test Mode 1, the SEL[2:0] inputs are set to 000 by connecting external resistors from pins 17, 18, and 19 to VSS (ground).

To return the WD90C55 to normal operation, pins 17, 18, and 19 must be reconnected in their normal configuration. Refer to Section 3.2.

INPUT		OUTPUT	
PIN	NAME	PIN	NAME
2	UD3	43	D15
3	UD2	42	D14
4	UD1	41	D13
5	UD0	40	D12
6	LD3	39	D11
7	LD2	38	D10
8	LD1	37	D9
9	LD0	36	D8
10	RPLT	35	D7
16	RESET	34	D6
20	PDOWN	33	D5
19	SEL 2	36	D4
18	SEL1	31	D3
17	SEL0	30	D2
15	PCLK	29	D1
13	SCLK	28	DO

NOTES:

1. The following signal pins are not I/O mapped:
   11 (FP), 12 (LP), 14 (WGTCLK), 21 (XENABLE), 24 (XFP), 25 (XLP), 26 (XUCLK), and 27 (XLXLK).
2. The power pins 1 and 23 (VDD) and the power return pins 22 and 44 (VSS) are not I/O mapped.

TABLE 4-1 I/O MAPPING GROUPS

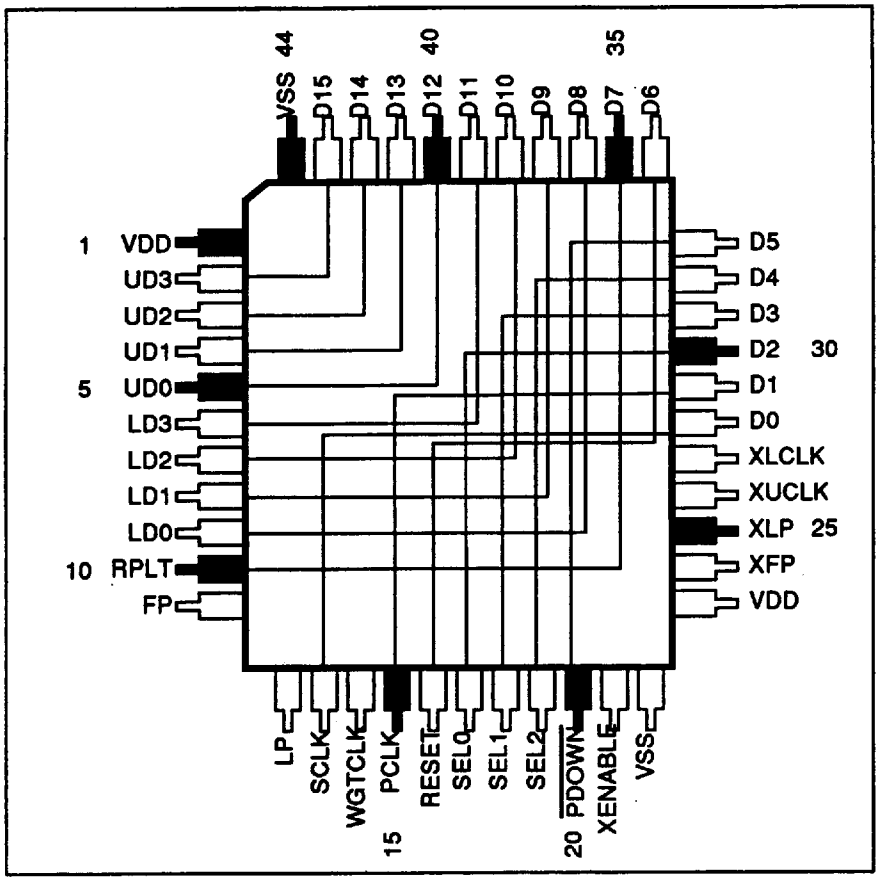

FIGURE 4-1 I/O MAPPING GROUP DIAGRAM

5.0 OPERATING ENVIRONMENT

The following table lists the absolute maximum ratings for the WD90C55 controller.

Package temperature range (operating)	0°C to 70°C
Storage Temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	V_{SS} -0.3 to 7 Volts
Maximum Power Dissipation	0.85 Watts
Electrostatic Discharge	700V Human Body Model
Latch up Threshold	+/- 100 mA
Maximum Input Current	+/- 20 mA

TABLE 5-1 ABSOLUTE MAXIMUM RATINGS

CAUTION

Stresses above those listed in the table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

5.1 STANDARD TEST CONDITIONS

The following characteristics apply to the standard test conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin.

Operating Temperature Range	0° to 70° C
Power Supply Voltage	4.75 to 5.25 Volts

6.0 DC ELECTRICAL CHARACTERISTICS

This section contains information about the DC electrical characteristics of the WD90C55. These characteristics define the minimum and maximum supply voltage and voltages on the input and output pins. Information is also provided about power consumption under typical conditions.

6.1 SUPPLY PINS

Table 6-1 lists the minimum and maximum supply voltage.

SUPPLY VOLTAGE	MIN	MAX	CONDITIONS
VDD	4.75V	5.25V	Pins 1, 23

TABLE 6-1 WD90C55 SUPPLY VOLTAGE

6.2 INPUT PINS

Table 6-2 lists the minimum and maximum DC voltage and current for the following input signal pins:

FP	$\overline{\text{PDOWN}}$	$\overline{\text{SEL}}$[2:0]
LD[3:0]	$\overline{\text{RESET}}$	UD[3:0]
LP	$\overline{\text{RPTL}}$	WGTCLK
PCLK	SCLK	

PARA-METER	MIN	MAX	CONDITIONS
VIL	-0.5V	0.8V	
VIH	2.0V	VCC +0.5V	
IIL	-10 µA	-10 µA	VIH = VCC, VIL = 0V
IDDS		100 µA	VIN=VCC or VSS, IOH=IOL=0mA

TABLE 6-2 WD90C55 INPUT PIN PARAMETERS

6.3 OUTPUT PINS

Table 6-3 lists the minimum and maximum DC voltage and current for the following output signal pins:

D[15:0] XENABLE XFP
XLCLK XLP XUCLK

PARAMETER	MIN	MAX	CONDITIONS
VOL		0.4V	IOL = 6 mA
VOH	2.4V		IOH = -6 mA
IOZ	-50 µA	50 µA	VOUT = VCC or VSS
C_{out}		100 pF	

TABLE 6-3 WD90C55 OUTPUT PIN PARAMETERS

6.4 TYPICAL POWER DOWN/NOMINAL POWER CONSUMPTION

Table 6-4 lists the typical power consumption in milliamperes (mA) and milliwatts (mW) for six common display modes:

DISPLAY MODE	NOMINAL		POWERDOWN	
	LOAD	NO LOAD	LOAD	NO LOAD
CRT	17.5/87.5	16.57/82.9	1.38/6.9	.02/100 µW
8-Bit Color STN (Sharp)	23.3/117	19.43/97.2	.02/100 µW	.02/100 µW
16-Bit Color STN (Sanyo)	27.88/139	19.13/95.7	.02/100 µW	.02/100 µW
9-Bit Color TFT[1] (Hitachi Simulation)	24.63/123	18.06/90.3	.04/200 µW	.04/200 µW
9-Bit Color TFT[2] (Hitachi Simulation)	28.30/142	17.60/88	1.46/7.3	.02/100 µW
Monochrome	18.68/93.4	16.16/80.8	.02/100 µW	.02/100 µW

NOTE:
1. For WD90C22 VGA Flat-Panel Display Controllers
2. For WD90C20 VGA Flat-Panel Display Controllers
3. All values are given in mA/mW unless otherwise specified.

TABLE 6-4 WD90C55 TYPICAL POWER CONSUMPTION

6.5 TYPICAL LOAD/NO-LOAD POWER CONSUMPTION

Table 6-5 lists the typical load/no load power consumption at typical PCLK frequencies

LCD TYPE	LCD/CRT FREQUENCY				COMMENT
	25 MHZ	28 MHZ	32 MHZ	IDLE	
8-Bit Color STN (Sharp)	30.5 mA/ 19.5 mA	33.7 mA/ 22.1 mA	38.1 mA/ 24.9 mA	24.6 mA/ 19.6 mA	Tested at 80 columns, 34 rows
16-Bit Color STN (Sanyo)	27.3 mA/ 18.7 mA	30.4 mA/ 20.9 mA	34.1 mA/ 23.6 mA	22.8 mA/ 19.1 mA	Tested at 80 columns, 34 rows
9-Bit Color TFT (Hitachi)	19.2 mA/ 17.6 mA	21.4 mA/ 19.6 mA	24.2 mA/ 22.2 mA	20.3 mA/ 18.7 mA	Tested at 80 columns, 34 rows
NOTE: The typical load/no-load values are given in milliamperes (mA) unless other wise specified.					

TABLE 6-5 TYPICAL LOAD/NO-LOAD POWER CONSUMPTION

7.0 AC OPERATING CHARACTERISTICS

Timing is provided for the following:

- STN Color LCD Mode - Input Timing
- STN Color LCD Mode - 8-bit interface
- STN Color LCD Mode - 16-bit interface
- TFT Color LCD Mode - 9-bit interface
- Mono LCD Mode

NOTE

Throughout this section, the minimum (MIN) and maximum (MAX) values are given in nanoseconds (ns) unless otherwise specified.

ITEM	DESCRIPTION	MIN	MAX
1	Rise/Fall Time (Inputs: PCLK SCLK FP LP WGTCLK		5 10 10 10 10
2	UD[3:1], LD[3:1] setup to ⇓ SCLK	18	
3	UD[3:1], LD[3:1] hold from ⇓ SCLK	18	
4	UD[3:1], LD[3:1] valid from ⇑ WGTCLK	10	
5	UD[3:1], LD[3:1] invalid from ⇓ WGTCLK	-10	
6	SCLK period	62.5 (PCLK = 32 MHz)	80 (PCLK = 25 MHz)
7	FP ⇑ to LP ⇓ SETUP time	1 LP[1]	
8	FP ⇓ to LP ⇓ HOLD time		0

NOTE:
1. $LP = 1/_{PCLK} \cdot 800$
2. See Figure 7-1.

TABLE 7-1 STN COLOR LCD MODE - INPUT TIMING

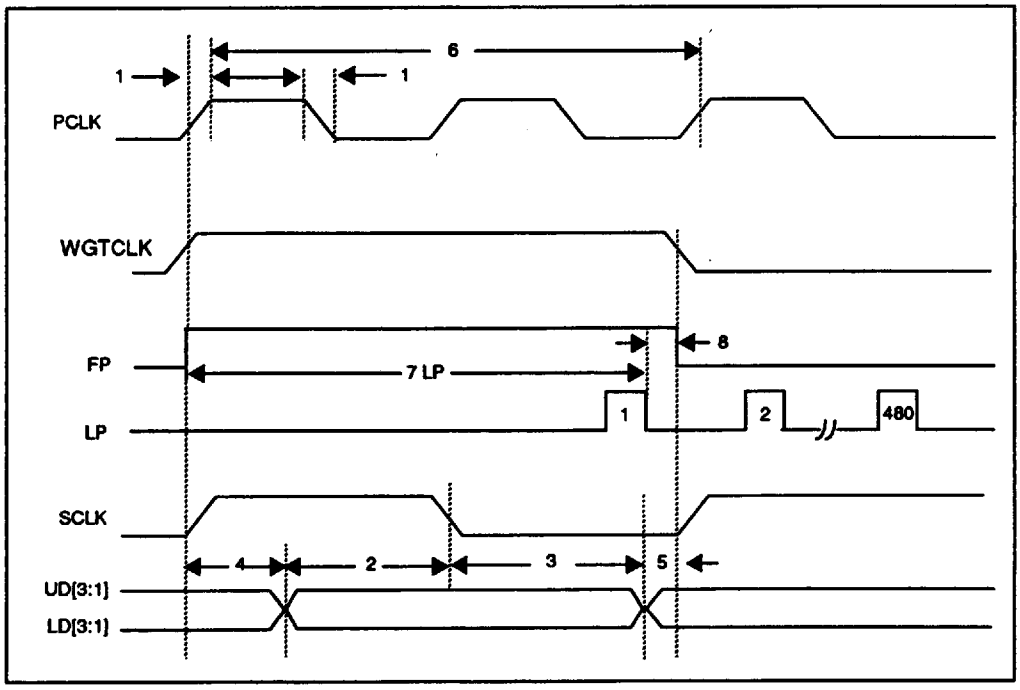

FIGURE 7-1 STN COLOR LCD MODE - INPUT TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	XFP⇓ to XLP⇓ Hold time	24 PCLK	32 PCLK
2	XFP ⇑ to XLP ⇑ Setup time		1 LP[1]
3	⇑ SCLK to ⇑ XUCLK		240
4	⇑ SCLK to ⇑ XLCLK		345
5	D[7:0] (even byte) setup to XUCLK ⇓ or setup to XLCLK ⇓	30 @ t=32 MHz 35 @ t=28 MHz 40 @ t=25 MHz	
6	D[7:0] (odd byte) hold from XUCLK⇓ or hold from XLCLK⇓	30 @ t=32 MHz 35 @ t=28 MHz 40 @ t=25 MHz	
7	XUCLK cycle time	163	218
8	XLCLK cycle time	165	205

NOTE:
1. $LP = 1/_{PCLK} \cdot 800$
2. See Figure 7-2.

TABLE 7-2 STN COLOR LCD MODE - 8-BIT INTERFACE

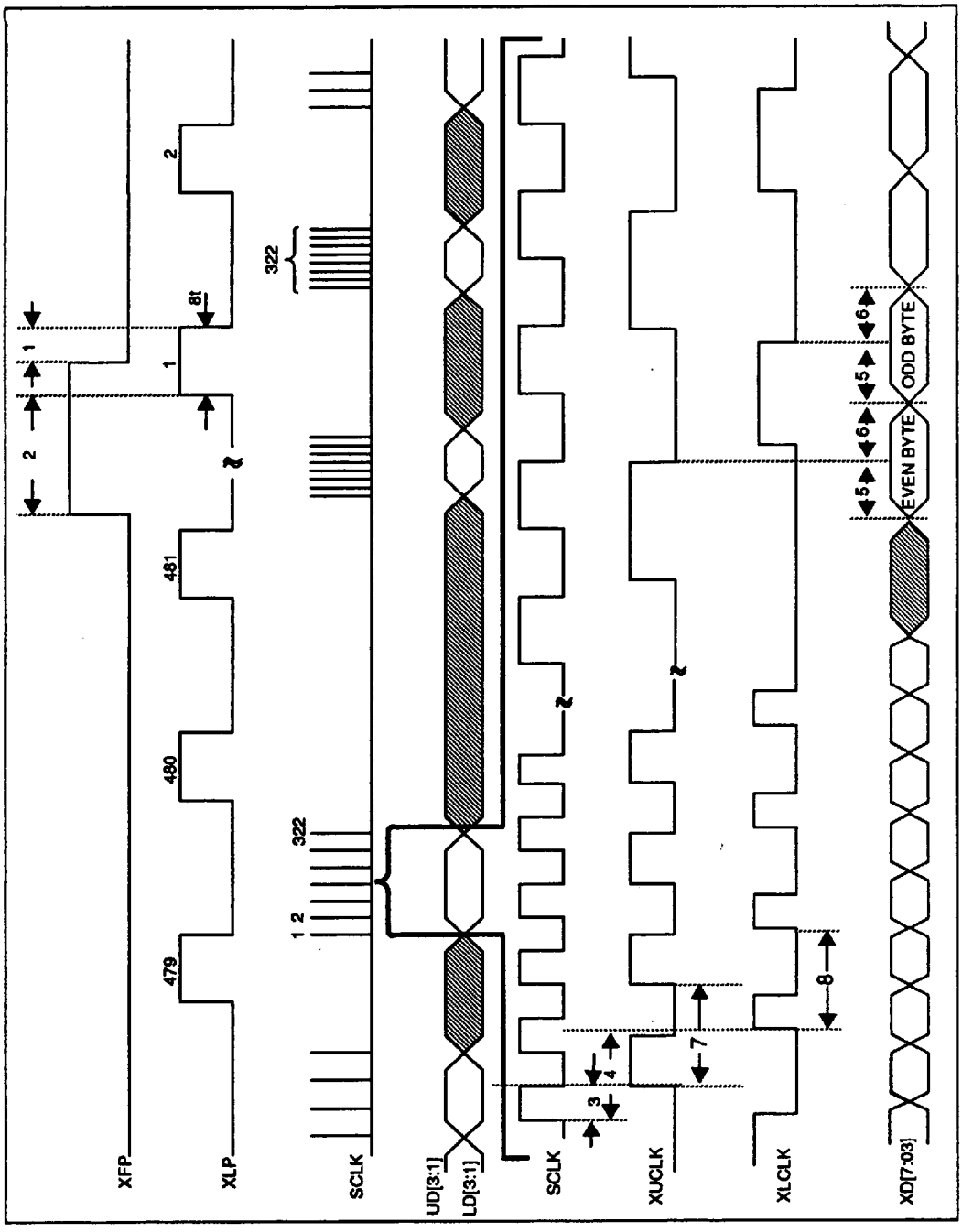

FIGURE 7-2 STN COLOR LCD 8-BIT INTERFACE MODE TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	XFP ⇑ to XLP ⇑ Hold time	24 PCLK	32 PCLK
2	XFP⇓ to XLP⇓ Setup time		1 LP[1]
3	D[15:0] setup to XLCLK ⇓	30 @ t=32 MHz 35 @ t=28 MHz 40 @ t=25 MHz	
4	D[15:0] hold to XLCLK ⇑	30 @ t=32 MHz 35 @ t=28 MHz 40 @ t=25 MHz	

NOTE:
1. $LP = 1/_{PCLK} \cdot 800$
2. See Figure 7-3.

TABLE 7-3 STN COLOR LCD MODE - 16-BIT INTERFACE

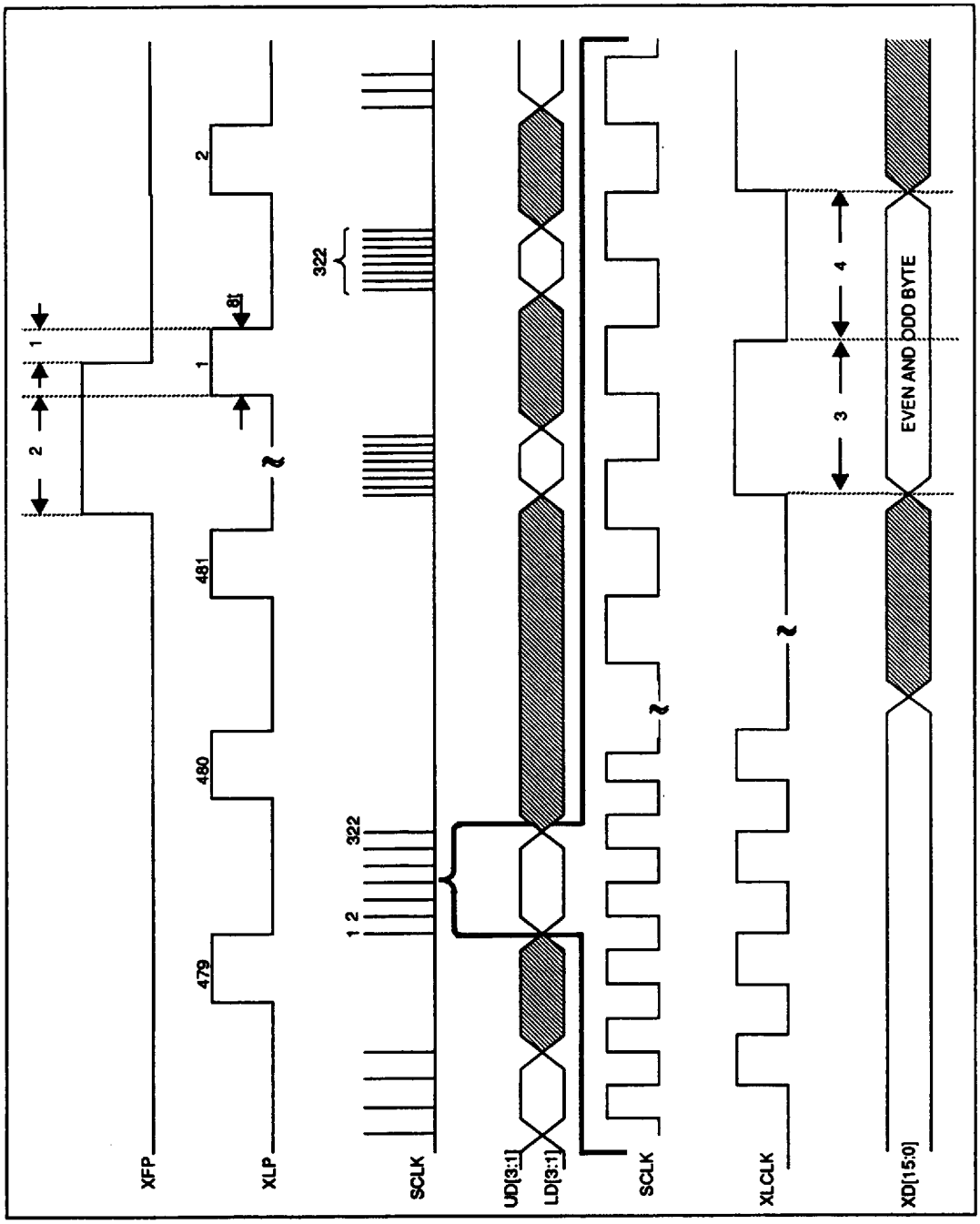

FIGURE 7-3 STN COLOR LCD 16-BIT INTERFACE MODE TIMING DIAGRAM

ITEM	DESCRIPTION	MIN	MAX
1	Data IN [8:0] setup to PCLK ⇓	10	
2	Data IN [8:0] hold from PCLK⇓	10	
3	D[8:0] setup to XUCLK ⇓(WD90C22) PCLK=25 MHz	10	
4	D[8:0] hold from XUCLK ⇓(WD90C22) PCLK=25 MHz	10	
5	D[8:0] setup to XUCLK ⇓ (WD90C20) PCLK=25 MHz	10	
6	D[8:0] hold from XUCLK ⇓ (WD90C20) PCLK=25 MHz	10	
NOTE: See Figure 7-4.			

TABLE 7-4 TFT COLOR LCD MODE - 9-BIT INTERFACE

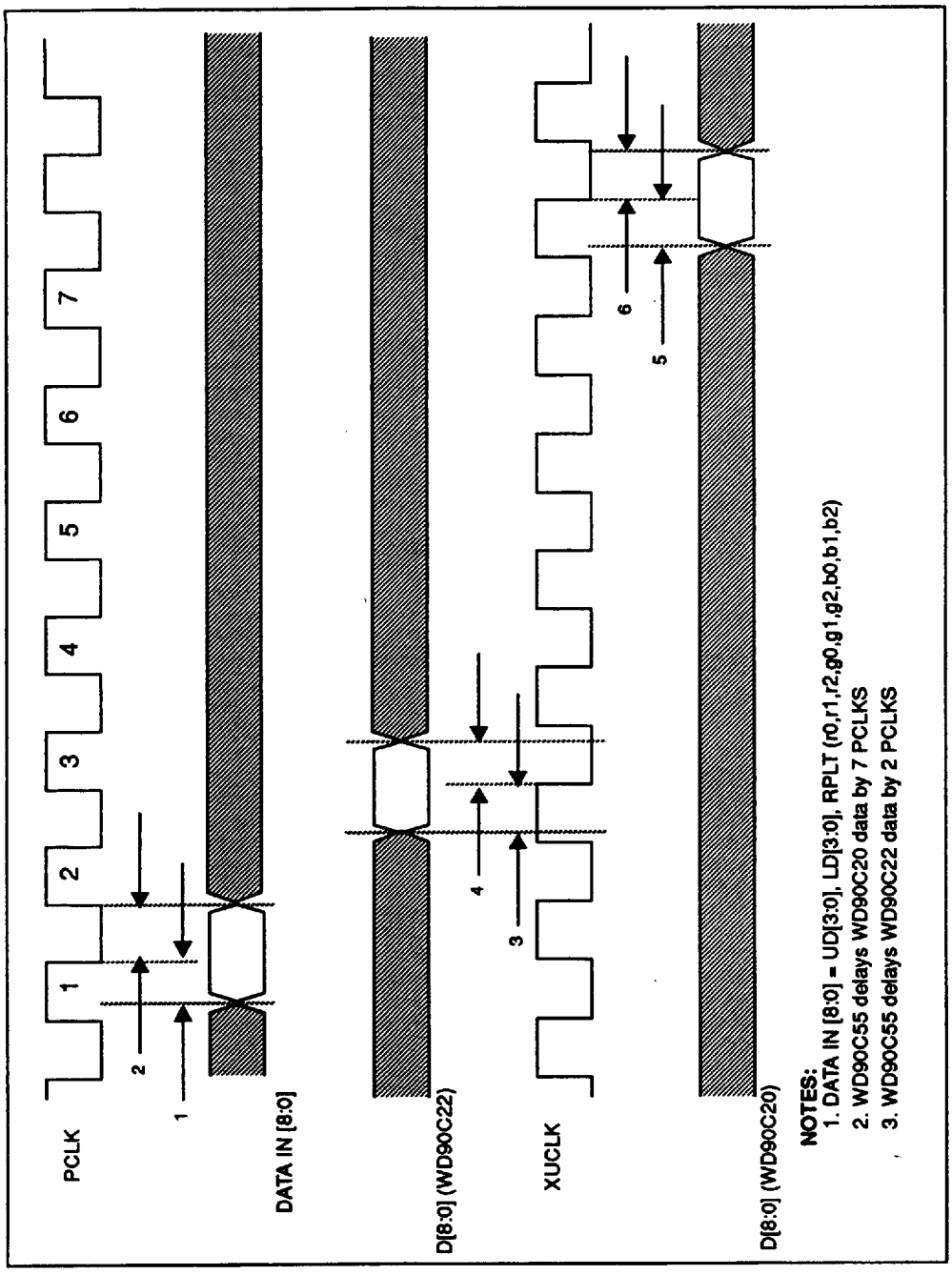

FIGURE 7-4 TFT COLOR LCD 9-BIT INTERFACE MODE TIMING DIAGRAM

8.0 APPLICATIONS

This section provides block diagrams of the WD90C55 device connected to support the following VGA Flat-Panel Display Controllers:

- WD90C20
- WD90C20A
- WD90C22
- WD90C26 and WD90C26A

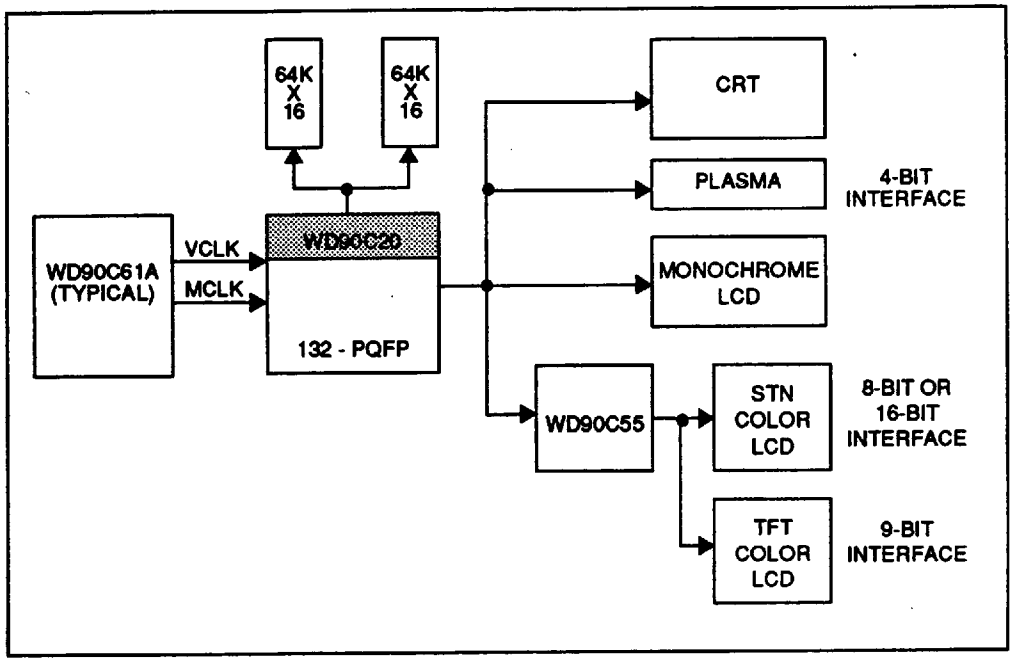

FIGURE 8-1 WD90C55 WITH A WD90C20 VGA FLAT-PANEL DISPLAY CONTROLLER

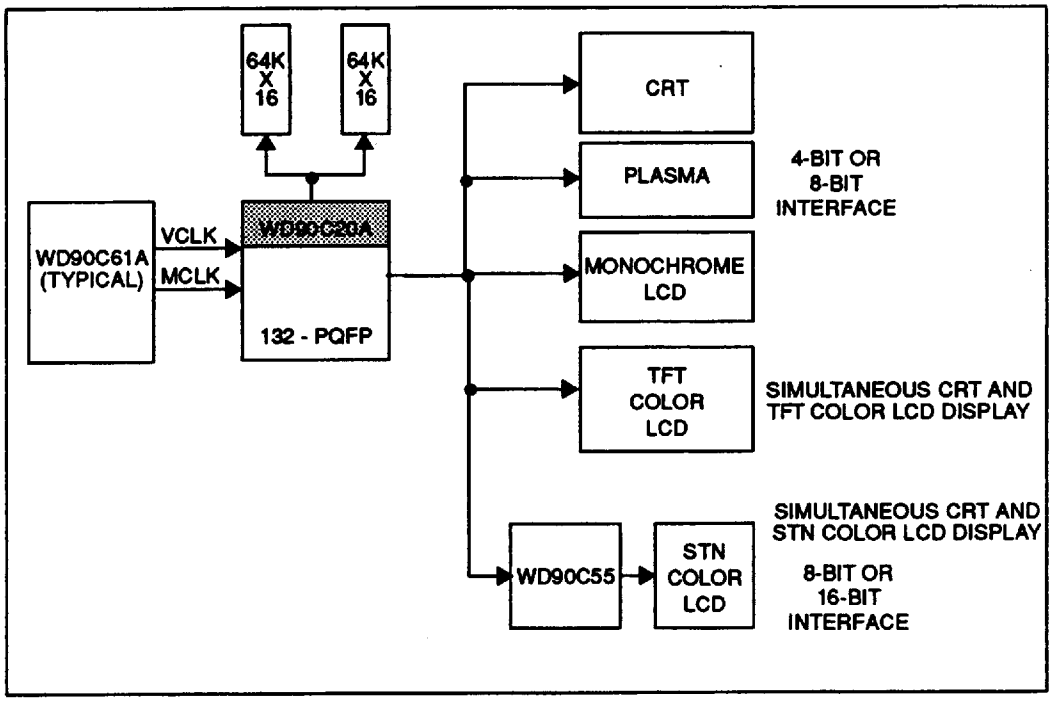

FIGURE 8-2 WD90C55 WITH A WD90C20A VGA FLAT-PANEL DISPLAY CONTROLLER

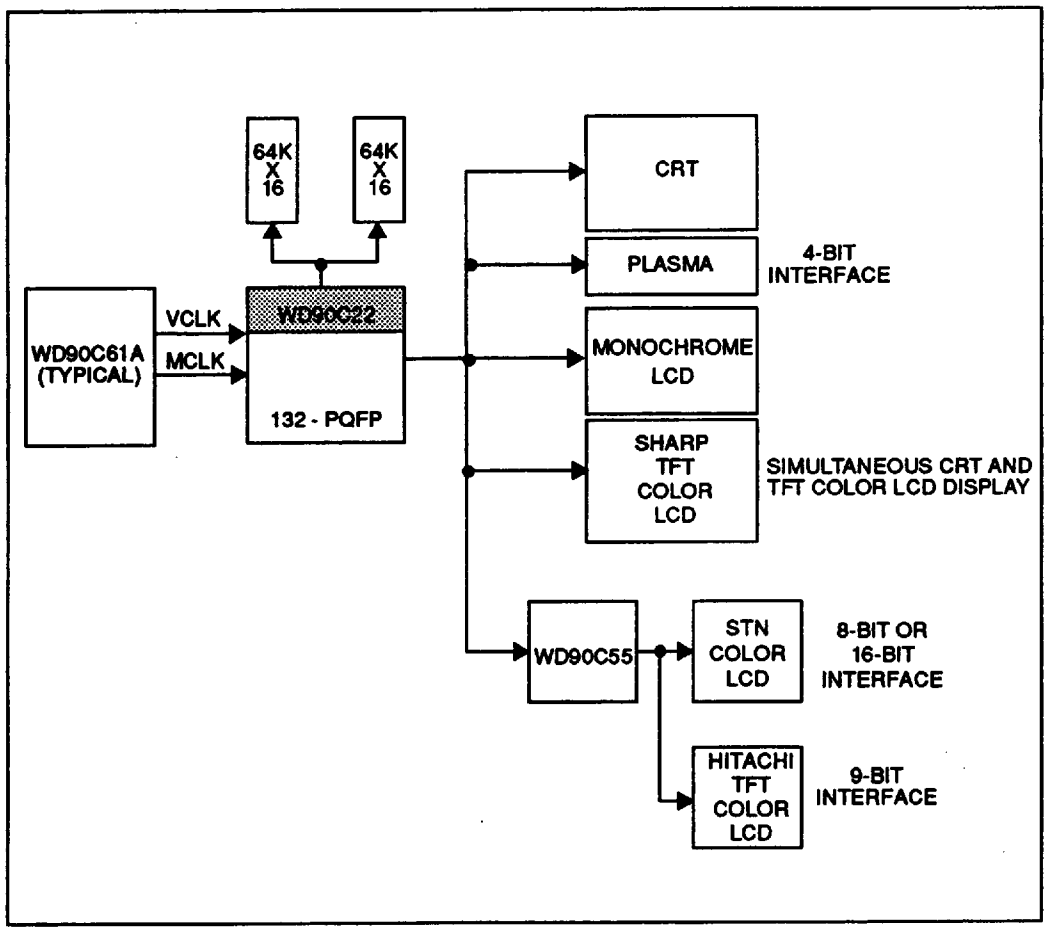

FIGURE 8-3 WD90C55 WITH A WD90C22 VGA FLAT-PANEL DISPLAY CONTROLLER

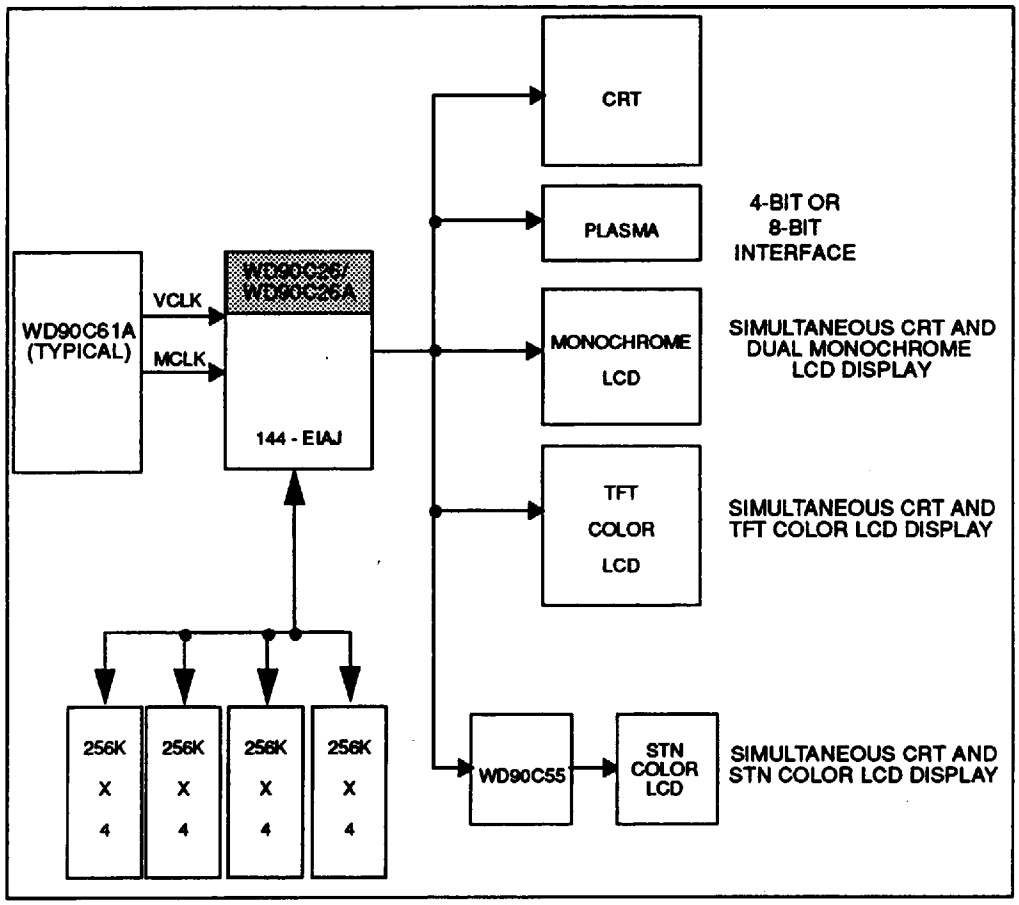

FIGURE 8-4 WD90C55 WITH A WD90C26/WD90C26A VGA FLAT-PANEL DISPLAY CONTROLLER

9.0 MECHANICAL SPECIFICATIONS

Figure 9-1 contains the mechanical specifications for WD90C55 44-pin MQFP package.

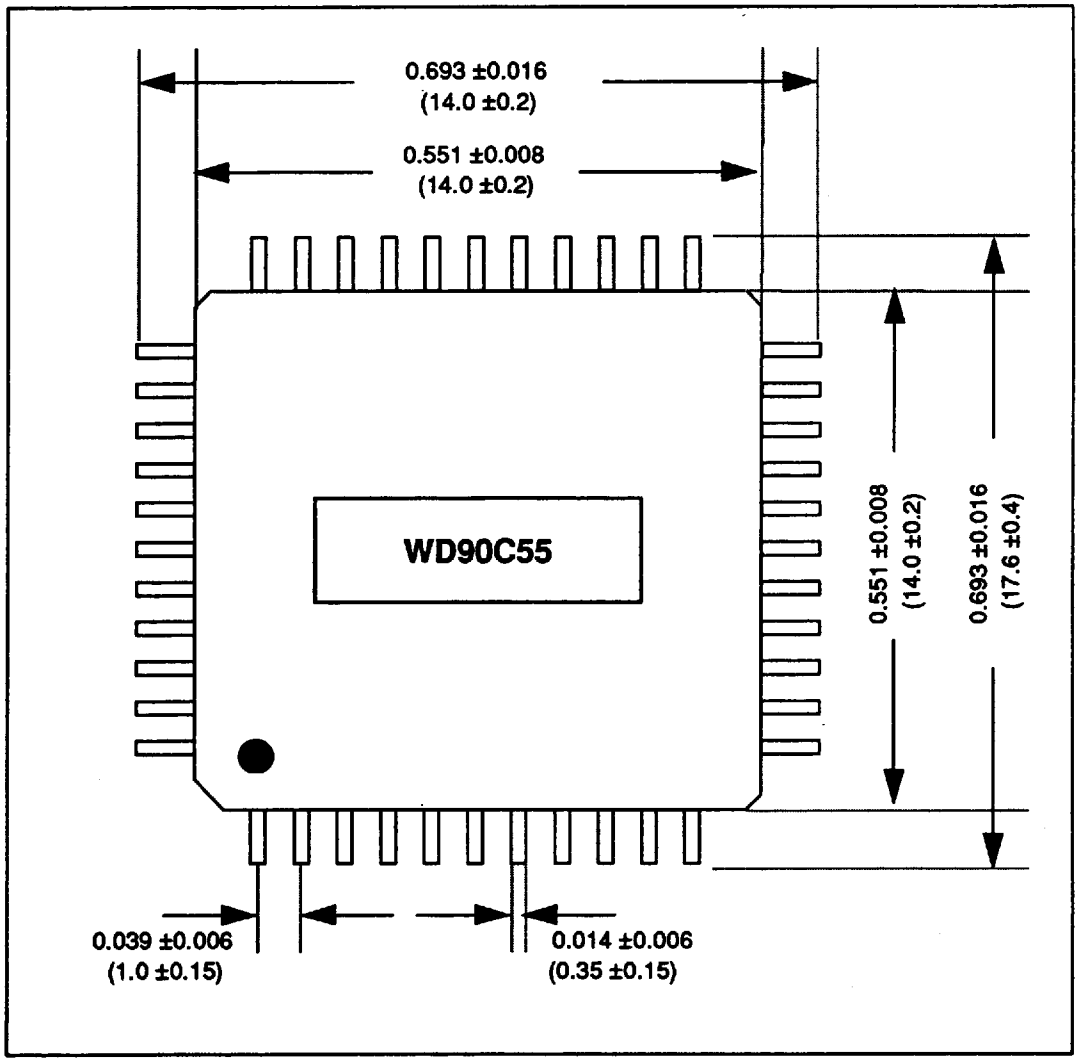

FIGURE 9-1 44-PIN MQFP MECHANICAL SPECIFICATION