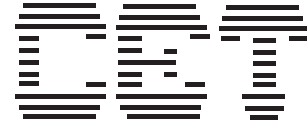


CED61A3/CEU61A3



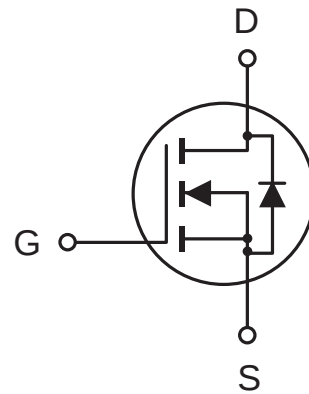
Jan. 2003

N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

6

- 30V , 40A , $R_{DS(ON)}=13.5m\Omega$ @ $V_{GS}=10V$.
 $R_{DS(ON)}=20m\Omega$ @ $V_{GS}=4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous -Pulsed	I_D	40	A
	I_{DM}	120	A
Drain-Source Diode Forward Current	I_S	40	A
Maximum Power Dissipation @ $T_c=25^{\circ}C$ Derate above $25^{\circ}C$	P_D	50	W
		0.4	W/ $^{\circ}C$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}C$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^{\circ}C/W$

CED61A3/CEU61A3

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V			1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
ON CHARACTERISTICS ^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D 250μA	1		3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		11	13.5	mΩ
		V _{GS} = 4.5V, I _D = 18A		16.5	20	mΩ
On-State Drain Current	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	40			A
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 26A		34		S
DYNAMIC CHARACTERISTICS ^b						
Input Capacitance	C _{ISS}	V _{DS} =15V, V _{GS} = 0V f =1.0MHz		1200		pF
Output Capacitance	C _{OSS}			480		pF
Reverse Transfer Capacitance	C _{RSS}			130		pF
SWITCHING CHARACTERISTICS ^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 15V, I _D = 40A, V _{GS} = 10V R _{GEN} =24Ω		18	30	ns
Rise Time	t _r			25	50	ns
Turn-Off Delay Time	t _{D(OFF)}			45	90	ns
Fall Time	t _f			75	130	ns
Total Gate Charge	Q _g	V _{DS} = 15V,I _D = 40A V _{GS} = 5V		19	23	nC
Gate-Source Charge	Q _{gs}			5		nC
Gate-Drain Charge	Q _{gd}			9		nC

CED61A3/CEU61A3

ELECTRICAL CHARACTERISTICS (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS^a						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 26A		0.9	1.3	V

6

Notes

a. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

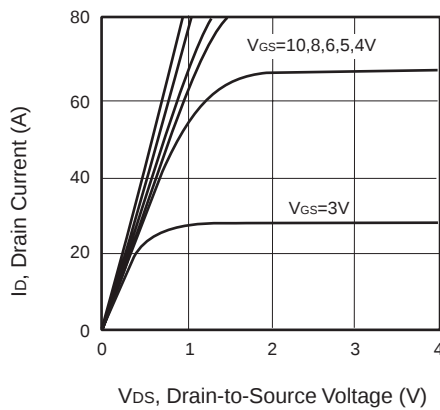


Figure 1. Output Characteristics

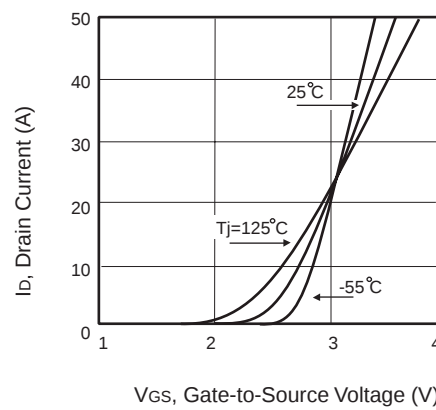


Figure 2. Transfer Characteristics

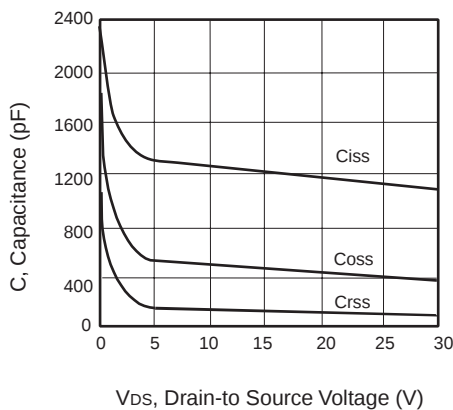


Figure 3. Capacitance

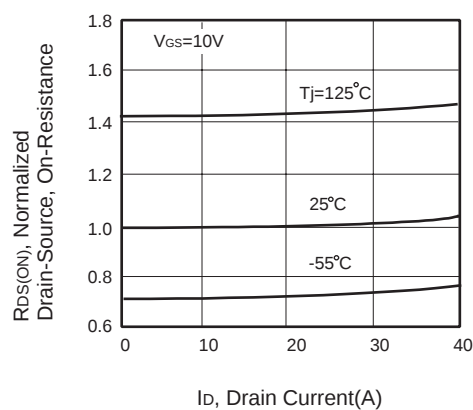


Figure 4. On-Resistance Variation with Drain Current and Temperature

CED61A3/CEU61A3

6

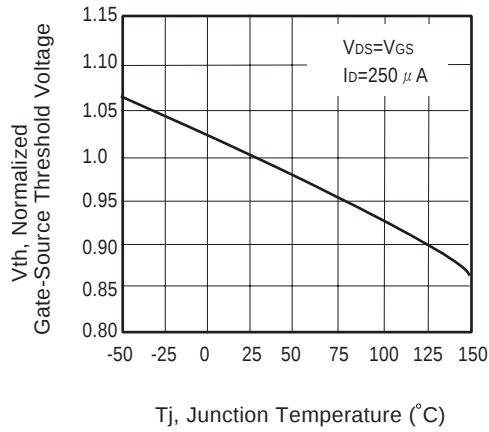


Figure 5. Gate Threshold Variation with Temperature

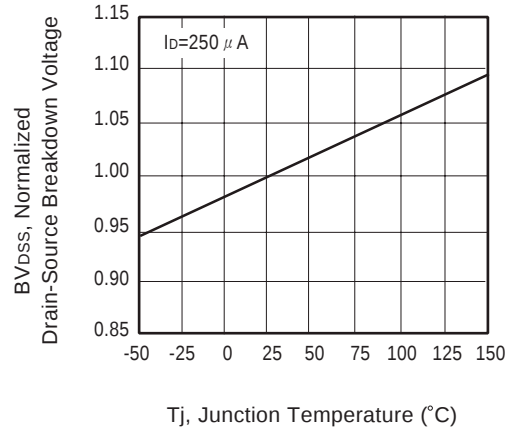


Figure 6. Breakdown Voltage Variation with Temperature

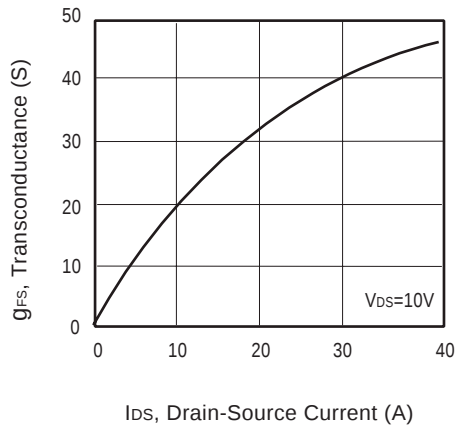


Figure 7. Transconductance Variation with Drain Current

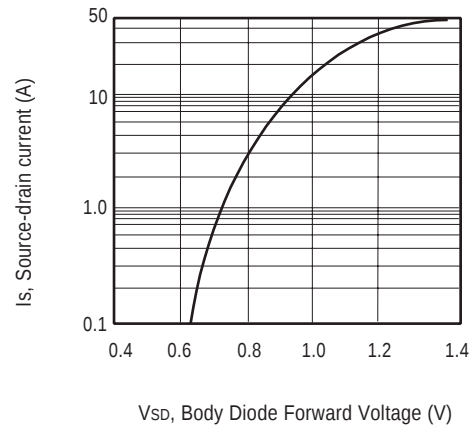


Figure 8. Body Diode Forward Voltage Variation with Source Current

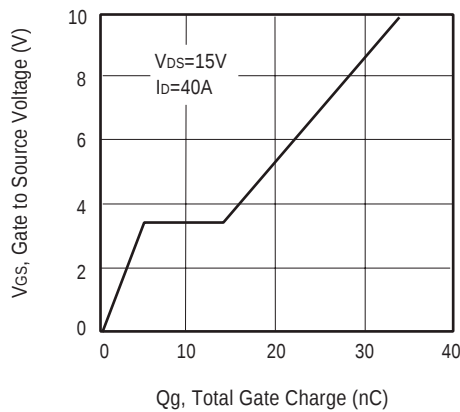


Figure 9. Gate Charge

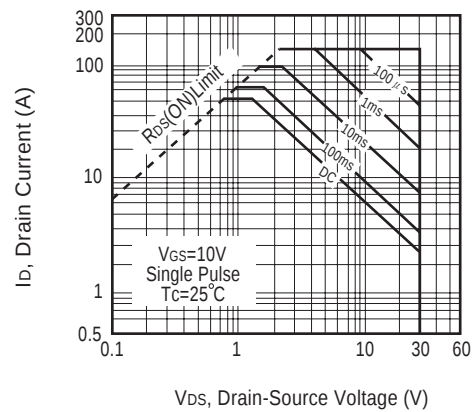


Figure 10. Maximum Safe Operating Area

CED61A3/CEU61A3

6

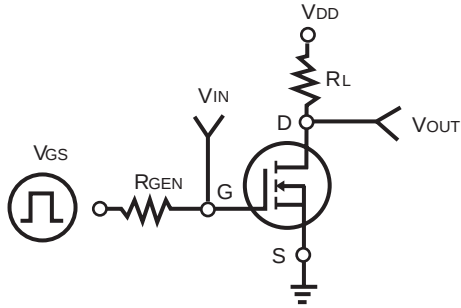


Figure 11. Switching Test Circuit

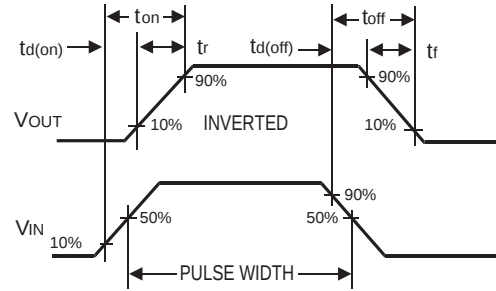


Figure 12. Switching Waveforms

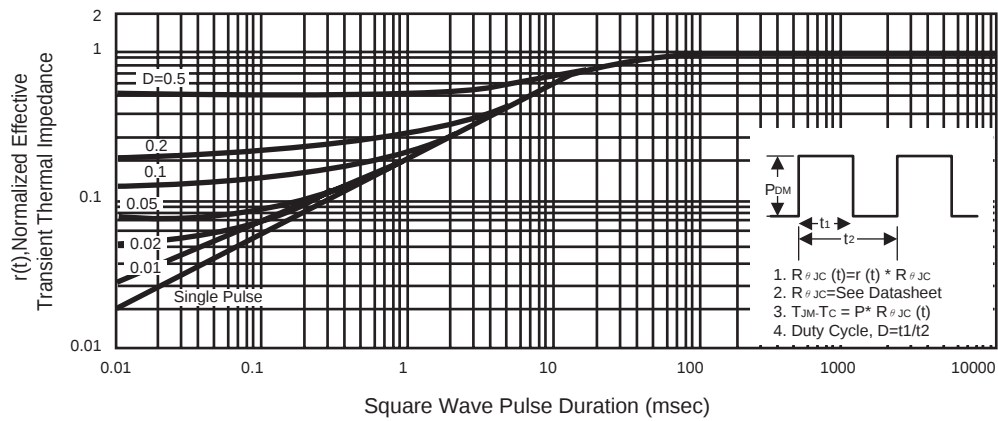


Figure 13. Normalized Thermal Transient Impedance Curve