MOSEL VITELIC *V53C664H*

64K x 16 BIT FAST PAGE MODE BYTE WRITE CMOS DYNAMIC RAM

V53C664H	50	55	60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	50 ns	55 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	26 ns	28 ns	30 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	30 ns	32 ns	34 ns
Min. Read/Write Cycle Time, (t_{RC})	95 ns	100 ns	110 ns

Features

- 64K by 16-bit organization
- $\overline{RAS}$ Access time: 50, 55, 60 ns
- Low power dissipation
- Low CMOS Standby Current
- Fast Page, Byte-Write, Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, and $\overline{RAS}$-only refresh capability
- Refresh Interval 4ms (256 cycles)
- Available in 40 Pin Plastic SOJ package

Description

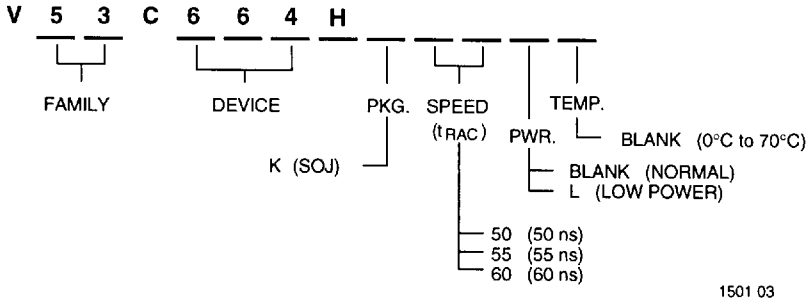
The V53C664H is a new generation, 65,536 word x 16 bit CMOS dynamic RAM fabricated with VICMOS III technology. The 16-bit wide organization makes the V53C664H ideal for high bandwidth applications such as imaging and graphics.

The V53C664H supports Fast Page Mode operation for high data bandwidth. Fast Page Mode allows 256 random accesses within a single row with access cycle times as short as 38ns per 16-bit word. The addition of Byte Write control, of upper and lower byte, makes the V53C664H ideal for use in 16-, 32-bit wide data bus systems.

Mulitplexed address inputs and common input/output permit the V53C664H to be packaged in a standard 40 pin plastic SOJ to provide high system bit densities.

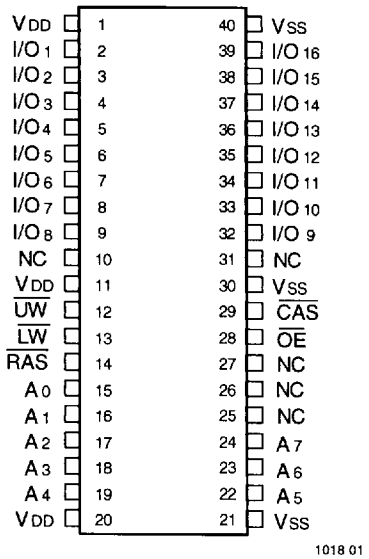
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power		Temperature Mark
	K	50	55	60	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	Blank



Description	*Pkg.*	*Pin Count*
Plastic SOJ	K	40

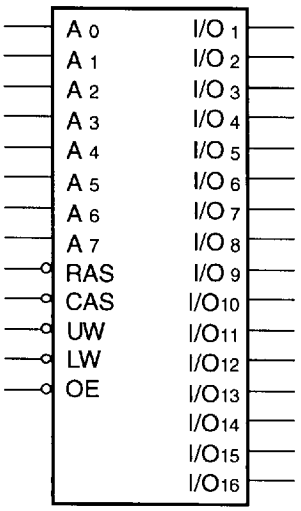
40-Pin Plastic SOJ
PIN CONFIGURATION
Top View



Pin Names

Symbol	Name
A0 – A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Byte Write Input
$\overline{LW}$	Read/Lower Byte Write Input
$\overline{OE}$	Output Enable
I/O1 – I/O16	Data Input/Output
V_{DD}	Power (+ 5V)
V_{SS}	Ground
NC	No Connection

Logic Symbol



*Absolute Maximum Ratings**

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

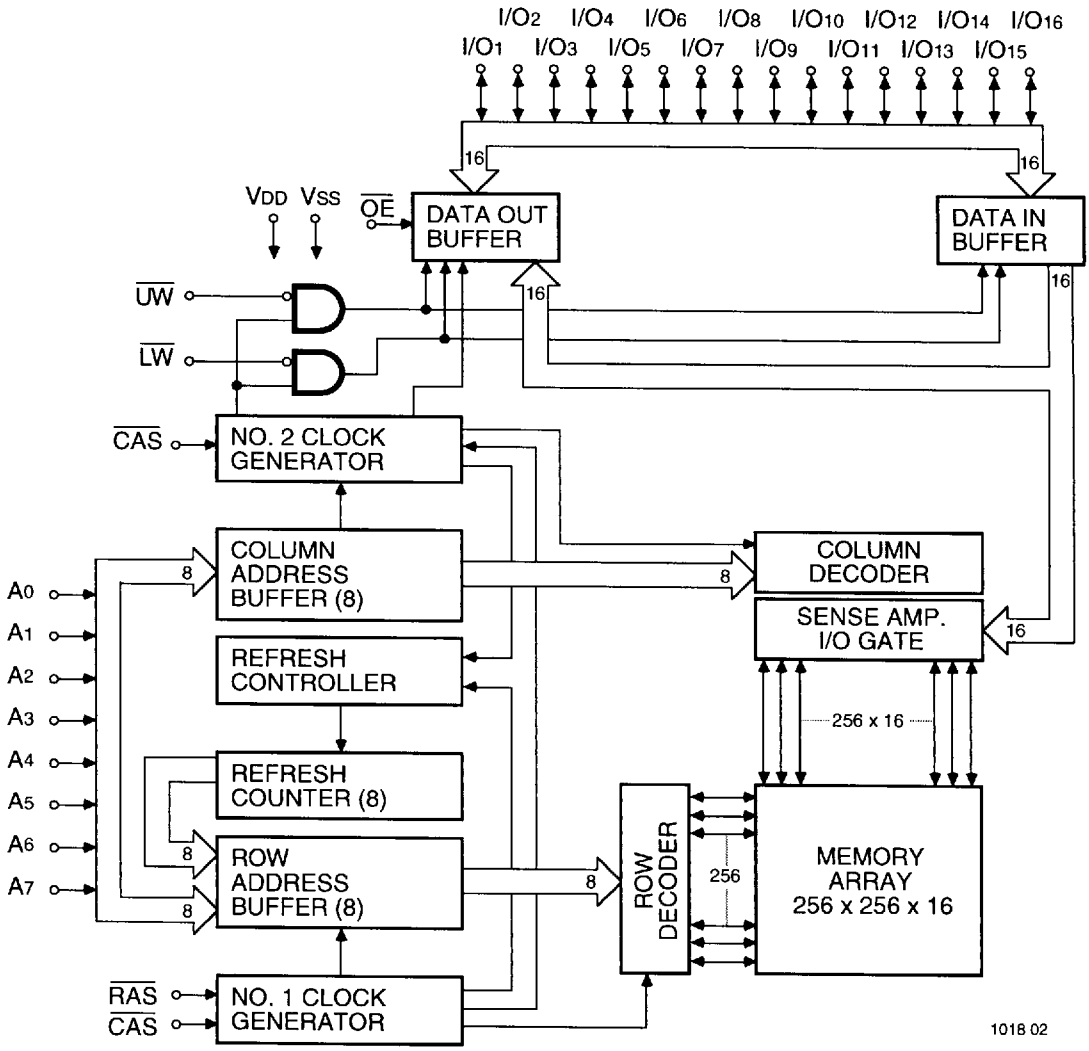
*Capacitance**

V_{DD} = 5V ± 10%, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Input Capacitance (A0 – A7)	3	4	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	4	5	pF
C_{OUT}	Output Capacitance (I/O1 – I/O16)	5	7	pF

*NOTE: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C664H						Unit	Test Conditions	Notes
			Min.	Typ.	Max.	Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10		10				µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10		10				µA	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	50			160				mA	$t_{RC} = t_{RC}$ (min.)	1,2
		55			150						
		60			140						
I_{DD2}	V_{DD} Supply Current, TTL Standby				2.0				mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	50			160				mA	$t_{RC} = t_{RC}$ (min.)	2
		55			150						
		60			140						
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	50			150				mA	Minimum Cycle	1,2
		55			140						
		60			130						
I_{DD6}	V_{DD} Supply Current, CMOS Standby				1.0				mA	$\overline{RAS} \ge V_{DD}$–0.2 V, $\overline{CAS} \ge V_{DD}$ – 0.2V, other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		–1		0.8				V		3
V_{IH}	Input High Voltage		2.4		V_{DD} +1				V		3
V_{OL}	Output Low Voltage				0.4				V	I_{OL} = -2.5 mA	
V_{OH}	Output High Voltage		2.4						V	I_{OH} = 2.1 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3 V

#	JEDEC Symbol	Symbol	Parameter	50		55		60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	55	10K	60	10K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	95	—	100	—	110	—	ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	35	—	35	—	40	—	ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	50	—	55	—	60	—	ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	18	10K	20	10K	ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	35	18	37	20	40	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8	—	8	—	10	—	ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10	—	10	—	10	—	ns	
12	$t_{CL1RH1(R)}$	t_{RSHr}	$\overline{RAS}$ Hold Time (Read Cycle)	15	—	18	—	20	—	ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	—	0	—	0	—	ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15	—	15	—	15	—	ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$	—	15	—	18	—	20	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	18	—	20	ns	6, 7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	55	—	60	ns	6, 8, 9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address	—	26	—	28	—	30	ns	6, 7, 10
21	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	15	0	15	0	15	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	40	—	45	—	50	—	ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	24	15	27	15	30	ns	11
25	$t_{CL1RH1(W)}$	t_{RSHw}	RAS or CAS Hold Time in Write Cycle	15	—	18	—	20	—	ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	18	—	20	—	22	—	ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Set-Up Time	0	—	0	—	0	—	ns	12, 13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	10	—	10	—	ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	10	—	10	—	10	—	ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	40	—	45	—	50	—	ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	18	—	20	—	22	—	ns	

AC Characteristics (continued)

#	JEDEC Symbol	Symbol	Parameter	50		55		60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
32	t_{DVWL2}	t_{DS}	Data-In Set-Up Time	0	—	0	—	0	—	ns	14
33	t_{WL1DX}	t_{DH}	Data-In Hold Time	10	—	10	—	10	—	ns	14
34	t_{WL1GL2}	t_{WOH}	$\overline{OE}$ Hold Time	10	—	10	—	10	—	ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	15	—	15	—	15	—	ns	
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	150	—	160	—	170	—	ns	
37		t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Cycle Only	50	100K	55	100K	60	100K	ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	40	—	43	—	45	—	ns	12
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time in Read-Modify-Write Cycle	75	—	80	—	85	—	ns	12
41	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	51	—	53	—	55	—	ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	30	—	32	—	34	—	ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	26	—	28	—	30	—	ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge	—	28	—	30	—	32	ns	7
46	t_{RL1DX}	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	40	—	45	—	50	—	ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	5	—	ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	85	—	90	—	95	—	ns	
51	t_{WH2CL2}	t_{MCS}	Byte-Masked Write Setup Time	0	—	0		0		ns	
52	t_{RH2WL2}	t_{MRH}	Byte-Masked Write Hold Time Referenced to $\overline{RAS}$	0	—	0		0		ns	
53	t_{CH2WL2}	t_{MCH}	Byte-Masked Write Hold Time Referenced to $\overline{RAS}$	0	—	0		0		ns	
		t_T	Transition Time (Rise and Fall)	5	50	5	50	5	50	ns	15
		t_{REF}	Refresh Interval (256 Cycles)	4	—	—	4	—	4	ms	17

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in First Page Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to –1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL loads and 50 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{WHC}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the later occurance of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

    t_{RC} = 125 µs (125 µs x 256 = 32ms)

    $t_{RAS} = t_{RAS}$ (min) to 1µs

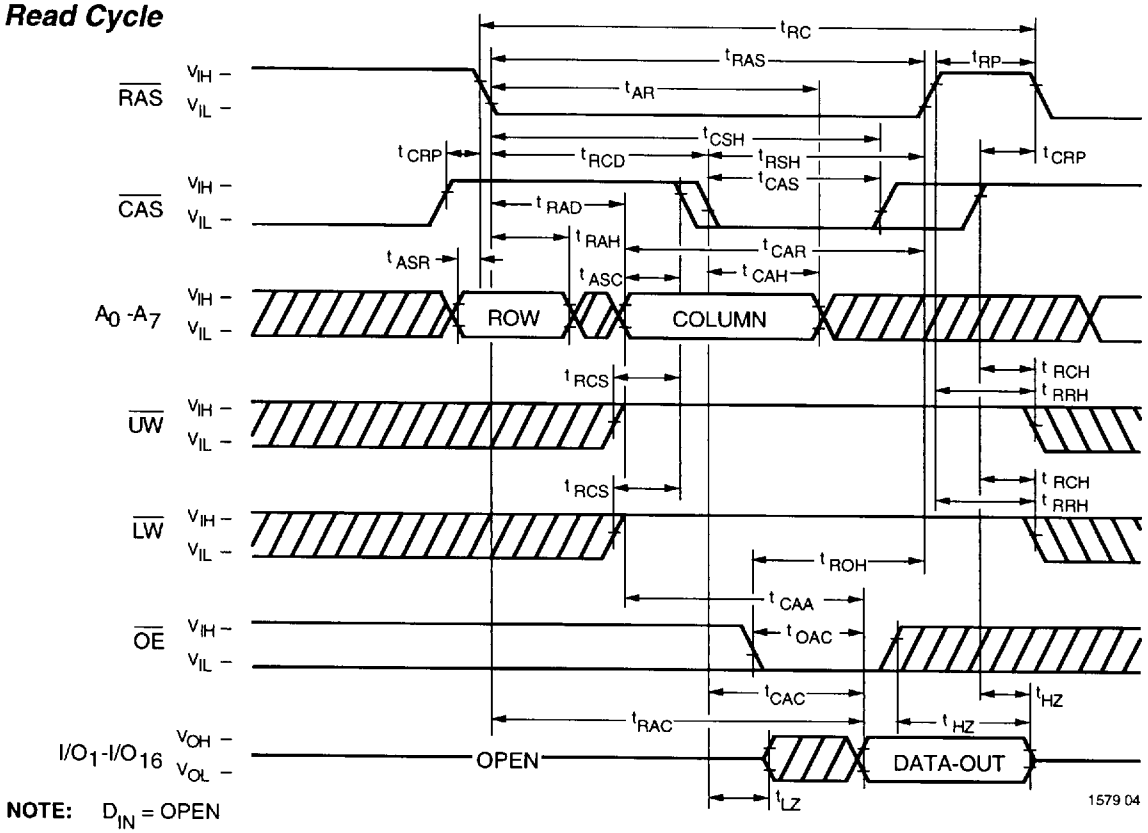
    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V

    $V_{IL} < 0.2$ V

    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V

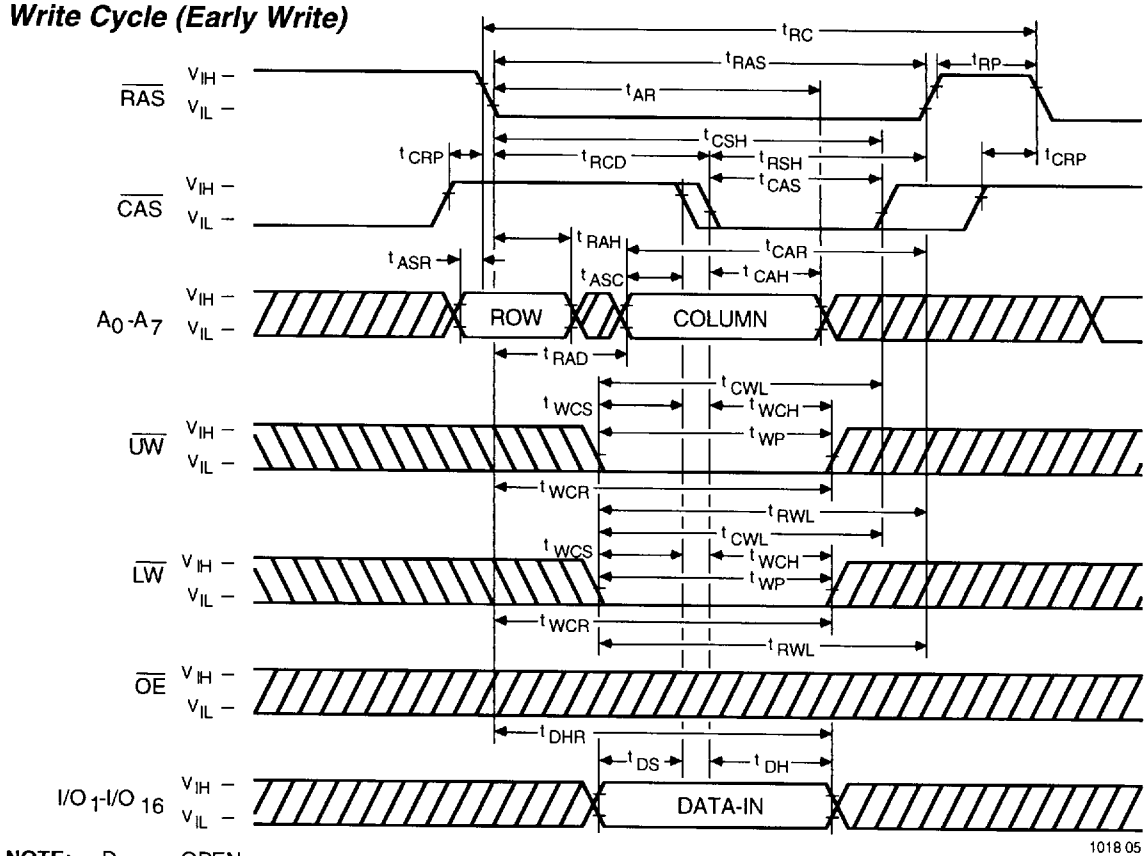
    All other inputs at stable V_{IH} or V_{IL}

Read Cycle



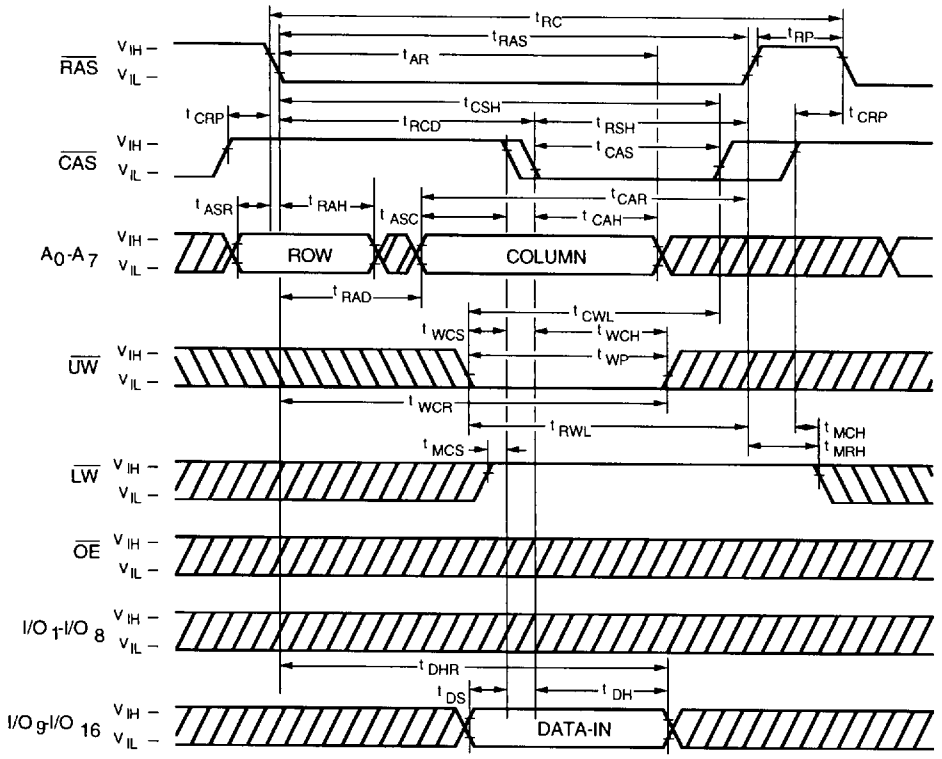
NOTE: D_{IN} = OPEN

Write Cycle (Early Write)



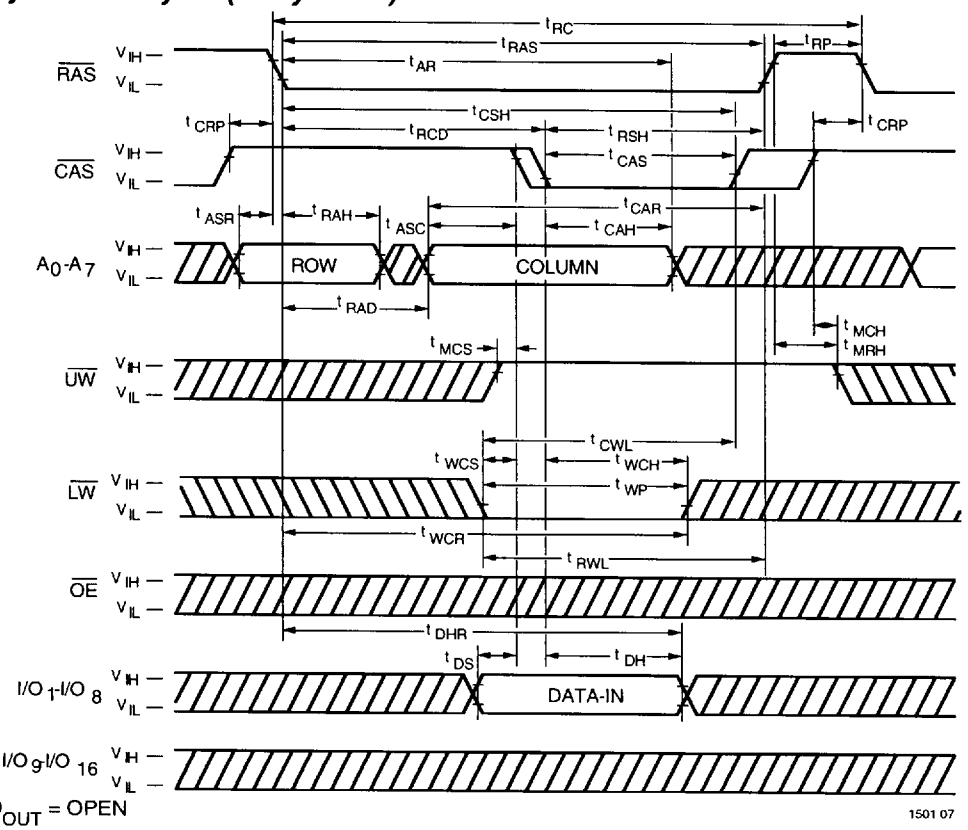
NOTE: D_{OUT} = OPEN

Upper Byte Write Cycle (Early Write)



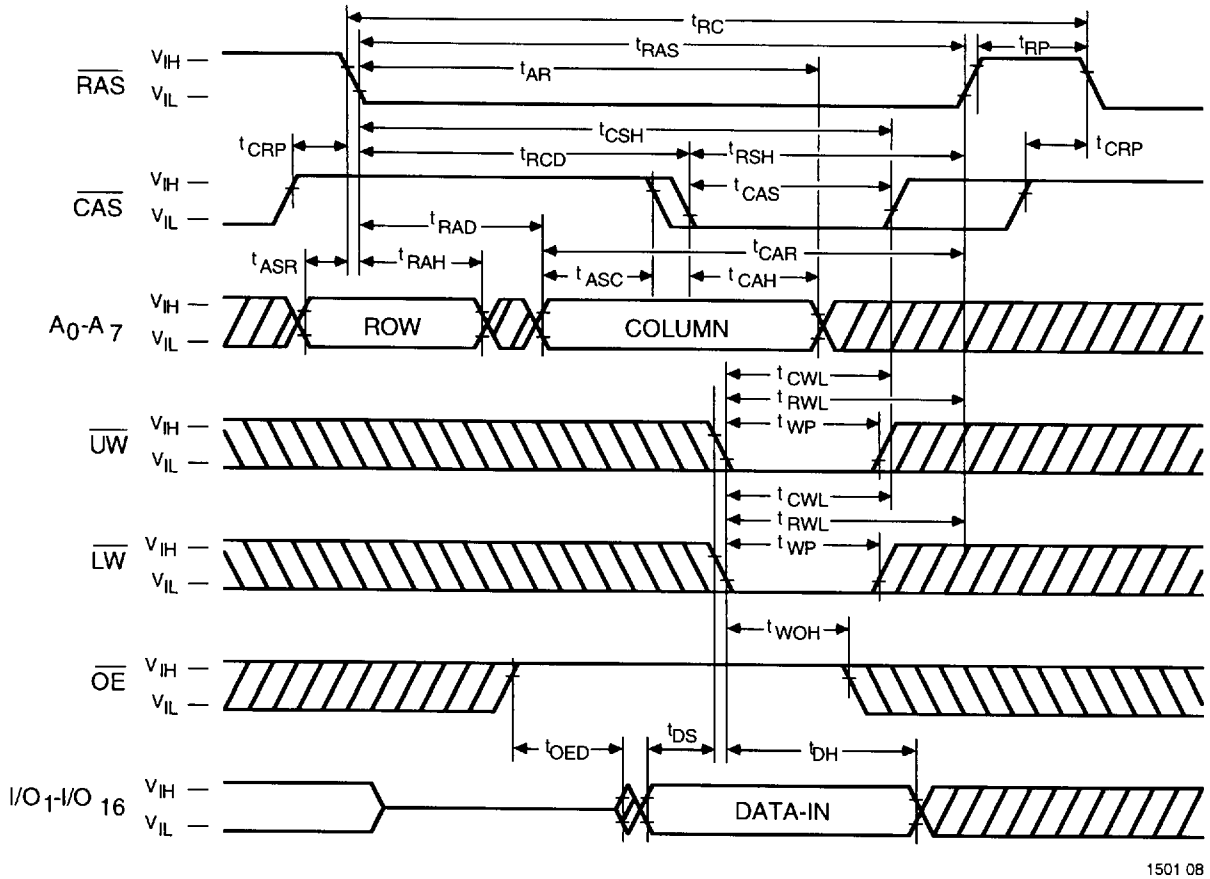
NOTE: D_{OUT} = OPEN

Lower Byte Write Cycle (Early Write)



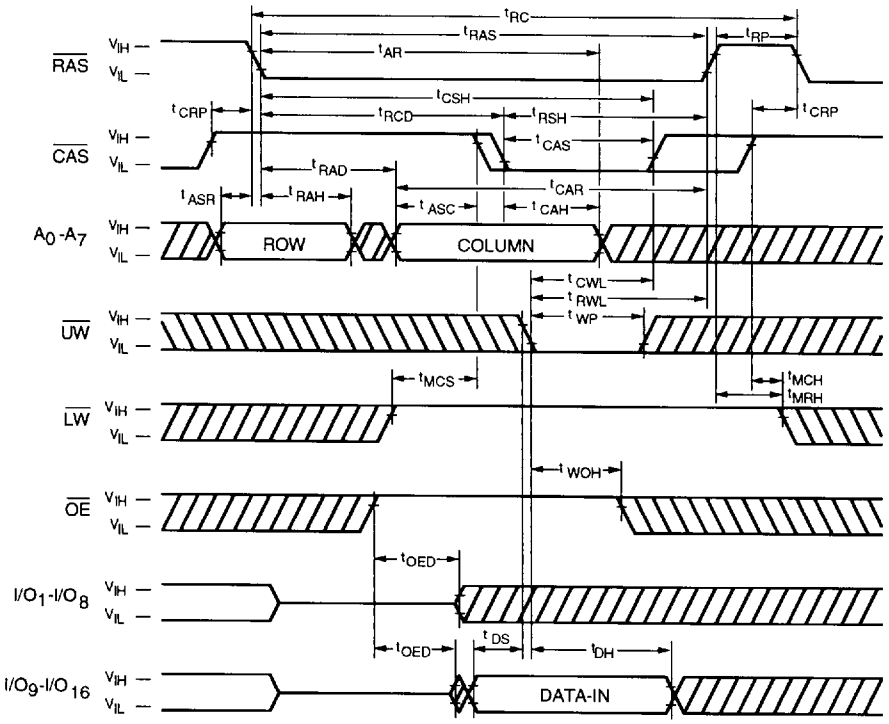
NOTE: D_{OUT} = OPEN

Write Cycle ($\overline{OE}$-Controlled Write)



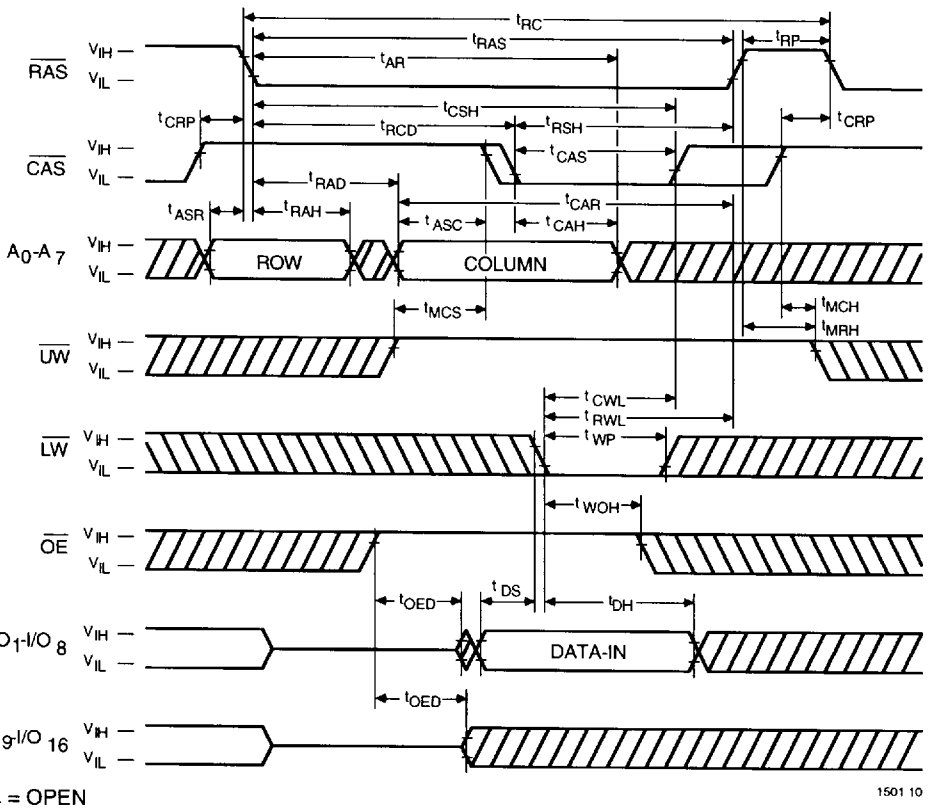
NOTE: D_{OUT} = OPEN

Upper Byte Write Cycle ($\overline{OE}$-Controlled Write)



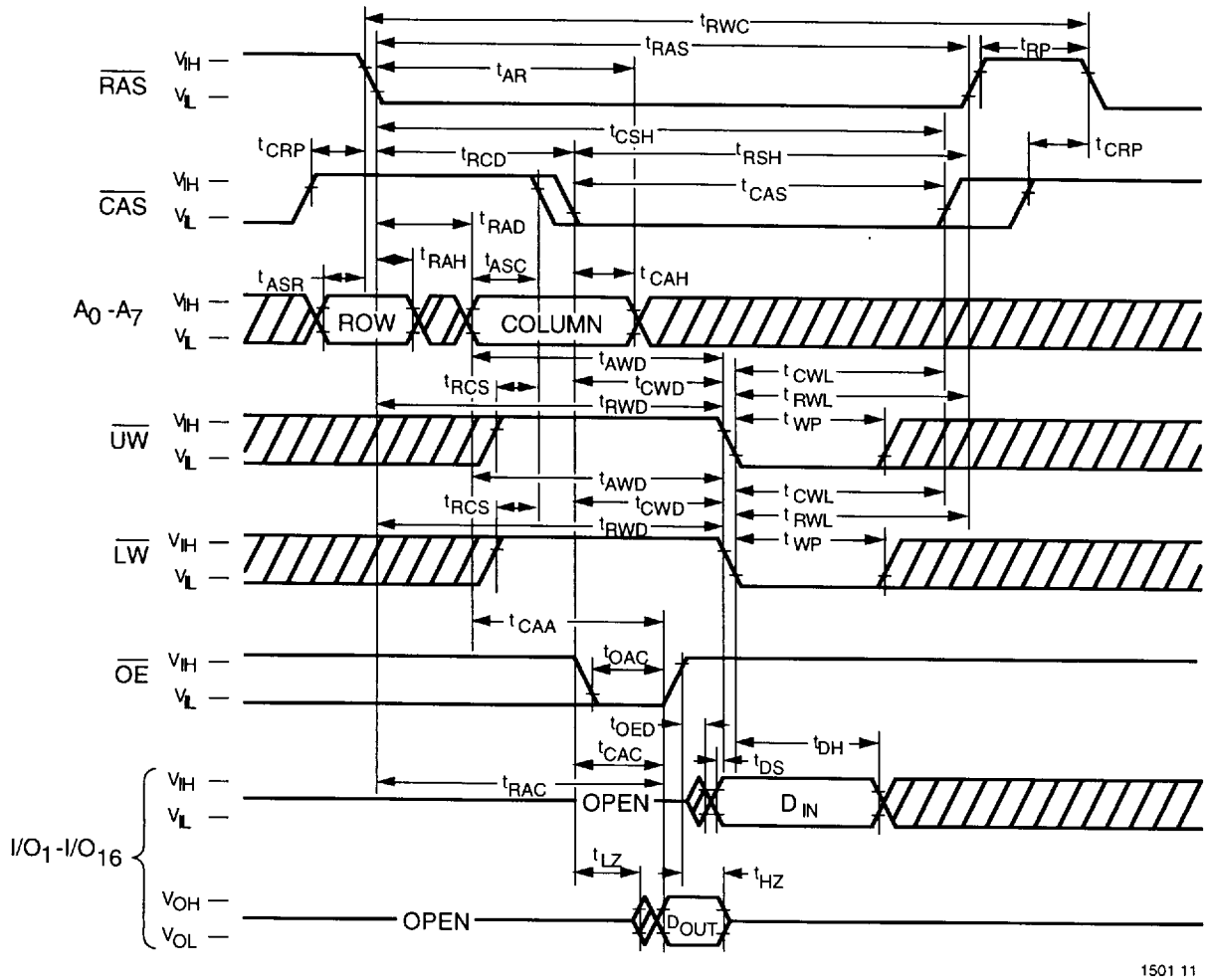
NOTE: D_{OUT} = OPEN

Lower Byte Write Cycle ($\overline{OE}$-Controlled Write)

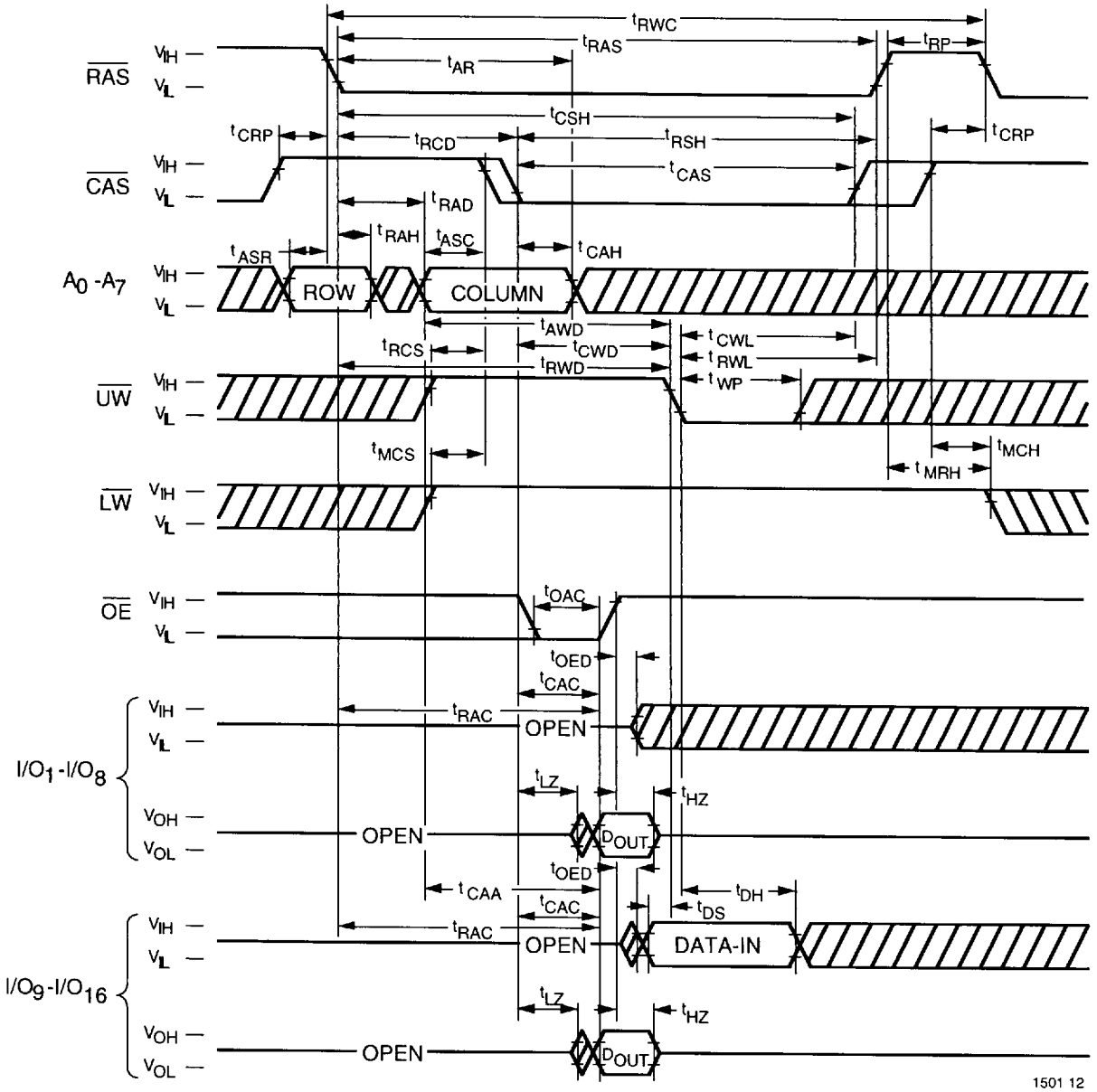


NOTE: D_{OUT} = OPEN

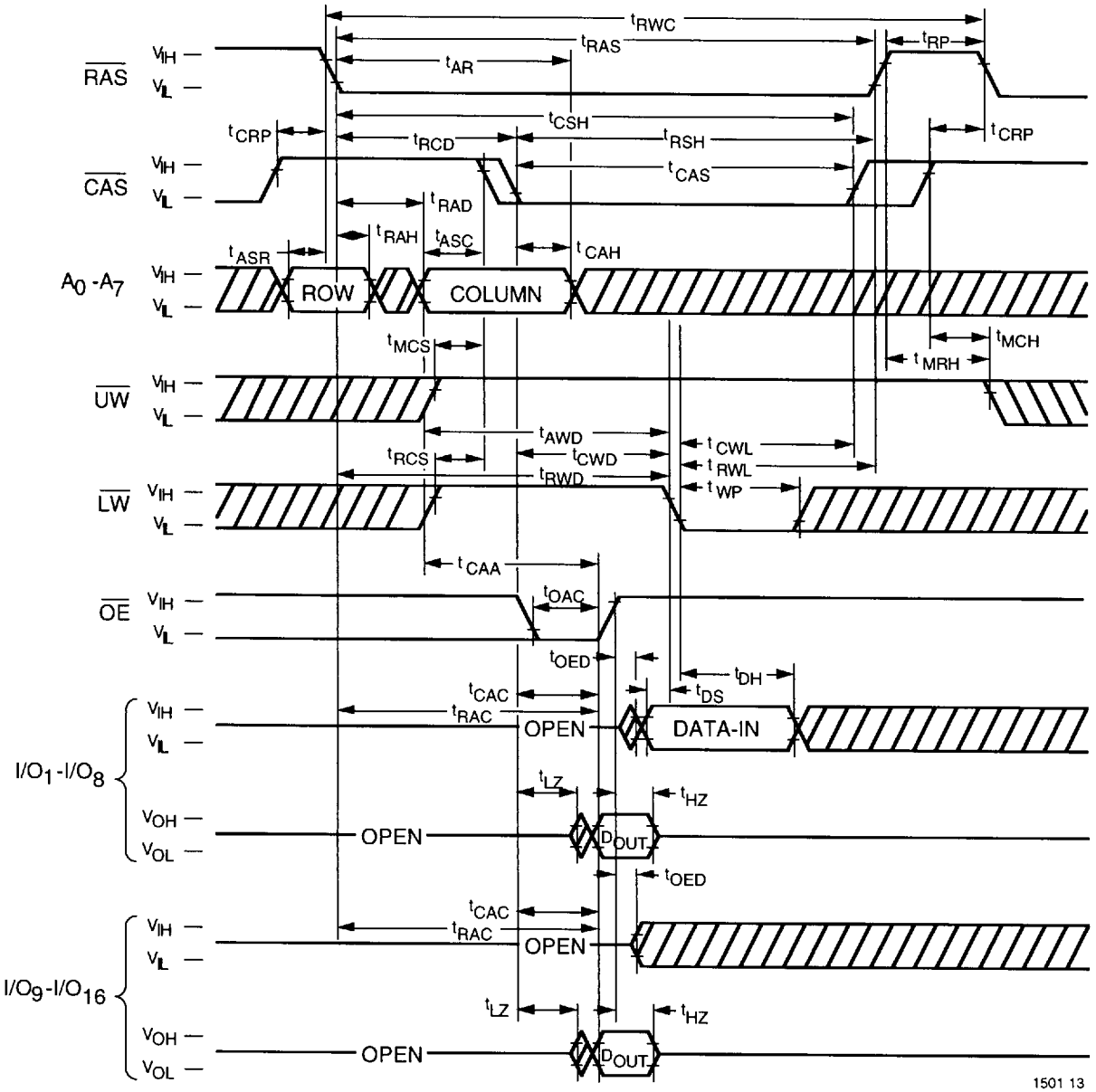
Read-Modify-Write Cycle



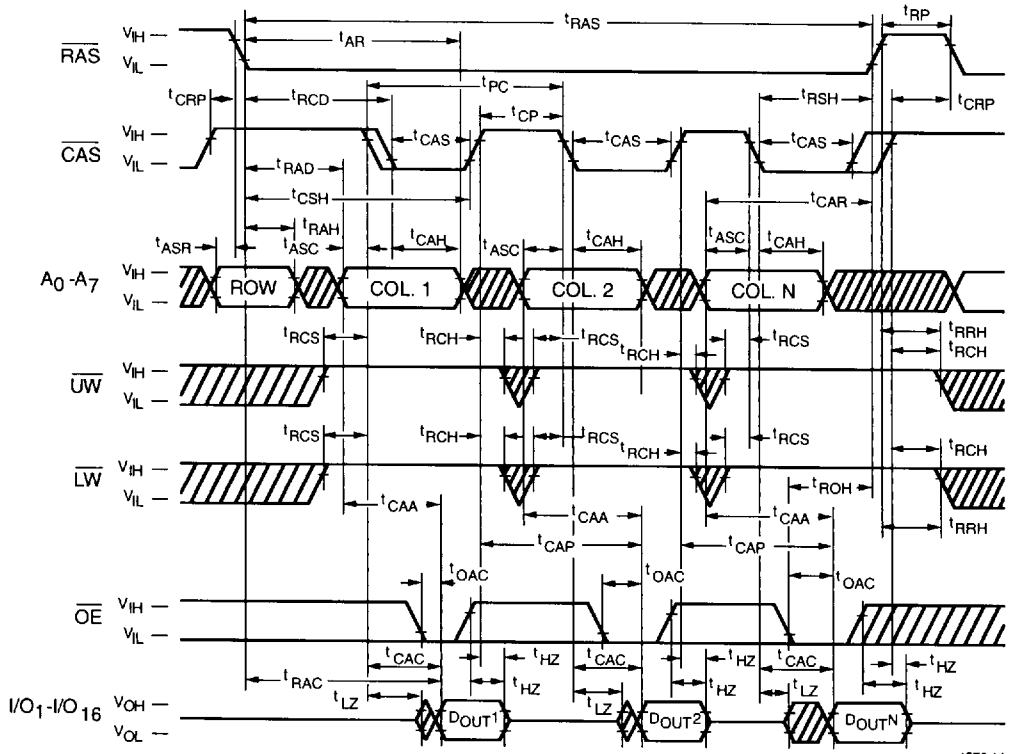
Read-Modify-Upper-Byte-Write Cycle



Read-Modify-Lower-Byte-Write Cycle



Fast Page Mode Read Cycle



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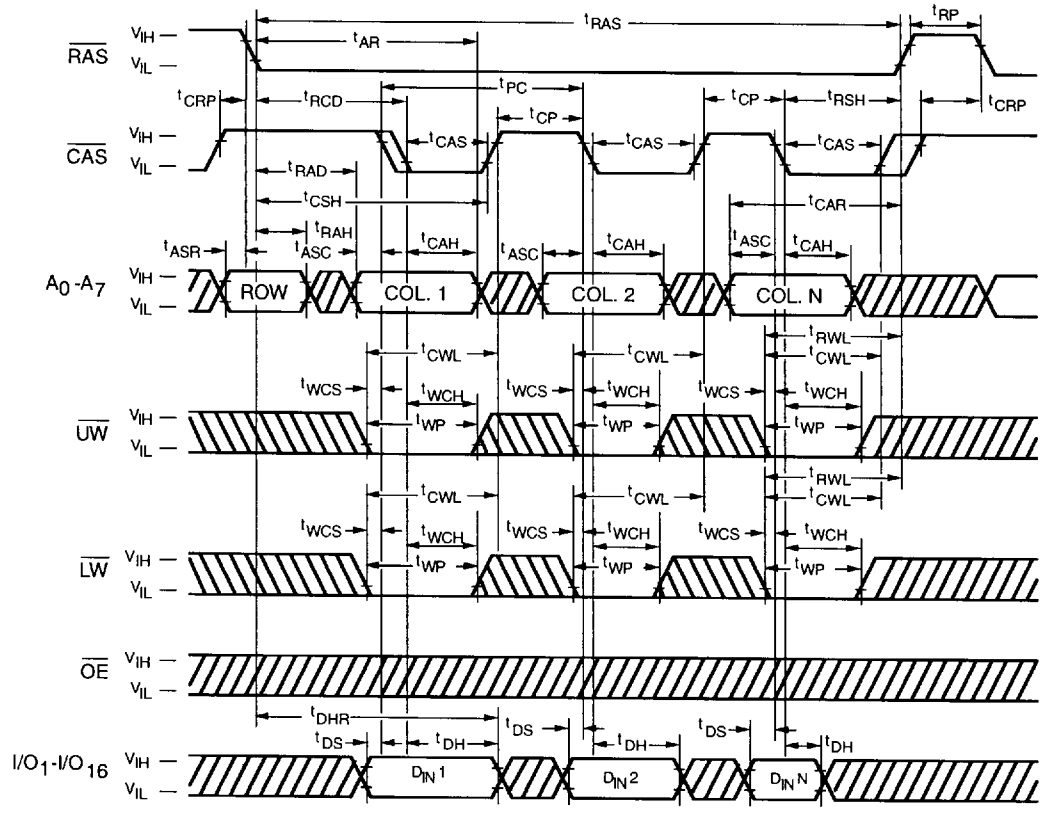
NOTE: D_{IN} = OPEN

Fast Page Mode Write Cycle



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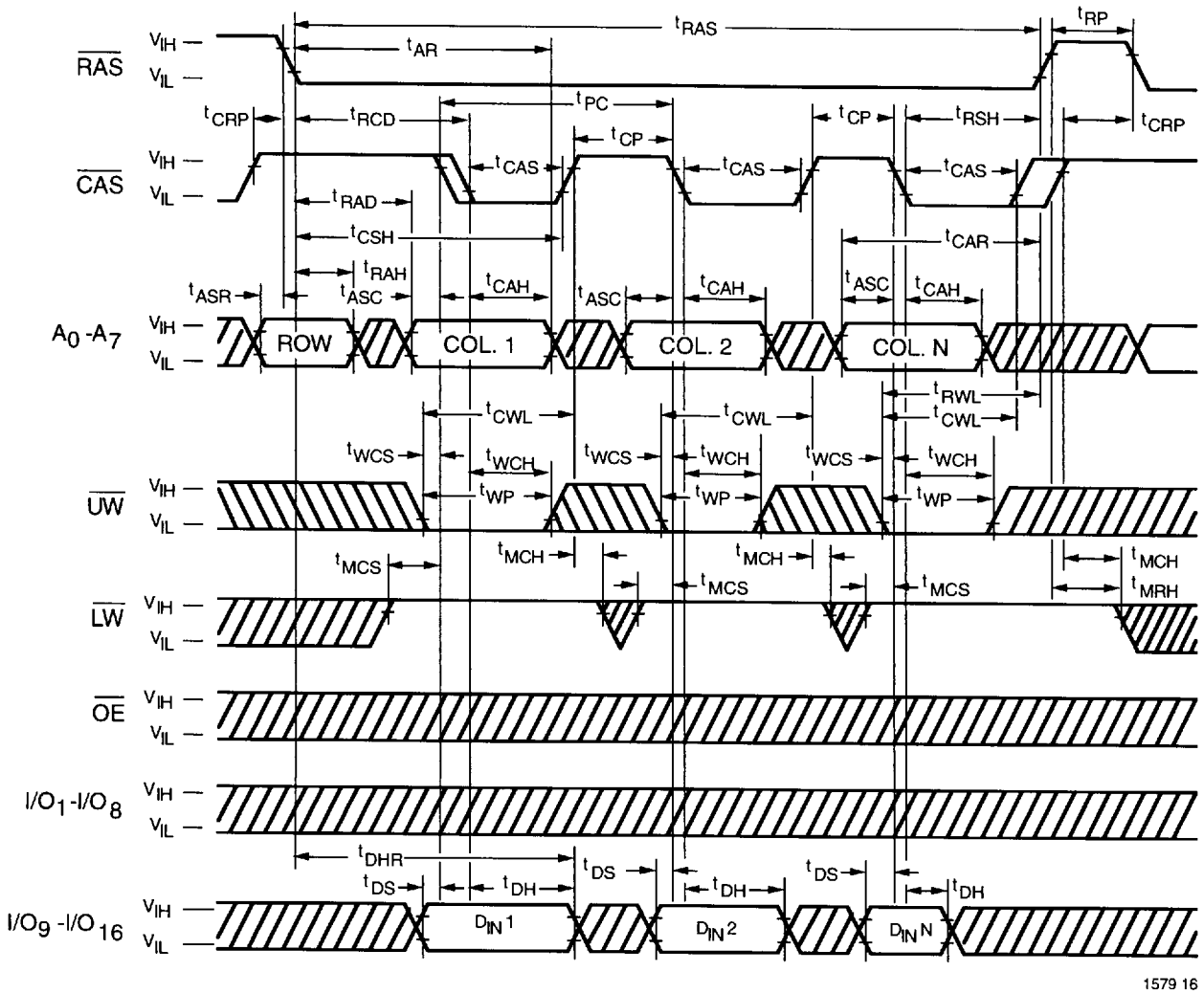
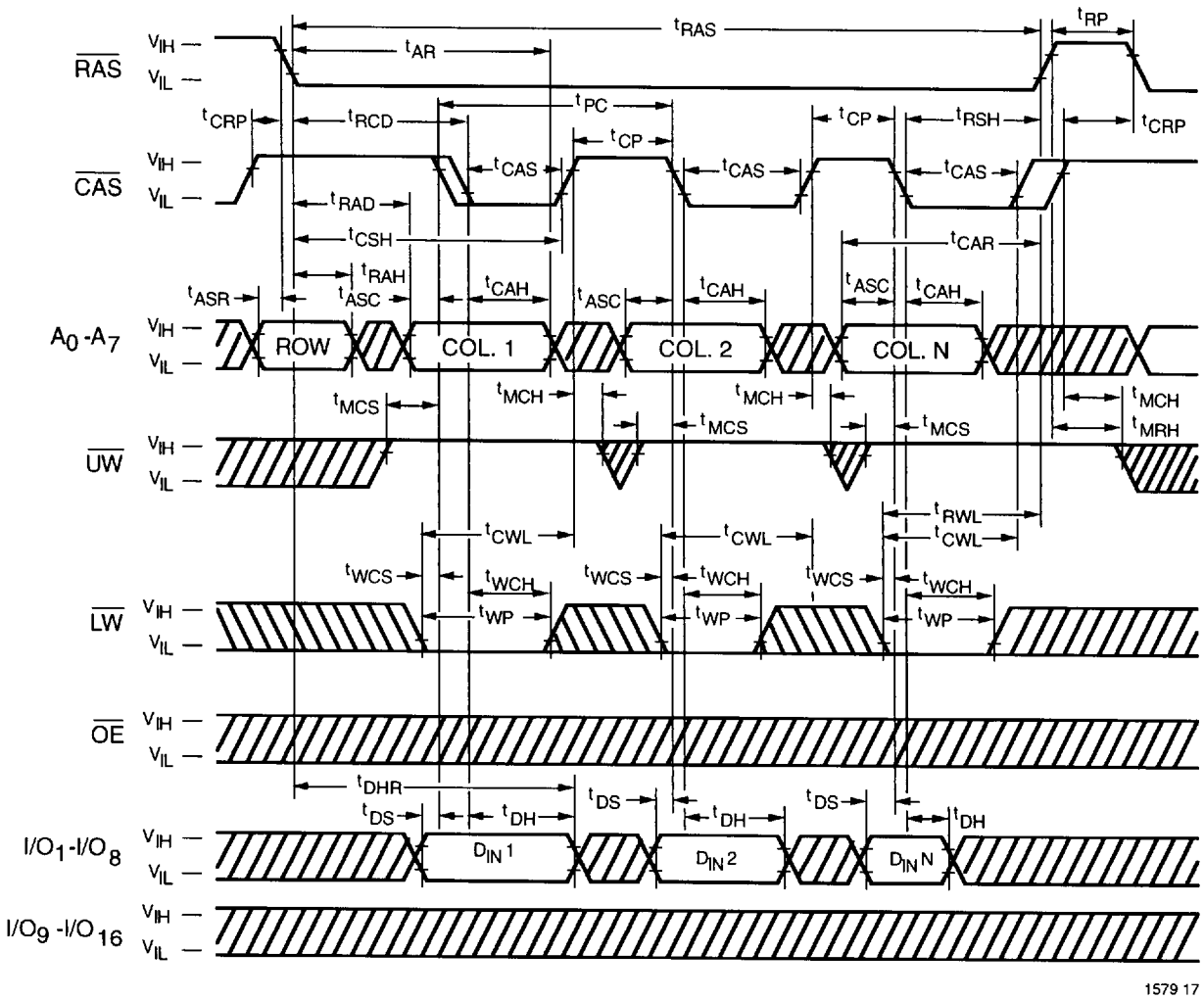
NOTE: D_{OUT} = OPEN

Fast Page Mode Upper Byte Write Cycle



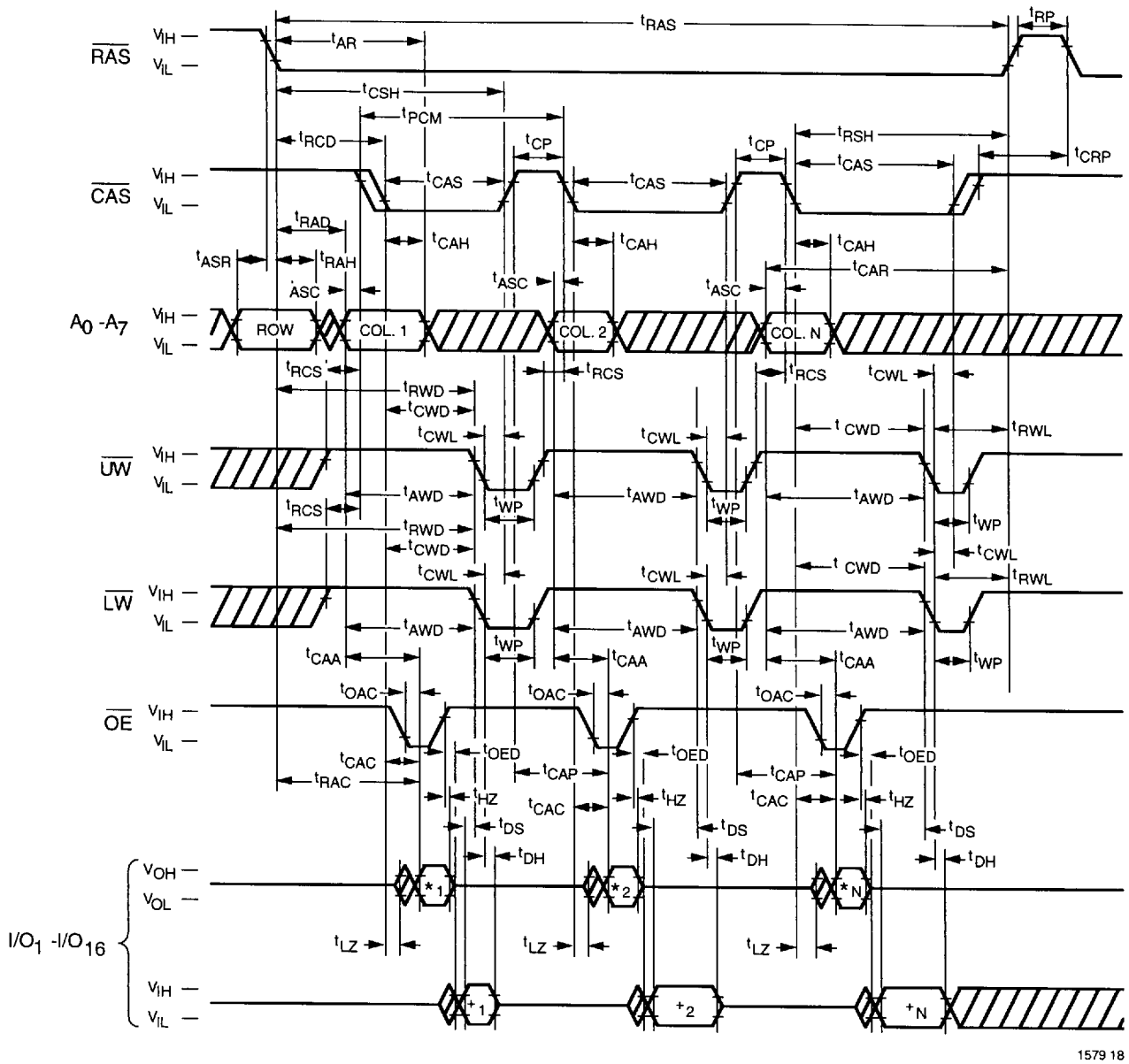
NOTE: D_{OUT} = OPEN

Fast Page Mode Lower Byte Write Cycle



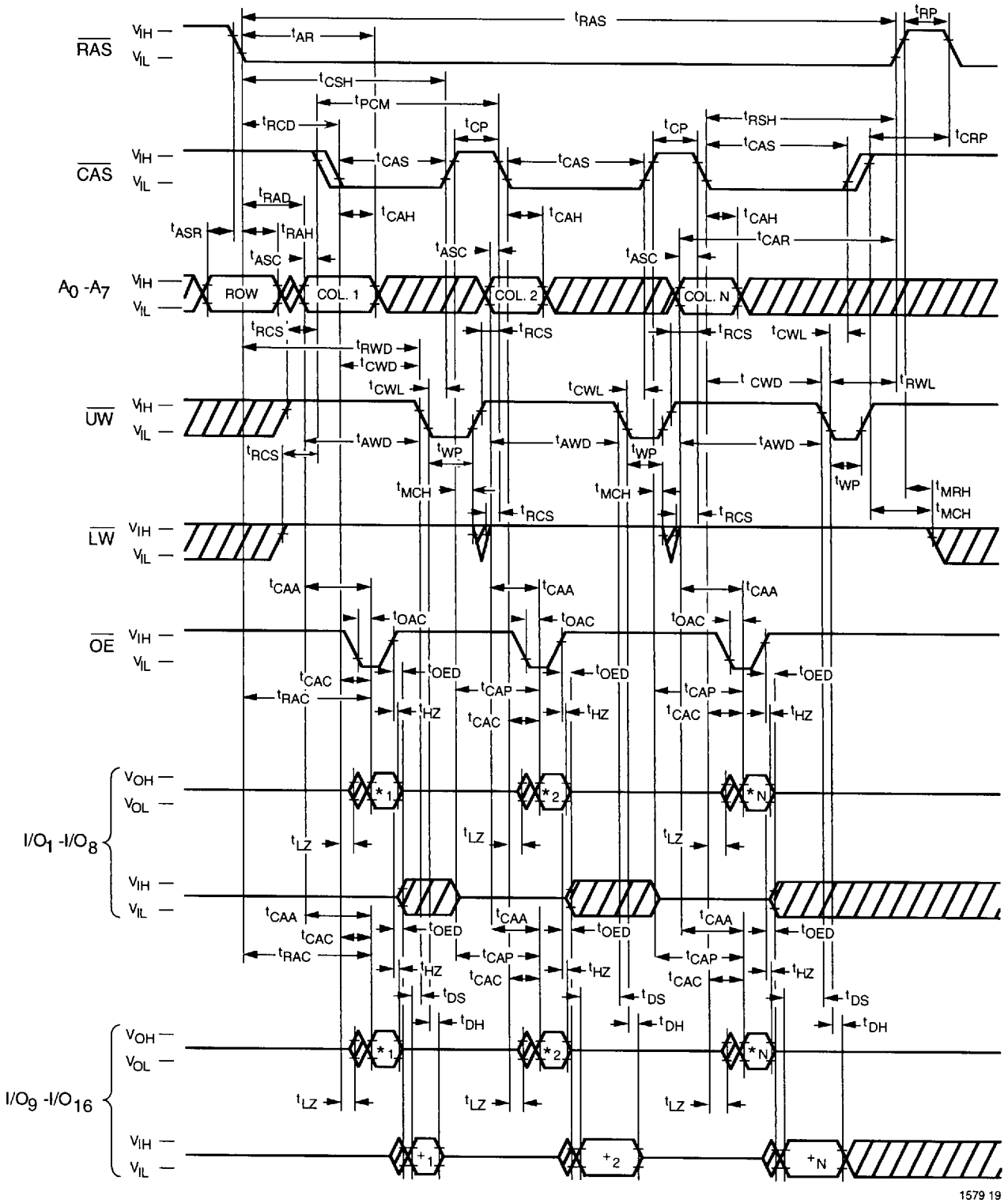
NOTE: D_{OUT} = OPEN

Fast Page Read-Modify-Write Cycle



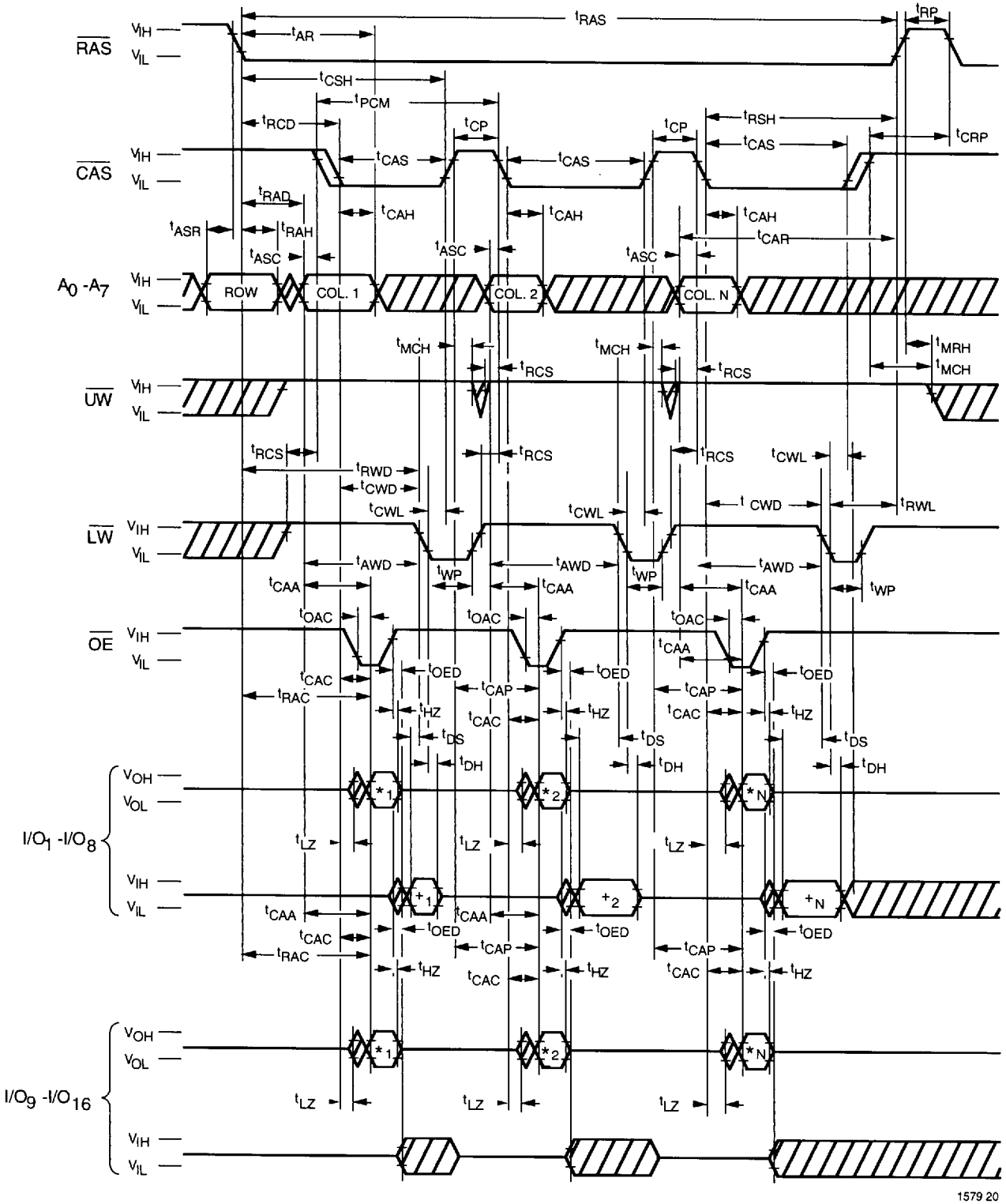
NOTE: * = D_{OUT}, + = D_{IN}

Fast Page Mode Read-Modify-Upper-Byte-Write Cycle



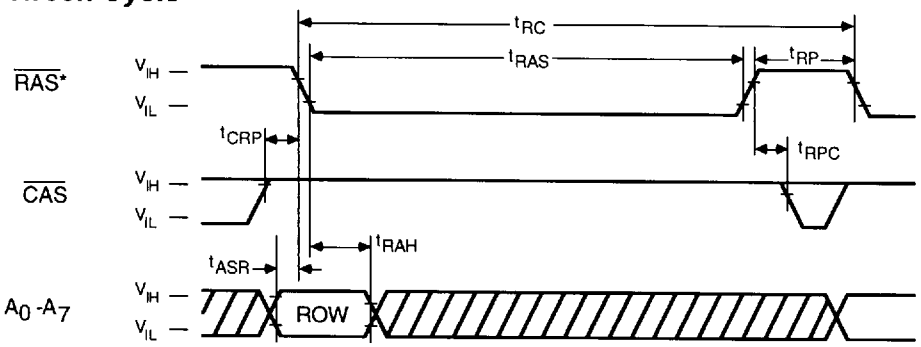
NOTE: $^{*} = D_{OUT}$, $^{+} = D_{IN}$

Fast Page Mode Read-Modify-Lower-Byte-Write Cycle



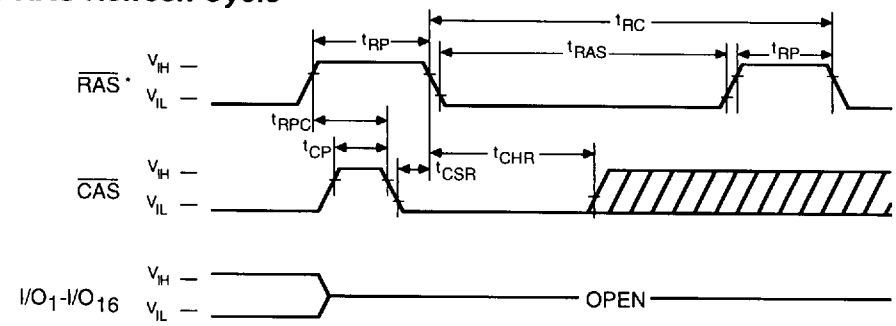
NOTE: * = D_{OUT}, + = D_{IN}

RAS-Only Refresh Cycle



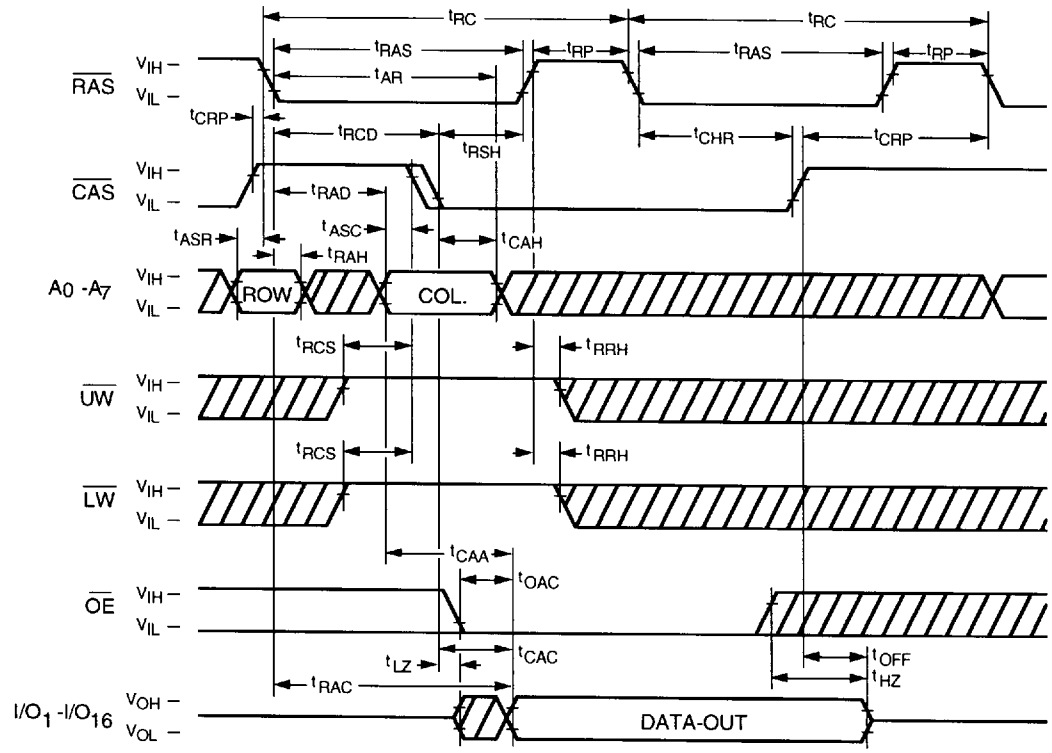
NOTE: $\overline{UW}$, $\overline{LW}$, $\overline{OE}$ = "H" or "L"

CAS-Before-RAS Refresh Cycle



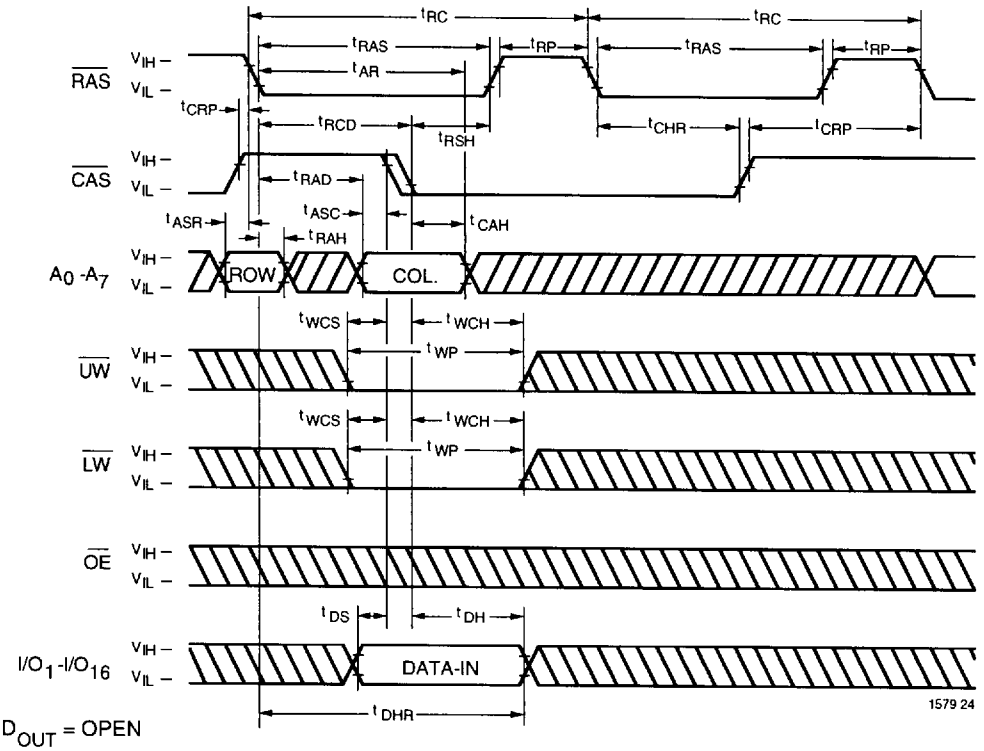
NOTE: D_{IN}, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A0 – A7 = "H" or "L"

Hidden Refresh Cycle (Read)



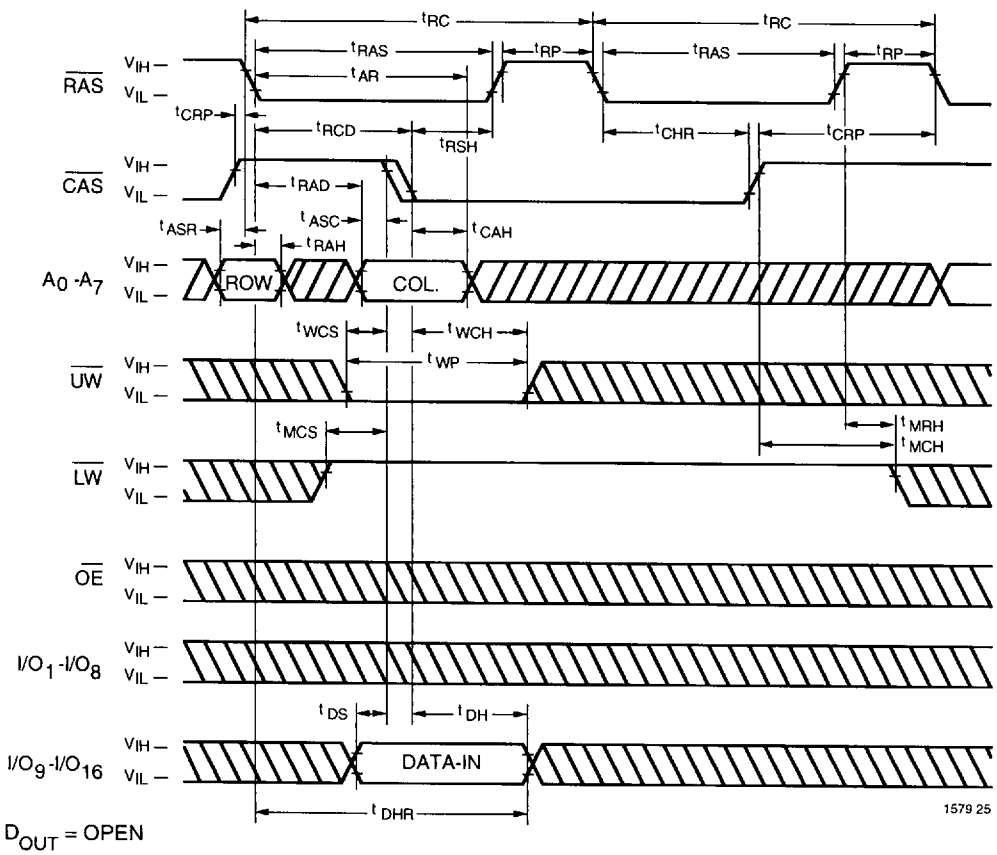
NOTE: D_{IN} = OPEN

Hidden Refresh Cycle (Write)



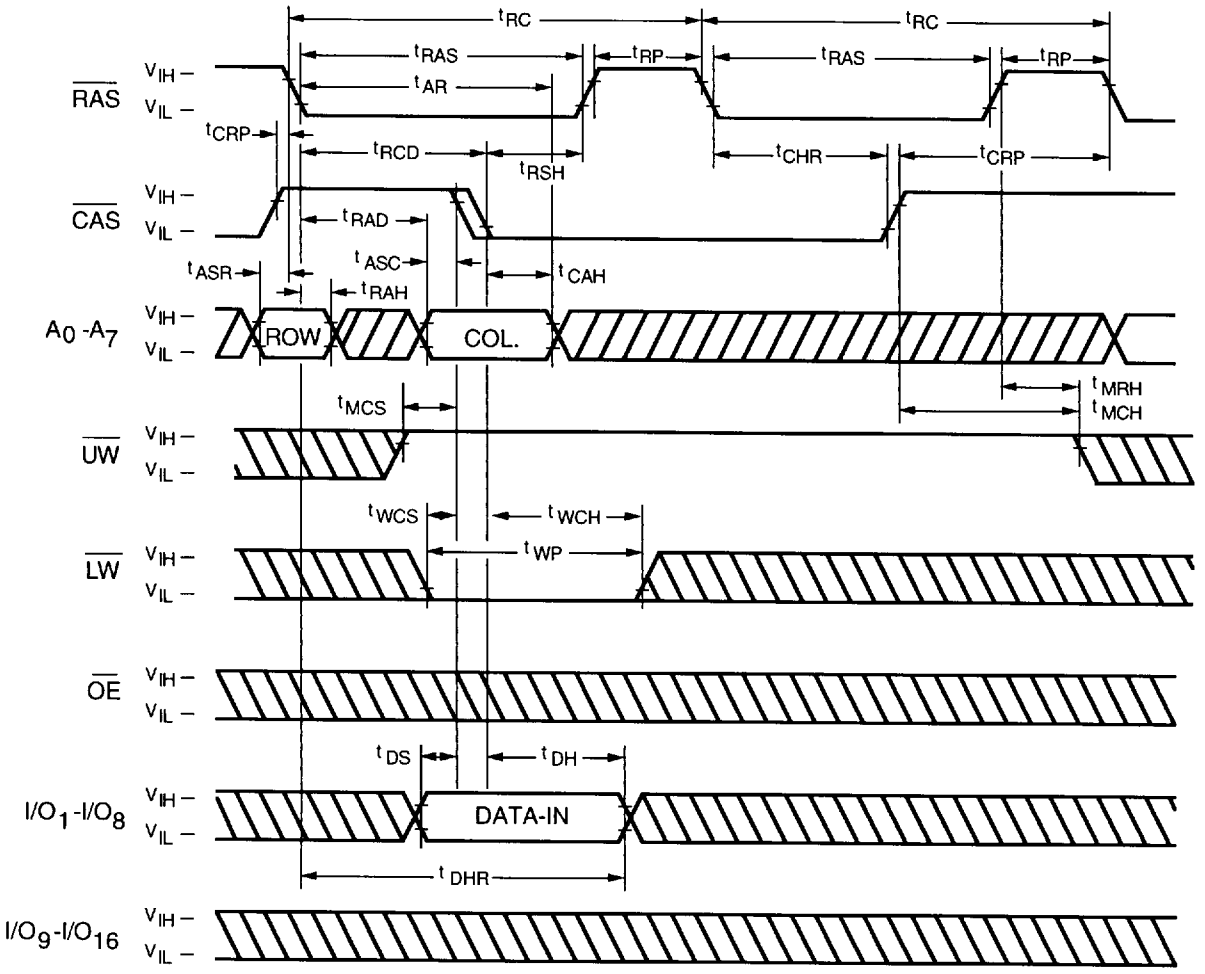
NOTE: D_{OUT} = OPEN

Hidden Refresh Cycle (Upper Byte Write)



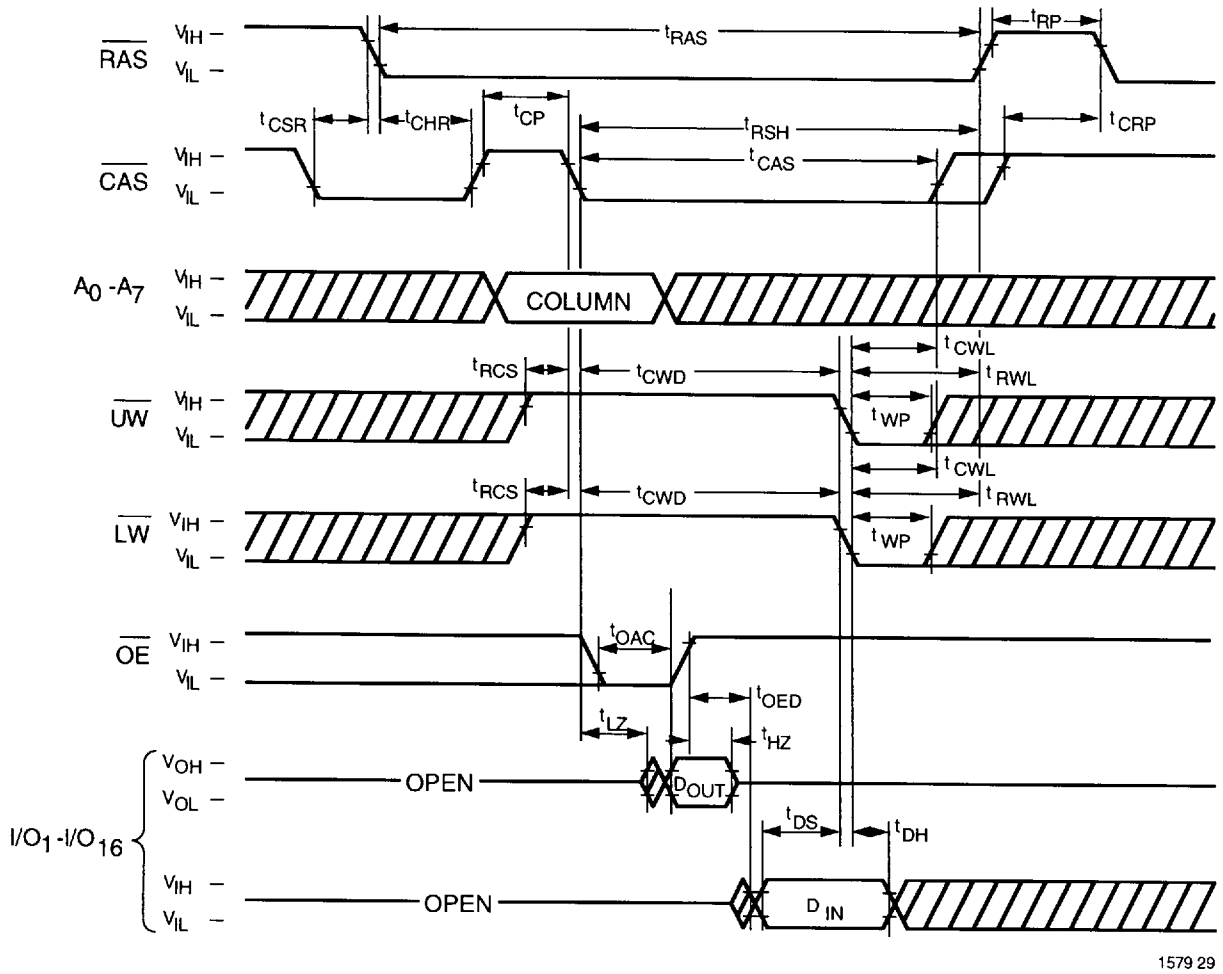
NOTE: D_{OUT} = OPEN

Hidden Refresh Cycle (Lower Byte Write)



NOTE: D_{OUT} = OPEN

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



40-Pin Plastic SOJ