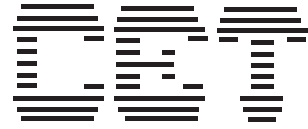


CEP09N6/CEB09N6



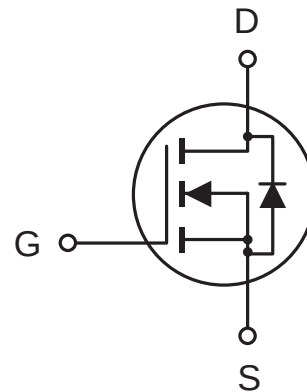
Jul. 2002

4

N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

- 600V , 9A , $R_{DS(ON)} = 1.2\Omega$ @ $V_{GS}=10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current-Continuous -Pulsed	I_D	9	A
	I_{DM}	35	A
Drain-Source Diode Forward Current	I_S	9	A
Maximum Power Dissipation @ $T_c=25^\circ\text{C}$ Derate above 25°C	P_D	156	W
		1.25	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.8	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$

CEP09N6/CEB09N6

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

4

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATING^a						
Single Pulse Drain-Source Avalanche Energy	E _{AS}	V _{DD} = 50V, L = 23.4mH R _G = 25Ω		500		mJ
Maximum Drain-Source Avalanche Current	I _{AS}			9		A
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	600			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600V, V _{GS} = 0V			50	μA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±30V, V _{DS} = 0V			±100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2		4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 6A		1.0	1.2	Ω
On-State Drain Current	I _{D(ON)}	V _{GS} = 10V, V _{DS} = 10V	9			A
Forward Transconductance	g _{FS}	V _{DS} = 50V, I _D = 6A	3	5		S
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 200V, I _D = 9A, V _{GS} = 10V R _{GEN} = 9.1Ω		23	45	ns
Rise Time	t _r			26	50	ns
Turn-Off Delay Time	t _{D(OFF)}			105	165	ns
Fall Time	t _f			22	45	ns
Total Gate Charge	Q _g	V _{DS} = 480V, I _D = 9A, V _{GS} = 10V		73	85	nC
Gate-Source Charge	Q _{gs}			6.0		nC
Gate-Drain Charge	Q _{gd}			45		nC

CEP09N6/CEB09N6

4

ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS ^b						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} = 0V f =1.0MHz		950		pF
Output Capacitance	C _{OSS}			135		pF
Reverse Transfer Capacitance	C _{RSS}			90		pF
DRAIN-SOURCE DIODE CHARACTERISTICS ^a						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V, I _S =9A			1.5	V

Notes

a. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

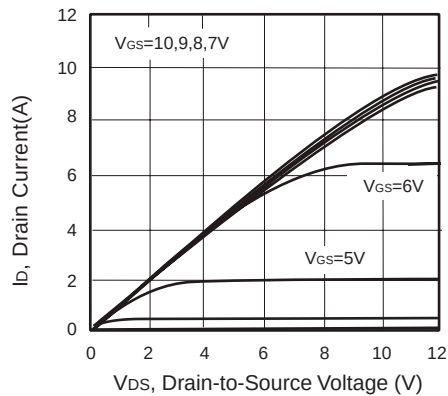


Figure 1. Output Characteristics

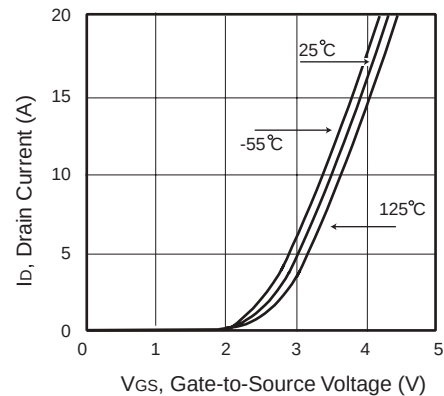


Figure 2. Transfer Characteristics

CEP09N6/CEB09N6

4

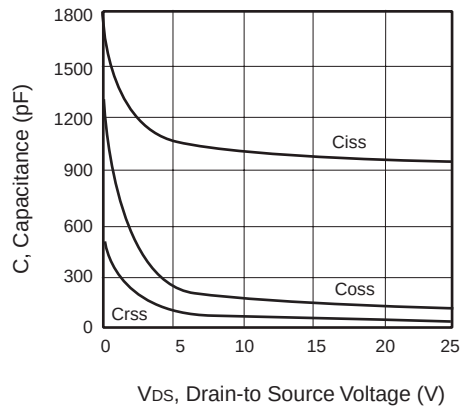


Figure 3. Capacitance

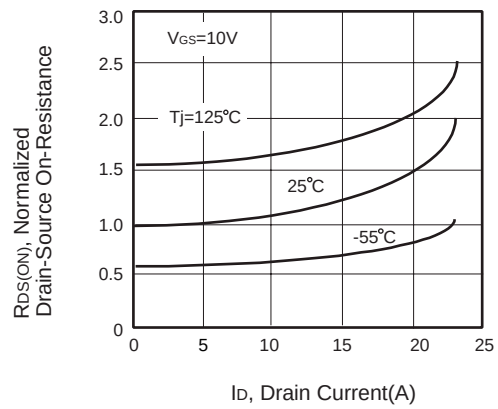


Figure 4. On-Resistance Variation with Drain Current and Temperature

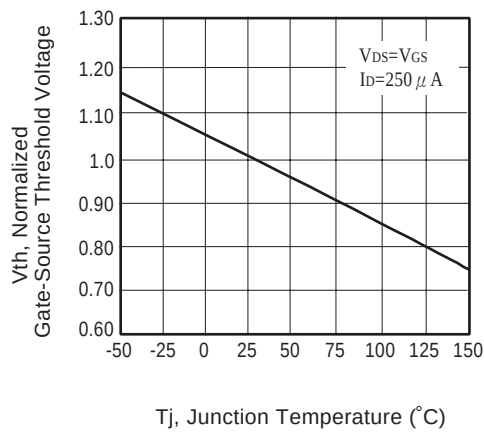


Figure 5. Gate Threshold Variation with Temperature

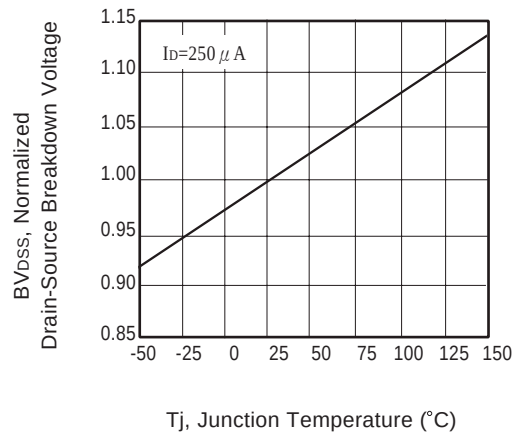


Figure 6. Breakdown Voltage Variation with Temperature

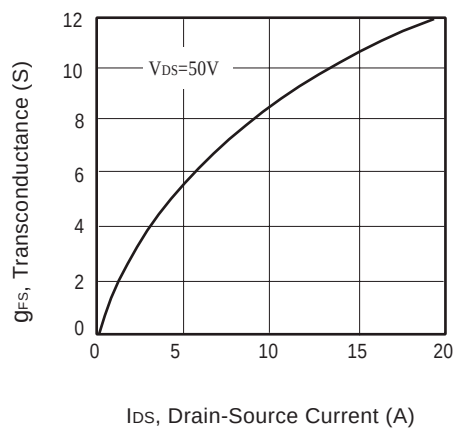


Figure 7. Transconductance Variation with Drain Current

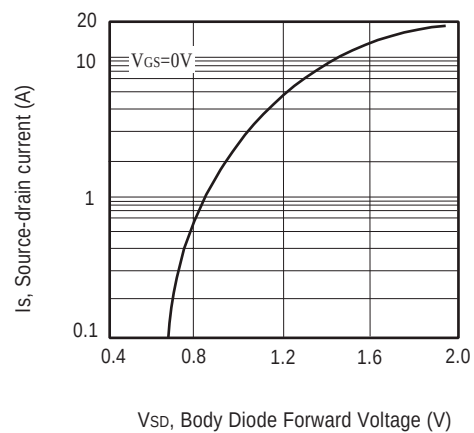


Figure 8. Body Diode Forward Voltage Variation with Source Current

CEP09N6/CEB09N6

4

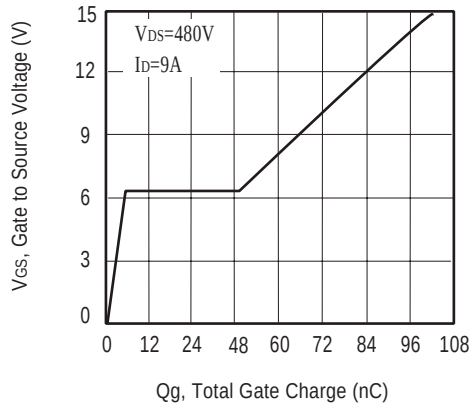


Figure 9. Gate Charge

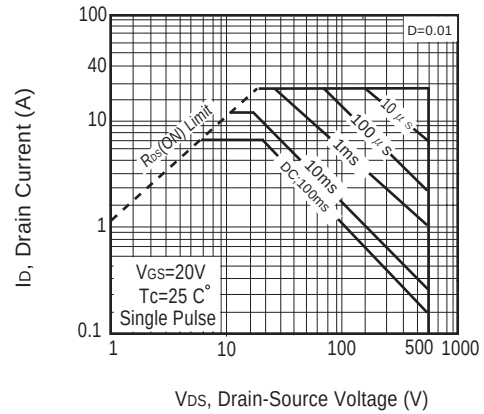


Figure 10. Maximum Safe Operating Area

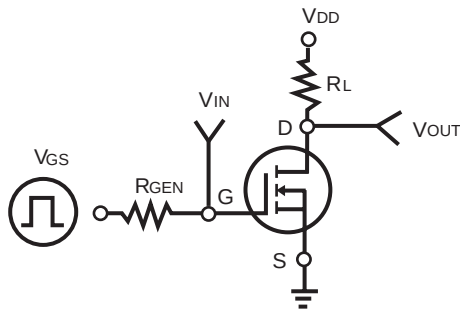


Figure 11. Switching Test Circuit

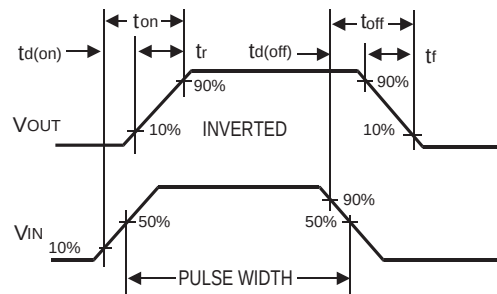


Figure 12. Switching Waveforms

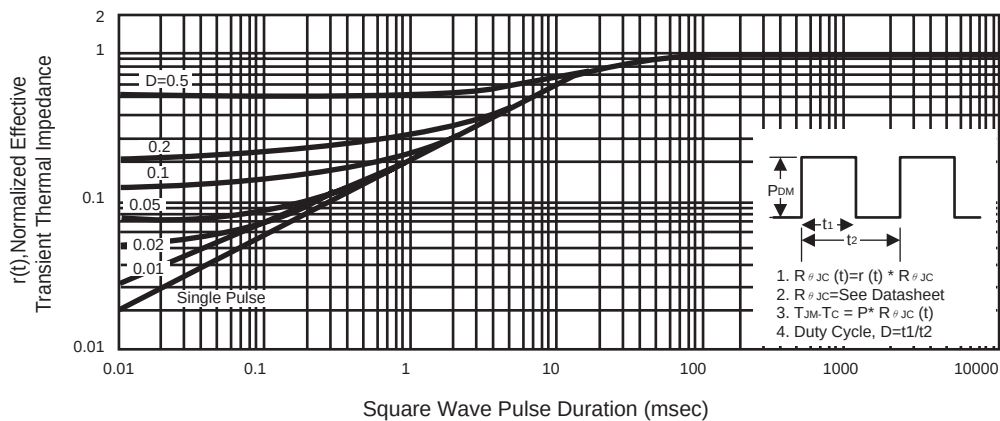


Figure 13. Normalized Thermal Transient Impedance Curve