CED21A2/CEU21A2

PRELIMINARY

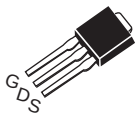
N-Channel Logic Level Enhancement Mode Field Effect Transistor

6

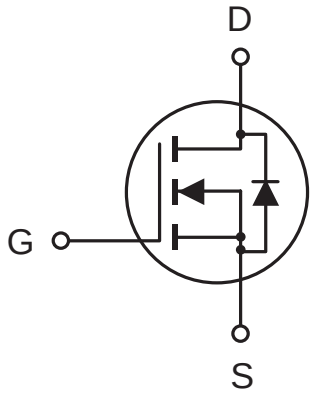
FEATURES

- 20V , 20A , $R_{DS(ON)}$=40mΩ @V_{GS}=4.5V.
  $R_{DS(ON)}$=70mΩ @V_{GS}=2.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-251 & TO-252 package.

CEU SERIES
TO-252AA(D-PAK)



CED SERIES
TO-251(I-PAK)



ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	20	A
-Pulsed	I_{DM}	60	A
Drain-Source Diode Forward Current	I_S	20	A
Maximum Power Dissipation @Tc=25°C	P_D	38	W
Derate above 25°C		0.25	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0V			±100	nA
ON CHARACTERISTICS[a]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.5		1.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 8A		30	40	mΩ
		V_{GS} = 2.5V, I_D = 6.6A		55	70	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	20			A
Forward Transconductance	g_{FS}	V_{DS} = 10V, I_D = 8A		15		S
DYNAMIC CHARACTERISTICS[b]						
Input Capacitance	C_{ISS}	V_{DS} =15V, V_{GS} = 0V f =1.0MHz		511		pF
Output Capacitance	C_{OSS}			216		pF
Reverse Transfer Capacitance	C_{RSS}			73		pF
SWITCHING CHARACTERISTICS[b]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 10V, I_D = 1A V_{GS} = 4.5V, R_{GEN} =6Ω		20	50	ns
Rise Time	t_r			12	30	ns
Turn-Off Delay Time	$t_{D(OFF)}$			50	100	ns
Fall Time	t_f			10	25	ns
Total Gate Charge	Q_g	V_{DS} = 10V,I_D = 8A V_{GS} = 4.5V		11	15	nC
Gate-Source Charge	Q_{gs}			3.6		nC
Gate-Drain Charge	Q_{gd}			2.8		nC

CED21A2/CEU21A2

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS [a]						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, Is = 4A			1.3	V

6

Notes

a.Pulse Test:Pulse Width≤300 μs, Duty Cycle≤ 2%.

b.Guaranteed by design, not subject to production testing.

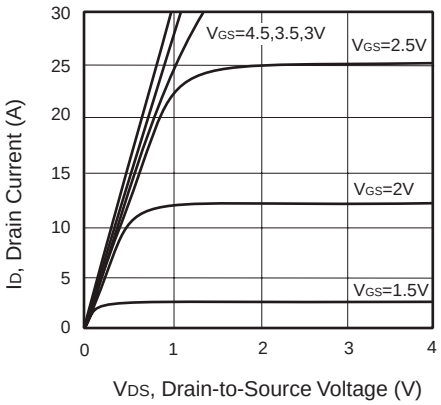


Figure 1. Output Characteristics

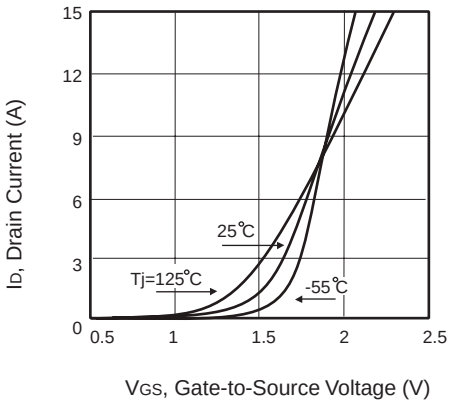


Figure 2. Transfer Characteristics

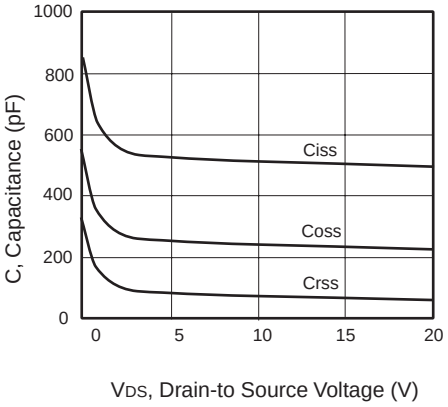


Figure 3. Capacitance

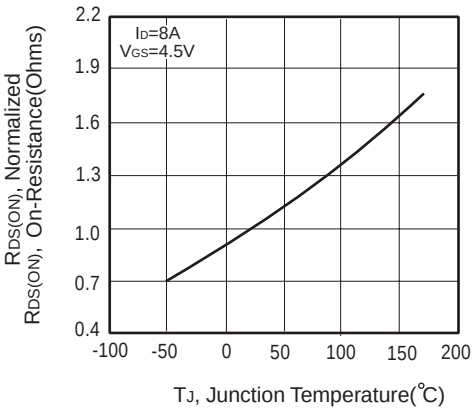


Figure 4. On-Resistance Variation with Temperature

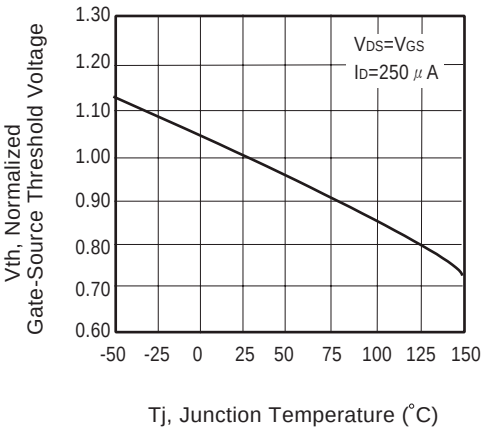


Figure 5. Gate Threshold Variation with Temperature

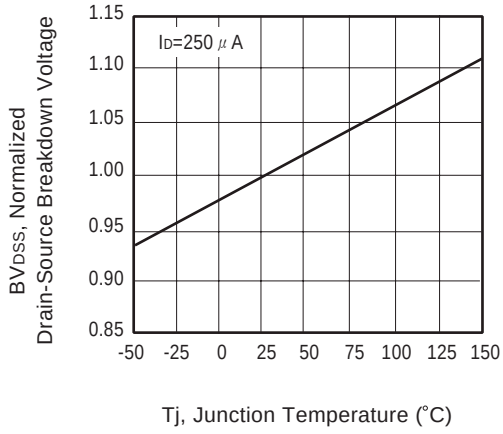


Figure 6. Breakdown Voltage Variation with Temperature

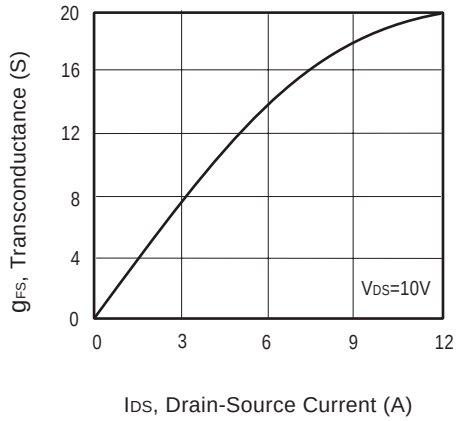


Figure 7. Transconductance Variation with Drain Current

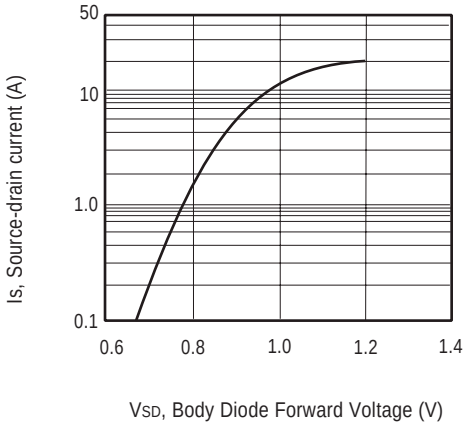


Figure 8. Body Diode Forward Voltage Variation with Source Current

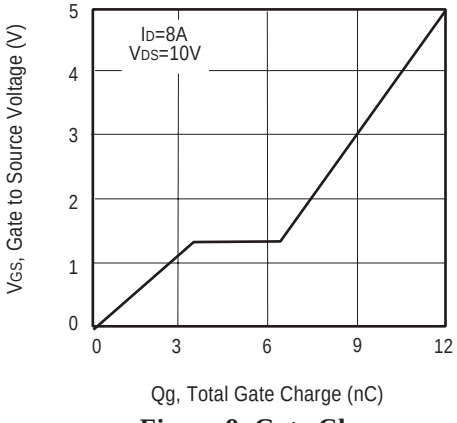


Figure 9. Gate Charge

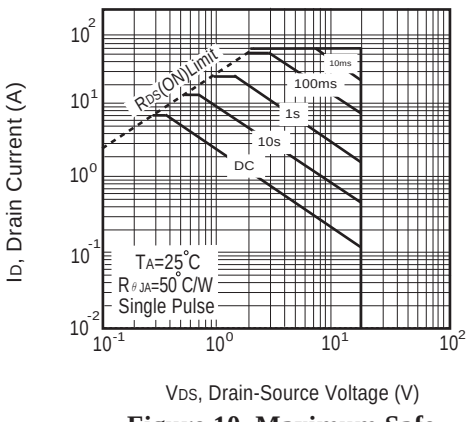


Figure 10. Maximum Safe Operating Area

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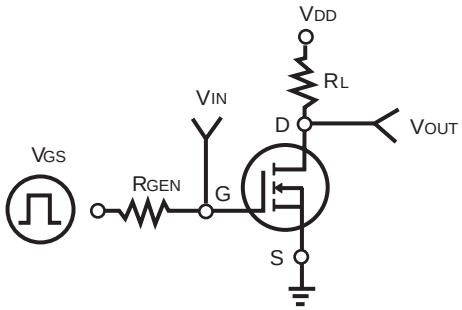

Figure 11. Switching Test Circuit

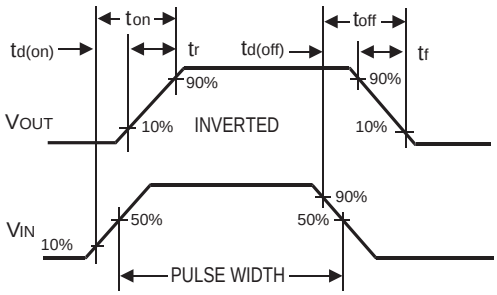

Figure 12. Switching Waveforms

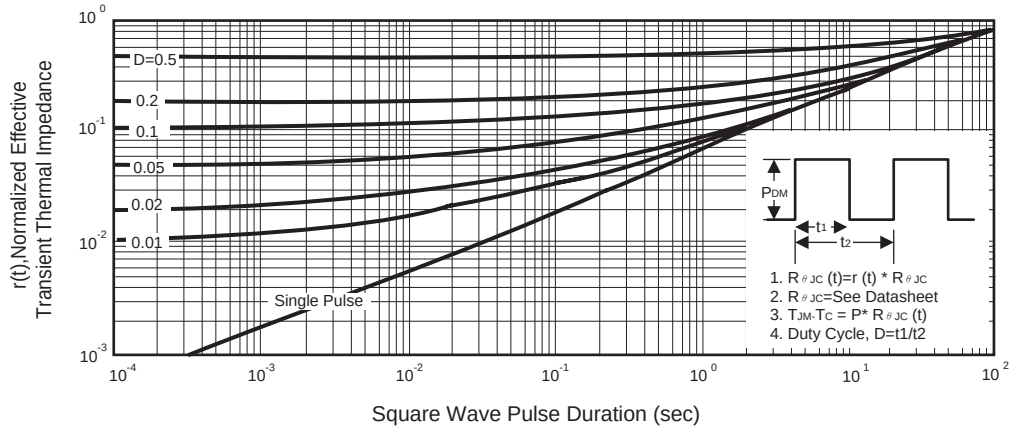

Figure 13. Normalized Thermal Transient Impedance Curve