DATA SHEET





# CG/CE46 0.65 Micron High Performance, Low Power CMOS Gate Arrays

### **Description**

The Fujitsu CG46 is a high performance, 0.65 µm drawn channel length, digital CMOS gate array family. The CE46 is a 0.65 µm drawn channel length, digital CMOS embedded gate array product family. The CE46 offers full support of diffused high speed RAMs, ROMs and embedded megacells. The CE46 series offers density and performance approaching that achievable with standard cell solutions but with the time to market advantage of traditional gate arrays. Both product families feature channelless (Sea-of-Gates) architecture with two layer metal.

A 5.0 volt product, the CG/CE46 features low power and high pin to gate count ratio. These product families are optimized for cost sensitive, high volume applications such as personal computers, workstations and communication systems. A wide variety of high performance and cost effective packages are available including PQFP, CQFP, TQFP, BGA and MCM's. Pin counts of up to 352 are available.

#### **Features**

- · 0.65 mm drawn channel length
- 5V  $\pm$  5% or 3.3V  $\pm$  0.3V supply voltage
- Channelless, Sea-of-gates Architecture
- Internal gate delay of 300ps, F/O = 2, L= 1mm @ 5.0V
- CE46 RAM compiler supports Single/Dual Port RAM
- Supports JTAG boundary scan, full and partial scan
- PCI buffer available
- Clock net for optimized on-chip clock skew control
- High drive capability: 3.2, 8, or 12 mA in a single I/O slot (24 mA available with double I/O)
- Optimized for 5V ±5%, capable of 3.3V ±0.3V
- Maximum toggle frequency is 175 MHz, Supports system clock frequencies in excess to 70 MHz
- CE46 Supports mixed 5V and 3.3V I/Os

- Supports all major third party design tools including Cadence, Mentor, Synopsys and Sunrise.
- Higher performance and 30% lower power than 0.8 µm technology
- · High pad to gate ratio

### **CE46 Embedded Gate Array Product Summary**

Device Name	Gross Gates	Usable Gates	Max. Pads	Metal Wiring
CE46F10	53,636	28,427	208	2
CE46F20	71,004	36,922	240	2
CE46F30	83,028	42,344	256	2
CE46F40	90,804	45,402	272	2
CE46F50	101,616	49,791	288	2
CE46F60	113,036	54,257	304	2
CE46F70	137,700	64,719	336	2
CE46F80	154,260	70,959	352	2
CE46F90	198,084	89,137	400	2

#### CG46 Gate Array Product Summary

Device Name	Gross Gates	Usable Gates	Max. Pads	Metal Wiring
CG46533	53,636	28,427	208	2
CG46713	71,004	36,922	240	2
CG46833	83,028	42,344	256	2
CG46104	101,616	49,791	288	2
CG46134	137,700	64,719	336	2
CG46194	198,084	89,137	400	2

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# **DC CHARACTERISTICS**

Measuring conditions:  $V_{DD}$  = 5V  $\pm$  5%, Vss = 0 V, Ta = 70  $^{\circ}$ C

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Parameter	Symbol	Test Conditions		Min.	Тур.	Max.	Unit
Supply Voltage	I <sub>DDS</sub>	Standby mode	Standby mode <sup>1</sup>			0.2 <sup>2</sup>	mA
		CMOS level	Normal cell	V <sub>DD</sub> x0.7	···	V <sub>DD</sub>	
			Schmitt trigger	V <sub>DD</sub> x0.8		V <sub>DD</sub>	V
High-level input voltage	V <sub>IH</sub>		Normal cell	2.2		$V_{DD}$	l
		TTL level	Schmitt trigger	2.4		$V_{DD}$	
Low-level input voltage		011001	Normal cell	V <sub>SS</sub>		V <sub>DD</sub> x0.3	
		CMOS level	Schmitt trigger	V <sub>SS</sub>		0.6	٧
	V <sub>IL</sub>	TTL level	Normal cell	V <sub>SS</sub>		0.8	
			Schmitt trigger	V <sub>SS</sub>		0.6	
		I <sub>OH</sub> =-2 mA <sup>3</sup>		4.0	*******		
High-level output voltage	V <sub>OH</sub>	I <sub>OH</sub> =-4 mA				V <sub>DD</sub>	V
		I <sub>OH</sub> =-8 mA					
		I <sub>OL</sub> =3.2 mA	I <sub>OL</sub> =3.2 mA				٧
l and land and and and and		I <sub>OL</sub> =8 mA		V <sub>SS</sub>		0.4	V
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> =12 mA					V
		I <sub>OL</sub> =24 mA				0.5	V
Input leakage current	ILI	V <sub>I</sub> =0 to V <sub>DD</sub>		<b>-</b> 5		5	μΑ
Input leakage current (Three-state pin input) <sup>4</sup>	$I_{LZ}$	VI=O 10 VDD		-5		5	_ μΛ
Input pull-up/pull-do <b>wn</b> resistors <sup>5</sup>	R <sub>P</sub>	Pull-up V <sub>I</sub> = V <sub>S</sub>	SS	25	50	100	kΩ
resistors <sup>5</sup>	$R_N$	Pull-down = V	= V <sub>DD</sub>	25	30	100	1,32

### NOTES:

- 1.  $V_{IH} = V_{dd}$  and  $V_{IL} = V_{SS}$ , the memory is in the standby mode
- 2. If an input buffer with pull-up/pull-down resistor is used, the supply current may not be assured depending on the circuit configuration.
- 3. The high level output voltage of the IOL=8mA type output buffer is identical to that (IOH = 2mA) of the IOL = 3.2mA type output buffer.
- 4. If an input buffer with pull-up/pull-down resistor is used, the input leakage current may exceed the above value.
- 5. Either a buffer without a resistor or with a pull-up/pull-down resistor can be selected from the input and biodirectional buffers.

### **ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol		Requirements			Unit		
Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> <sup>1</sup> -0.5 to +6.0				٧		
Input voltage	V <sub>I</sub>	V <sub>SS</sub> <sup>1</sup> -0.5 to V <sub>DD</sub> +0.5				V		
Output voltage	V <sub>O</sub>	V <sub>SS</sub> <sup>1</sup> -0.5 to V <sub>DD</sub> +0.5				°C		
0	-	Plastic -40 to +85				•c		
Operating temperature	Ta	Ceramic -55 to +125				1 ~		
Storage temperature	-	Plastic -40 to +85				- °C		
	T <sub>ST</sub>	Ceramic -65 to +150						
		Type/Cor	ndition	V <sub>O =</sub> V <sub>DD</sub>	Vo=OV			
		Normal Type	O <sub> L</sub> =3.2 mA	+40	-40	4		
0.44	lo <sup>3</sup>	Power-type	O <sub>IL</sub> =8 mA	+80	-40			
Output current	100	High-power type	O <sub>IL</sub> =12 mA	+120	-60	mA		
		Double high-power type	O <sub>IL</sub> ≖24 mA	+180	-90	7		
Overshoot	_	V <sub>SS</sub> <sup>1</sup> +1.0 V to max. <sup>2</sup>	/ <sub>SS</sub> <sup>1</sup> +1.0 V to max. <sup>2</sup>					
Undershoot		V <sub>SS</sub> <sup>1</sup> +1.0 V to max. <sup>2</sup>						

### NOTES:

- 1.  $V_{SS} = 0V$
- 2. For 50 ns max.
- 3. For one second per pin

# **RECOMMENDED OPERATING CONDITIONS (5.0V)**

Parameter Supply Voltage		Complete		Requirements				
		Symbol	Min.	Max.	Unit			
		$V_{DD}$	4.75	5.0	5.25	٧		
I l'ala la cal l'accest de la cal	CMOS level	V	V <sub>DD</sub> x0.7	_	$V_{DD}$	٧		
High-level input voltage	TTL level	<b></b>   ∨ <sub>iH</sub>	2.2	_	$V_{DD}$			
Lave lavel innut values	CMOS level	1,	V <sub>SS</sub> <sup>1</sup>	_	V <sub>DD</sub> x 0.3	٧		
Low-level input voltage	TTL level	<b>─</b> ┤∨⊩	V <sub>SS</sub> 1		0.8			
Operating temperature		Ta	0	25	70	°C		

### NOTES:

# **RECOMMENDED OPERATING CONDITIONS (3.3 V)**

Deservator	Combal		Requirements	Unit	
Parameter	Symbol	Min.	Тур.	Max.	) Unit
Supply Voltage	$V_{DD}$	3.0	3.3	3.6	٧
Operating temperature	Ta	0		70	°C

<sup>1.</sup>  $V_{SS} = 0V$ 

# INPUT/OUTPUT PIN CAPACITANCE

	Parameter		Requirements	Unit
Input pin		C <sub>IN</sub>	Max. 16	pF
Output pin	I <sub>OL</sub> = 3.2 mA, 8 mA, 12mA type		Max. 16	
	I <sub>OL</sub> = 24 mA type	C <sub>OUT</sub>	Max. 18	→ pF
I/O pin	I <sub>OL</sub> = 3.2 mA, 8 mA, 12mA type		Max. 16	
	I <sub>OL</sub> = 24 mA type	— c <sub>vo</sub>	Max. 18	→ pF

Measuring conditions:

T<sub>a</sub>=25 °C

V<sub>DD</sub>=V<sub>I</sub>=OV, f=1 MHz

## **PACKAGE AVAILABILITY**

Package					Array				
CE46 -	F10	F20	F30	F40	F50	F60	F70	F80	F90
CG46 -	533	713	833	•	104	_	134		194
QFP100	Р	Р	P	P	Р				
QFP160	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C
SQFP80	P	P	P						
SQFP100	P	P	P	P					
SQFP144	P	₽	P	P	P	P	P	P	
SQFP176	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C	
SQFP208	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C
SQFP240		P,C	P,C	P,C	P,C	P,C	P,C	P,C	P,C
SQFP256							P,C	P,C	P,C
TQFP100	Р	Р	P	P	P	Р	Р	P	
BGA256(B)			P	P	P	P	P	P	
BGA352(B)								Р	Р
BGA352(C)						P	P	Р	Р

NOTES: P: Plastic C: Cerquad

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# **DC CHARACTERISTICS at 3.3V Operating Conditions**

Measuring conditions:  $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{SS} = 0 V$ ,  $T_{A} = 0^{\circ} to 70^{\circ} C$ 

	0	T	1 One distance	R	equirement	S	A limits
Parameter	Symbol	Test Conditions		Min.	Тур.	Max.	Unit
Supply Current	I <sub>DDS</sub>	Standby mode *1		1 - 1		20 <sup>2</sup>	μА
	1.,	01400 11	Normal cell * 3	V <sub>DD</sub> x0.7	_	$V_{DD}$	
High-level input voltage	V <sub>IH</sub>	CMOS level	Schmitt trigger * 4	V <sub>DD</sub> x0.8	<del>-</del>	$V_{DD}$	] ,
		0110011	Normal cell * 3	V <sub>SS</sub>	_	$V_{DD}$	1
Low-level input voltage	V <sub>IL</sub>	CMOS level	Schmitt trigger * 4	V <sub>SS</sub>		$V_{DD}$	1
		I <sub>OH</sub> = -1 mA *	5				
	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA * <sup>6</sup>		V <sub>DD</sub> -0.3	-	V <sub>DD</sub>	v
High-level output voltage		I <sub>OH</sub> = -2 mA <sup>+7</sup>					
		I <sub>OH</sub> = -4 mA * 8					
		$I_{OL} = 2 \text{ mA} * 5$	I <sub>OL</sub> = 2 mA * <sup>5</sup>		-	0.4	V
1 1111	l <sub>v</sub>	I <sub>OL</sub> = 4 mA * <sup>6</sup>					V
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 6 mA * <sup>7</sup>		V <sub>SS</sub>			٧
		I <sub>OL</sub> = 12 mA * 8					V
Input pull-up/pull-down resistors *4	R <sub>P</sub>	Pull-up V <sub>I</sub> = V <sub>S</sub>	SS	40	150	350	kΩ
resistors *4	$R_N$	Pull-down = V <sub>l</sub>	= V <sub>DD</sub>	40	100	200	7 ~~

#### NOTES:

- \*1.  $V_{IH} = V_{DD}$  and  $V_{IL} = V_{SS}$ , the memory is in the standby mode.
- \*2. If an input buffer with pull-up/pull-down resistor is used, the supply current may not be assured depending on the circuit configuration.
- \*3. Equivalent to CMOS Input terminal.
- \*4. Equivalent to CMOS Schmitt Input terminal.
- \*5. Equivalent to IOL= 3.2mA ouput (at VDD = 5V).
- \*6. Equivalent to IOL= 8mA ouput (at VDD = 5V).
- \*7. Equivalent to IOL= 12mA ouput (at VDD = 5V).
- \*8. Equivalent to IOL= 24mA ouput (at VDD = 5V).

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This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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