VITELIC

V61C30 FAMILY
HIGH PERFORMANCE LOW POWER
8,192 BIT
CMOS DUAL PORT MEMORY
VICMOS TECHNOLOGY

Features

- 1K x 8 bit CMOS Static RAM with 3-state outputs
- Dual-port with on-chip arbitration logic
- High speed
  - 55 ns, 70 ns, 90 ns access time
- Battery backup 2 volt data retention
- Low power operation
  - operating 325 mW (typ)
  - standby 15 μW (typ)
- VICMOS process virtually eliminates alpha particle induced soft errors without die coating
- Full CMOS memory cell
- Both ports fully asynchronous
- Single 5 volt power supply
- TTL compatible
- 48 pin DIP, 52 pin PLCC, 48 Ceramic LCC
- Replaces 7130, 2130, and equivalent devices

Description

The Vitelic V61C30 is a CMOS 1K x 8 high speed dual-port static RAM with advanced arbitration logic that provides access to both ports simultaneously. Fabrication with the VICMOS technology provides a high performance, low power alternative to NMOS memory.

The Vitelic V61C30 provides two parallel 8-bit ports with separate controls, addresses, and I/O, permitting read or write access to any memory location. Automatic power-down circuitry permits a port to be placed in the standby mode when $\overline{CE}$ is high.

The $\overline{BUSY}$ signal is used to indicate an attempt by both ports to simultaneously access the same address location. The signal may be ignored or acted upon as required by system design. If both ports are attempting to read or write, data can be compromised and $\overline{BUSY}$ will be asserted on the port denied access.

The interrupt flag, $\overline{INT}$, permits communication between memory ports and systems. By writing and reading the two high-order locations in memory, the two interrupt flags $\overline{INTL}$ and $\overline{INTR}$ can be set and reset. The $\overline{INTL}$ flag is set only by the right port writing location 3FE (Hex) and cleared by the left port reading location 3FE (Hex). The $\overline{INTR}$ flag is set only by the left port writing location 3FF (Hex) and cleared by the right port reading location 3FF (Hex). By using the $\overline{INT}$ flags and the contents of locations 3FE and 3FF (Hex), mailbox or arbitration functions can be implemented. The $\overline{INT}$ flags are open-drain.

The Vitelic V61C30 offers a battery backup data retention mode where the device typically consumes only 2.5 μW from a 2 volt source.

The Vitelic V61C30 comes in either a 48 pin dual-inline package for insertion into mounting holes on 600 mil (15.2 mm) centers or 52 pin PLCC.

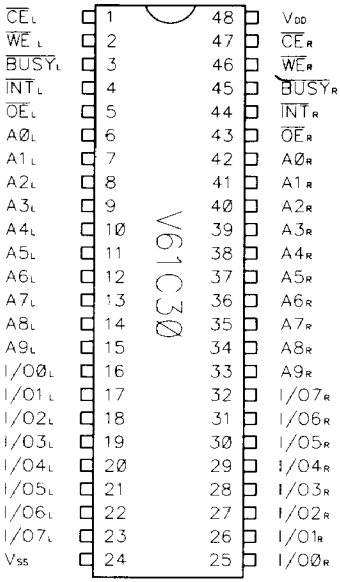
Device Usage Chart

Operating Temperature Range	Package Outline				Access Time (ns)			Power		Temperature Mark
	P	C	G	J	55	70	90	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	•	•	Blank

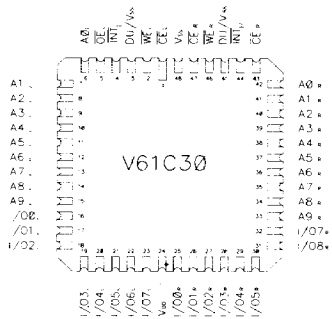
Package	Std.	Pin Count
Plastic DIP	P	48
PLCC (J Lead)	J	52
Ceramic Side Brazed	C	48
Ceramic LCC	G	48

V__C____
Family Device Package Speed Power Temp

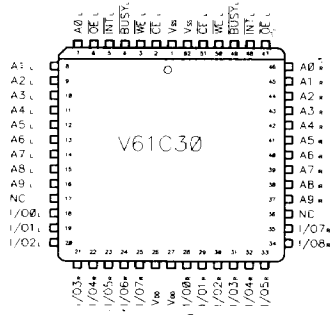
DIP
PIN CONFIGURATION
Top View



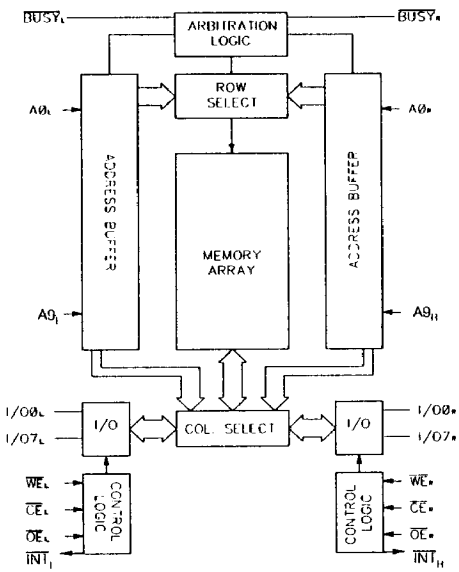
LCC
PIN CONFIGURATION
Top View



PLCC
PIN CONFIGURATION
Top View



BLOCK DIAGRAM



Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Unit
V_{TERM} (2)	Terminal Voltage with Respect to V_{SS}	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−40 to +85	°C
T_{STG}	Storage Temperature	−55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Operation at or near absolute maximum ratings can affect device reliability.
2. −3.5V for less than 30 ns.

Capacitance

T_A = +25°C, f = 1.0 MHz

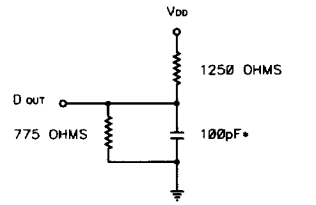
Symbol	Parameter	Conditions	Max.	Unit
C_{OUT}	Output Capacitance	V_{IN} = 0V	5	pF
C_{IN}	Input Capacitance	V_{OUT} = 0V	5	pF

NOTE:

This parameter is sampled and not 100% tested.

A.C. Test Conditions

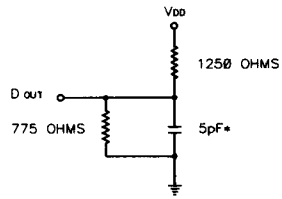
Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3



OUTPUT LOAD A

*Includes test fixture and scope capacitance

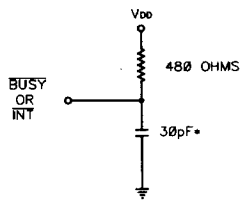
Fig. 1



OUTPUT LOAD B

(for t_{HZ}, t_{LZ}, and t_{OW})

Fig. 2



OUTPUT LOAD C

Fig. 3

Truth Tables

Non-Contention Read/Write Control

LEFT PORT INPUTS (1)			RIGHT PORT INPUTS (1)			FLAGS (2)		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	H	X	X	X	X	H	H	Left Port in Power Down Mode
X	X	X	X	H	X	H	H	Right Port in Power Down Mode
L	L	X	X	X	X	H	H	Data on Left Port Written Into Memory
H	L	L	X	X	X	H	H	Data in Memory Output on Left Port
X	X	X	L	L	X	H	H	Data on Right Port Written Into Memory
X	X	X	H	L	L	H	H	Data in Memory Output on Right Port

NOTES:
1. A_{0L}-$A_{9L} \neq A_{0R}$-A_{9R}
2. $\overline{INT}$ Flags are in the don't care state. H = HIGH, L = LOW, X = DON'T CARE

Interrupt Flag

LEFT PORT					RIGHT PORT					FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L	Set $\overline{INT}_R$ Flag
X	X	X	X	X	H	L	L	3FF	H	Reset $\overline{INT}_R$ Flag
X	X	X	X	L	L	L	X	3FE	X	Set $\overline{INT}_L$ Flag
H	L	L	3FE	H	X	X	X	X	X	Reset $\overline{INT}_L$ Flag

NOTE:
1. H = HIGH, L = LOW, X = DON'T CARE

$\overline{CE}$ Arbitration with Address Match Before $\overline{CE}$

LEFT PORT				RIGHT PORT				FLAGS (1)		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	LBR	X	MATCH	X	L	X	MATCH	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	MATCH	X	LBL	X	MATCH	L	H	Left Operation Not Permitted Right Operation Permitted
X	LST	X	MATCH	X	LST	X	MATCH	H	L	Left Operation Permitted Right Operation Not Permitted

Address Arbitration with $\overline{CE}$ Low Before Address Match

LEFT PORT				RIGHT PORT				FLAGS (1)		FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	L	X	VBR	X	L	X	VALID	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	VALID	X	L	X	VBL	L	H	Left Operation Not Permitted Right Operation Permitted
X	L	X	VST	X	L	X	VST	H	L	Left Operation Permitted Right Operation Not Permitted

NOTE:
1. $\overline{INT}$ Flags are in the don't care state.
X = DON'T CARE, L = LOW, H = HIGH, LST = Low Same Time, LBR = Low Before Right, LBL = Low Before Left

D.C. Electrical Characteristics

V_{DD} = 5V ±10%, T_A = 0°C to +70°C

Symbol	Parameter	Test Conditions	V61C30			V61C30-L			Unit
			Min.	Typ. (1)	Max.	Min.	Typ. (1)	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = 5.5V, V_{IN} = 0V to V_{DD}	—	—	10	—	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{DD}	—	—	10	—	—	5	µA
V_{IH}	Input High Voltage		2.2	—	6.0	2.2	—	6.0	V
V_{IL}	Input Low Voltage		−1.0(2)	—	0.8	−1.0(2)	—	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open	—	65	100	—	65	100	mA
I_{SB1}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}	—	15	25	—	10	15	mA
I_{SB2}	Standby Current (One Port Standby)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH} Active Port Outputs Open	—	40	60	—	40	60	mA
I_{SB3}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} − 0.2V V_{IN} ≥ V_{DD} − 0.2V or V_{IN} ≤ 0.2V	—	5	10000	—	3	100	µA
I_{SB4}	Full Standby Current (One Port Full Standby)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{DD} − 0.2V V_{IN} ≥ V_{DD} − 0.2 or V_{IN} ≤ 0.2V Active Port Outputs Open	—	35	50	—	35	50	mA
V_{OL}	Output Low Voltage (I/O_0–I/O_7)	I_{OL} = 3.5 mA	—	—	0.4	—	—	0.4	V
		I_{OL} = 8 mA	—	—	0.5	—	—	0.5	
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 8 mA	—	—	0.5	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA	2.4	—	—	2.4	—	—	V

NOTES:

1. V_{DD} = 5V, T_A = +25°C.
2. V_{IL} (min) = −3.5V for pulse width less than 30 ns.

A.C. Electrical Characteristics

Read Cycle

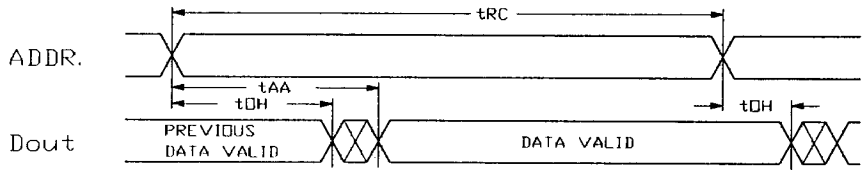
V_{DD} = 5V ±10%, T_A = 0°C to +70°C

Symbol	Parameter	55		70		90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55	—	70	—	90	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	90	ns
t_{ACE}	Chip Enable Access Time	—	55	—	70	—	90	ns
t_{AOE}	Output Enable Access Time	—	20	—	25	—	40	ns
t_{OH}	Output Hold From Address Change	10	—	10	—	10	—	ns
t_{LZ}	Output Low-Z Time (1)	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time (1)	—	20	—	30	—	40	ns
t_{PU}	Chip Enable to Power Up Time	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time	—	35	—	40	—	50	ns

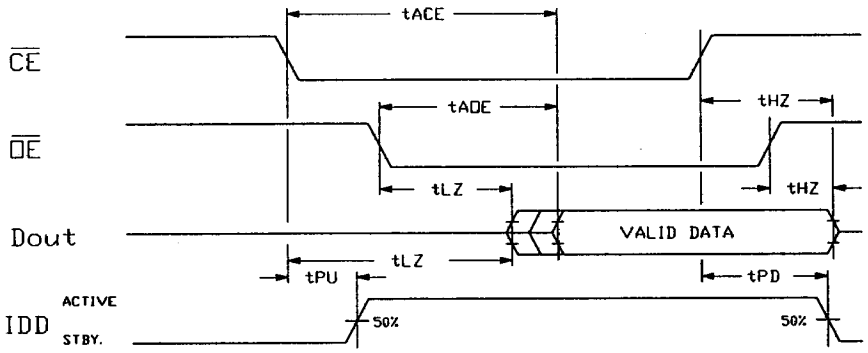
NOTE:

1. Transition is measured ±500 mV from low or high state with load (Figures 1, 2, and 3). This parameter is sampled and not 100% tested.

Timing Waveform of Read Cycle No. 1 Either Side (1, 2, 6)



Timing Waveform of Read Cycle No. 2 Either Side *(1, 3)*



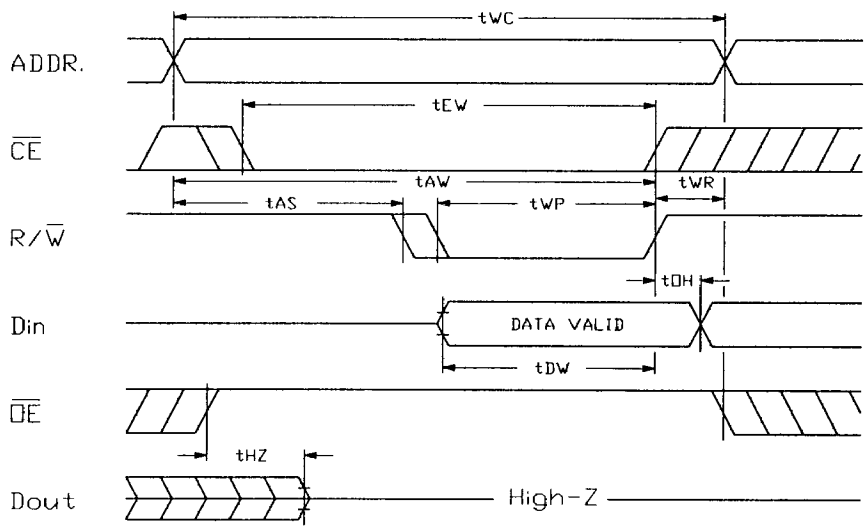
Write Cycle

Symbol	Parameter	55		70		90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	55	—	70	—	90	—	ns
t_{EW}	Chip Enable to End of Write	50	—	65	—	85	—	ns
t_{AW}	Address Valid to End of Write	50	—	65	—	85	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	30	—	40	—	50	—	ns
t_{HZ}	Output High-Z Time (1)	—	20	—	30	—	40	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High-Z (1)	0	25	0	35	0	40	ns
t_{OW}	Output Active From End of Write (1)	0	—	0	—	0	—	ns

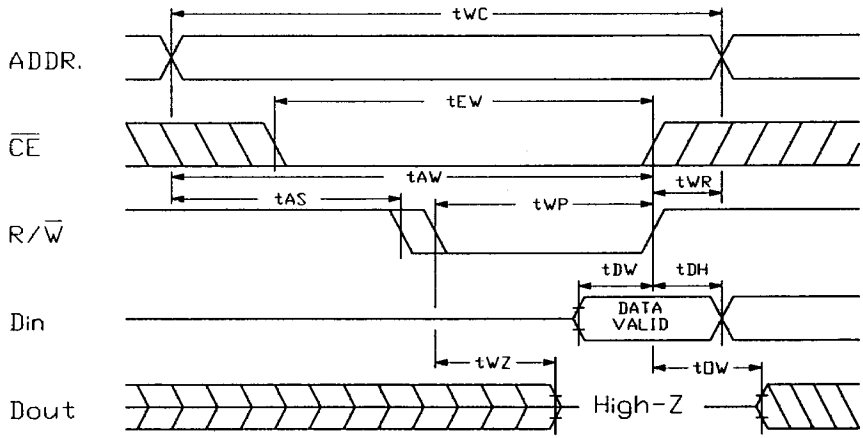
NOTE:

1. Transition is measured ±500 mV from low or high state with load (Figures 1, 2, and 3). This parameter is sampled and not 100% tested.

Timing Waveform of Write Cycle No. 1 Either Side (4, 7)



Timing Waveform of Write Cycle No. 2 Either Side *(4, 7)*

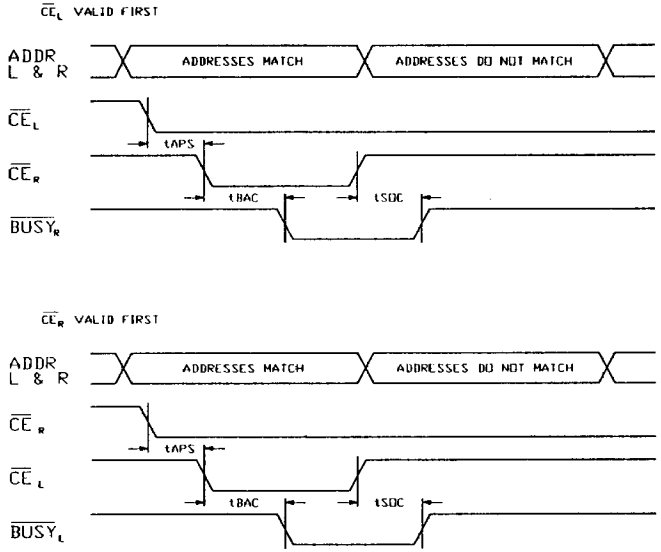


Busy Timing

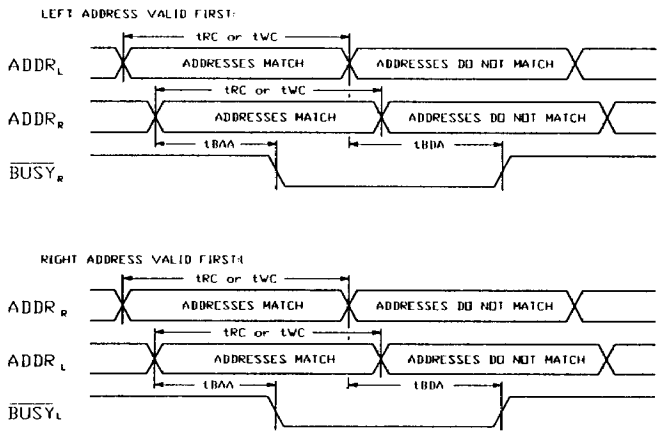
V_{DD} = 5V ±10%, T_A = 0°C to +70°C.

Symbol	Parameter	55		70		90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55	—	70	—	90	—	ns
t_{WC}	Write Cycle Time	55	—	70	—	90	—	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	40	—	40	—	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	45	—	45	—	45	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	—	40	—	40	—	45	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	—	45	—	45	—	45	ns
t_{APS}	Arbitration Priority Setup Time	10	—	10	—	10	—	ns

Timing Waveform of Contention Cycle No. 1



Timing Waveform of Contention Cycle No. 2 (5)



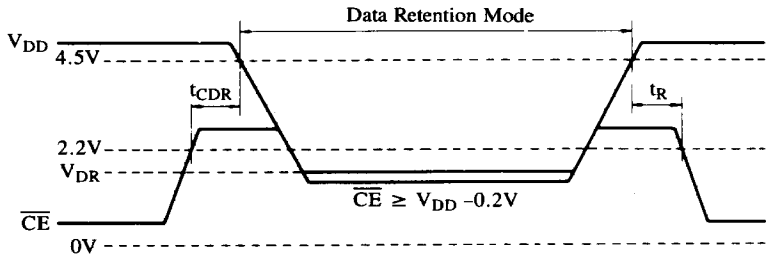
Data Retention Characteristics

For V61C30L Only

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Retention Data		2.0	—	—	V
I_{DDDR}	Data Retention Current	V_{DD} = 3.0V, $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$	—	3	100	μA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
t_R	Operation Recovery Time		t_{RC}*	—	—	ns

*t_{RC} = Read Cycle Time

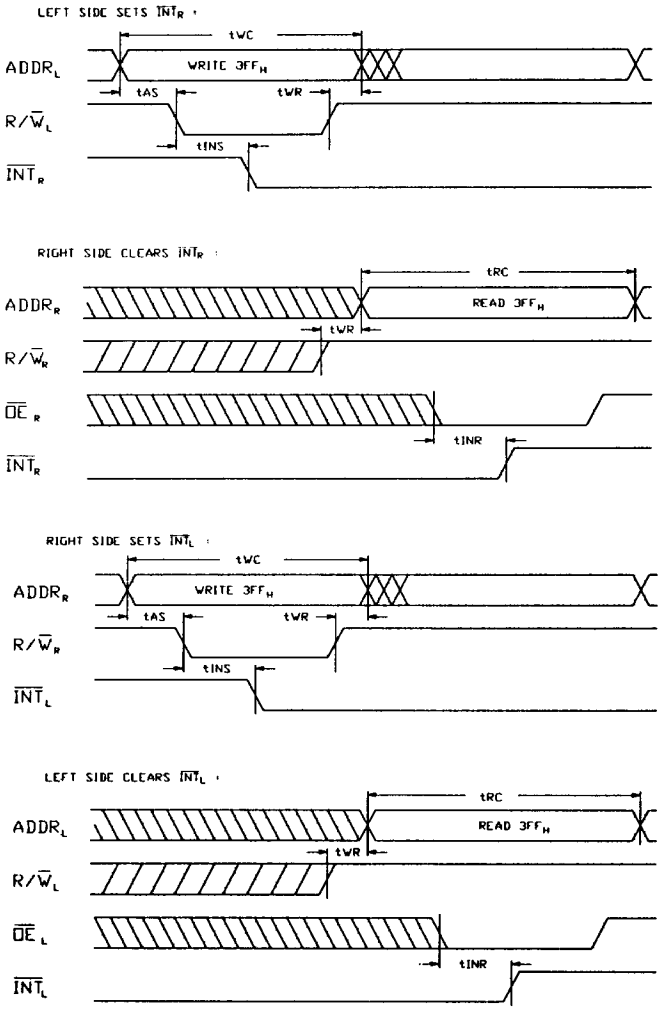
Low V_{DD} Data Retention Waveform



Interrupt Timing

Symbol	Parameter	55		70		90		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set Up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	40	—	45	—	55	ns
t_{INR}	Interrupt Reset Time	—	50	—	55	—	55	ns

Timing Waveform of Interrupt Mode (5, 8)



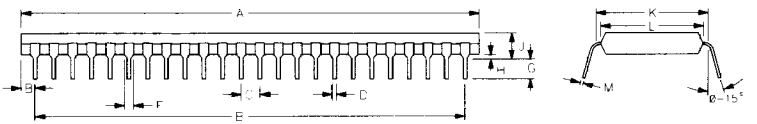
NOTES:

1. R/$\overline{W}$ is high Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}.
6. $\overline{OE}$ = V_{IL}.
7. R/$\overline{W}$ = V_{IH} during address transition.
8. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

Package Outline

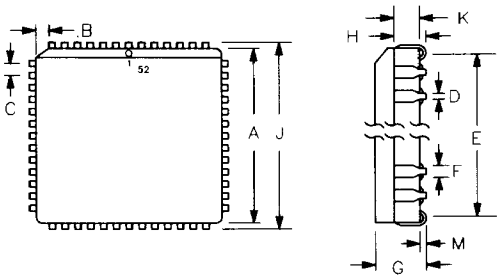
48 Pin Plastic

Item	Inches	Millimeters
A	2.460 max.	62.484 max.
B	.080	2.032
C	.1	2.54
D	.015/.020	.381/.508
E	2.3	58.42
F	.040/.065	1.016/1.651
G	.125/.160	3.175/4.064
H	.015/.065	.381/1.651
J	.160/.225	4.064/5.715
K	.590/.610	14.986/15.494
L	.530/.550	13.462/13.970
M	.009/.012	.229/.305



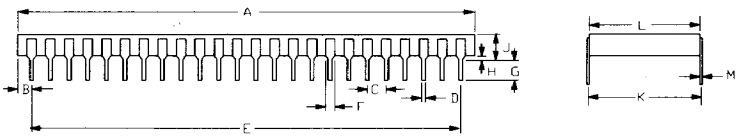
52 Pin PLCC-J

Item	Inches	Millimeters
A	.760 max.	19.30 max.
B	.045	1.14
C	.050 typ.	1.27 typ.
D	.017 typ.	.43 typ.
E	.730 max.	18.54 max.
F	.026/.032	.66/.81
G	.180 max.	4.57
H	.098 nom.	2.49
J	.795	20.19
K	.055 nom.	1.40
M	.030/.045	.76/1.14



48 Pin Ceramic Side Brazed

Dimension	Inches	Millimeters
A	2.430 max.	61.722 max.
B	.065	1.651
C	.100	2.54
D	.015/.023	.381/.584
E	2.300	58.42
F	.038/.060	.965/1.524
G	.120/.160	3.048/4.064
H	.030/.070	0.762/1.778
J	.100/.200	2.54/5.08
K	.590/.620	14.986/15.748
L	.550/.610	13.97/15.494
M	.008/.012	.203/.305



48 Pin CLCC

Dimension	Inches	Millimeters
A	.554/.572	14.072/14.529
B	.045/.055	1.143/1.397
C	.037/.043	.94/1.092
D	.015/.025	.381/.635
E	.434/.446	11.024/11.328
J	.065/.125	1.651/3.175