T-42-11-09

Application Specific ICs

CGA100 Series

Advance Information

Advanced Continuous Gate* Technology 1.5-Micron CMOS Gate-Array Series

Features:

- *Continuous Gate architecture offers maximum layout efficiency with 75% gate utilization*
- *Available in seven sizes from 9,000 to 50,000 usable gates (12,149 to 66,550 available gates)*
- *Proven 1.5-micron (drawn) silicon-gate double-level-metal CMOS technology*
- *High performance with balanced drive–0.95 ns typical for a 2-input NAND gate with a fanout of 2*
- *TTL, CMOS, and Schmitt Trigger I/O compatibility*
- *Programmable output drive from 2 to 12 mA*
- *Separate I/O and core power bus capability for noise reduction*
- *Extensive Macro library*
- *Workstation support for schematic capture and simulation*
- *Fully supported by GE/RCA's integrated CAE tools*
- *Available with Class B type screening for high-reliability applications*

The GE/RCA CGA100 Series is an advanced, high-performance, CMOS gate-array family using GE/RCA's proprietary Continuous Gate technology in which high transistor densities are achieved by means of a special array architecture. Continuous Gate technology along with a unique global routing scheme enable the CGA100 Series to offer maximum layout efficiency in which 75% of the total gates can be utilized. With its extremely high performance, high gate count, and high layout efficiency, the CGA100 Series is ideally suited to meet the user's design requirements for complex systems integration and low power consumption.

Designed with true 1.5-micron silicon-gate design rules, the CGA100 Series is fabricated on an advanced, double-level-metal, planarized, fully-implanted CMOS process. With typical effective channel lengths of 1.1 microns and reduced junction area capacitance, the CGA100 Series allows system clock speeds of up to 40 MHz. An internal 2-input NAND gate, with a fanout of 2 exhibits a typical propagation delay of just 0.95 ns. Operating from a single 5-volt power supply, the CGA100 Series of gate arrays exhibits extremely low power dissipation, typically 20 μW/gate/MHz.

In addition to standard commercial product, the CGA100 Series of gate arrays are available with Class B-type screening for applications requiring high reliability and −55° C to +125° C temperature-range operation.

CGA100 Gate-Array Series

DEVICE NUMBER	EQUIVALENT GATES[1]	ESTIMATED USABLE GATES[2]	MAXIMUM I/O PADS[3]
CGA100-121	12,149	9,000	152
CGA100-160	16,038	12,000	172
CGA100-205	20,465	15,000	196
CGA100-270	26,950	20,000	224
CGA100-397	39,700	30,000	272
CGA100-528	52,800	40,000	312
CGA100-665	66,550	50,000	348

1. An equivalent gate is defined as one 2-input NAND.
2. The estimated number of usable gates is 75% of the available gate count. The actual number of usable gates may vary, depending on the design.
3. Eight additional pads are dedicated as V_{SS} pads. All I/O pads are programmable to V_{DD} or V_{SS}.

*Advanced Continuous Gate is a Trademark of VLSI Technology, Inc.

File Number **2085**

MAXIMUM RATINGS, *Absolute-Maximum Values:*
(Voltages referenced to V_{SS} Terminal)

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) ..... -0.5 to +6 V
RECOMMENDED DC OPERATING VOLTAGE RANGE (V_{DD}) ..... 1.5 to 5.5 V
DC INPUT VOLTAGE RANGE, ALL INPUTS, (V_{IN}) ..... -0.5 to V_{DD} +0.5 V
DC OUTPUT VOLTAGE RANGE, ALL OUTPUTS, (V_{OUT}) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±20 mA
POWER DISSIPATION PER PACKAGE (P_D):
For Standard Temperature Range: -40 to +85°C
For T_A=-40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For External Temperature Range: -55 to +125°C
For T_A=-55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A=+100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
POWER DISSIPATION PER OUTPUT (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D (CERAMIC) ..... -55 to +125°C
PACKAGE TYPE E (PLASTIC) ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

DC CHARACTERISTICS, Specified at V_{DD} and Ambient Temperature over the Designated Range[1]

CHARACTERISTIC		TEST CONDITIONS	MIN.	MAX.	UNITS
Input HIGH Voltage CMOS TTL	V_{IH}	Guaranteed Input HIGH Voltage	0.7 x V_{DD} 2	V_{DD} V_{DD}	V
Input LOW Voltage CMOS TTL	V_{IL}	Guaranteed Input LOW Voltage	-0.5 -0.5	0.3 x V_{DD} 0.8	V
Schmitt-Trigger Positive-Going Threshold	V_T+		2.2	—	V
Schmitt-Trigger Negative-Going Threshold	V_T-		—	1.3	V
Output HIGH Voltage PC7O01 PC7O02 PC7O03 PC7O04	V_{OH}	I_{OH} = -1 µA I_{OH} = -2 mA I_{OH} = -4 mA I_{OH} = -8 mA I_{OH} = -12 mA	V_{DD} - 0.05 2.4 2.4 2.4 2.4	— — — — —	V
Output LOW Voltage PC7O01 PC7O02 PC7O03 PC7O04	V_{OL}	I_{OL} = 1 µA I_{OL} = 2 mA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA	— — — — —	0.05 0.4 0.4 0.4 0.4	V
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} or Gnd	-10	10	µA
3-State Output Leakage Current	I_{OZ}	V_{OUT} = V_{DD} or Gnd	-10	10	µA

CAPACITANCE, Specified at V_{DD} and Ambient Temperature Over the Designated Range[1]

CHARACTERISTIC[2]		TEST CONDITIONS	MIN.	MAX.	UNITS
Input Pad Capacitance	C_{IN}	Excluding Package	—	5	pF
Output Pad Capacitance	C_{OUT}				
Transceiver Pad Capacitance	$C_{I/O}$				

1. Military range is -55°C to +125°C, ± 10% power supply; industrial temperature range is -40°C to +85°C, ± 5% power supply; commercial temperature range is 0°C to +70°C, ± 5% power supply.
2. For cell pads only.

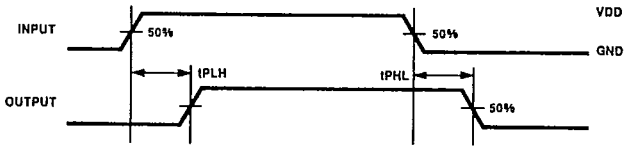
AC CHARACTERISTICS FOR SELECTED MACROS, T_J = 27°C, V_{DD} = 5 V, Process Model = Typical

MACRO	DESCRIPTION	SYMBOL	PROPAGATION DELAY (ns) - FANOUT				
			1	2	3	4	6
Logic Gates							
IN01D1	1X Inverting Buffer	t_{PLH}	0.57	0.72	0.87	1.02	0.31
		t_{PHL}	0.42	0.54	0.65	0.76	0.99
IN01D2	2X Inverting Buffer	t_{PLH}	0.34	0.43	0.51	0.60	0.77
		t_{PHL}	0.26	0.32	0.38	0.43	0.54
ND02D1	2-Input NAND	t_{PLH}	0.68	0.84	1.00	1.16	1.47
		t_{PHL}	0.86	1.05	1.24	1.42	1.80
ND04D1	4-Input NAND	t_{PLH}	1.46	1.62	1.78	1.94	2.25
		t_{PHL}	2.05	2.17	2.29	2.41	2.65
NR02D1	2-Input NOR	t_{PLH}	1.34	1.64	1.94	2.24	2.84
		t_{PHL}	0.63	0.75	0.86	0.97	1.19
NR04D1	4-Input NOR	t_{PLH}	2.14	2.29	2.45	2.61	2.93
		t_{PHL}	1.41	1.52	1.64	1.75	1.97
XN02D1	2-Input Exclusive-NOR	t_{PLH}	1.05	1.22	1.39	1.56	1.89
		t_{PHL}	0.86	0.99	1.12	1.25	1.51
PT05D1	Inverting Pad Driver	t_{PLH}	1.34	1.64	1.94	2.24	2.84
		t_{PHL}	1.63	1.85	2.08	2.30	2.75
Flip-Flops & Latches							
DFNTNB	Buffered D Flip-Flop (Clock → Q)	t_{PLH}	3.01	3.16	3.31	3.46	3.76
		t_{PHL}	3.70	3.81	3.93	4.04	4.26
		t_S	1.50	1.50	1.50	1.50	1.50
		t_H	0	0	0	0	0
LANFNB	Buffered Latch (D → Q)	t_{PLH}	1.92	2.07	2.22	2.32	2.67
		t_{PHL}	2.15	2.27	2.39	2.51	2.76
		t_S	1.10	1.10	1.10	1.10	1.10
		t_H	0	0	0	0	0
Input Buffers							
PC7T00	TTL Input Buffer	t_{PLH}	2.65	2.70	2.70	2.81	2.91
		t_{PHL}	2.96	2.96	3.01	3.11	3.21
PC7C00	CMOS Input Buffer	t_{PLH}	0.99	1.04	1.09	1.15	1.25
		t_{PHL}	1.13	1.17	1.21	1.25	1.33
Output Buffers							

MACRO	DESCRIPTION	SYMBOL	CAPACITIVE LOAD (pF)			
			15	50	85	100
PC7C13	Output Buffer with 8-mA Drive	t_{PLH}	2.44	5.72	9.00	10.40
		t_{PHL}	2.31	3.95	5.59	6.29

TIMING DIAGRAM

PROPAGATION DELAY



AC Performance

AC performance for a given operating condition is a function of several factors including: fanout, interconnect, supply voltage, junction temperature, and process variability.

The AC characteristics table shows the propagation delay (TDNOM) on a number of commonly used macros for a typical process model, 5-volt operation, and 27° C junction temperature.

The effect of supply voltage can be determined from Fig. 1 by extracting the factor KV. Fig. 2 is used to determine the temperature factor KT. A worst-case process factor (KPMAX) of 1.45, and a best-case process factor (KPMIN) of 0.67. as shown in Fig. 3, are used to determine the effects of process variability.

The worst-case propagation delay can be calculated as follows:

TDMAX = KV x KT x KPMAX x TDNOM

and the best-case delay is calculated:

TDMIN = KV x KT x KPMIN x TDNOM

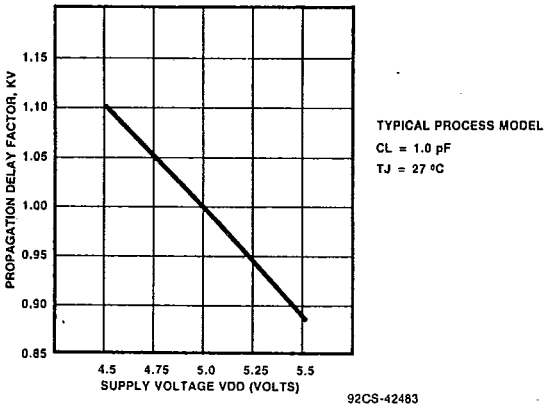


Fig. 1 - Performance vs voltage.

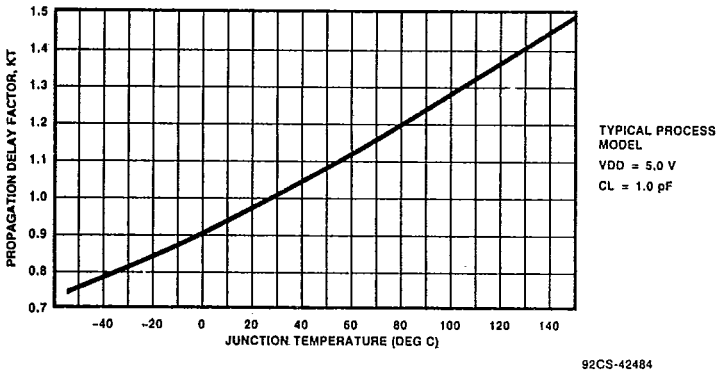


Fig. 2 - Performance vs temperature.

PROCESS FACTOR, KP

Process Model	Factor KP
Slow	1.45
Typical	1
Fast	0.67

92CS-42485

Fig. 3 - Performance vs process.

Array Organization

The general layout of the CGA100 Series consists of electrical components that are organized as structures of continuous arrays of transistor pairs. Macro cells, which are the basic building blocks of logic design, are comprised of one or more transistor pairs in the arrays. All of the CGA100 Series gate arrays use the same transistor array and I/O cell structure. The power busing structure of the CGA100 Series can isolate the I/O cells from the internal array. Both the VDD and the VSS buses surround the array in the second-level metal and are brought into the internal array via a power rail structure. The power bus structure also allows any pad to be programmed as VDD or VSS.

Internal Array Description

The CGA100 Series, using Continuous Gate technology, consists internally of rows of uncommitted P and N transistors laid out at continuous regular intervals. Key features of the Continuous Gate technology are:

1. High gate density arising from special array architectural features.
2. A unique global routing scheme that maximizes gate utilization, and allows for faster place and route.

Special architectural features include the use of gate isolation, and the use of specially contoured diffusion and poly nodes. In the traditional approaches, active regions are isolated from one another by a thick field oxide. This is referred to as oxide isolation and may consume 20% of the total core area. In comparison, the gate isolation technique employed in Continuous Gate technology turns off transistors to isolate active regions from one another. These isolation transistors are placed only where needed, therefore achieving higher silicon efficiency.

Specially contoured diffusion and poly nodes are used throughout the array to minimize the vertical metal routing required to connect each of the nodes. This in turn, allows for more horizontal metal routing tracks to be available, thus increasing routing efficiency and silicon utilization.

The global routing scheme for gate arrays built on the Continuous Gate technology architecture is quite unique. Rather than having open areas for routing channels, as in the traditional approach, the routing channels actually run over the utilized cells. Furthermore, local routing for macrocells does not compete with global routing for the required routing resources, thus allowing greater ease in routing.

I/O Buffers

Output Portion:

The output portion of the I/O buffer contains pre-drive logic, as well as programmable output drive. The output buffers have been designed to source or sink 2, 4, 8, or 12 mA.

Input Portion:

Each input location may be programmed as TTL, CMOS, or Schmitt Trigger.

General:

The I/O incorporates a dual power bus structure which may be used to isolate the output buffer power supply from that of the array core, thus achieving high noise immunity. Any I/O location may also be programmed as Power or Ground. All I/Os are protected against latch-up and static discharge. In addition, pull-up and pull-down resistors are available for use in combination with each I/O. Typical performance features are shown in the AC Characteristics table.

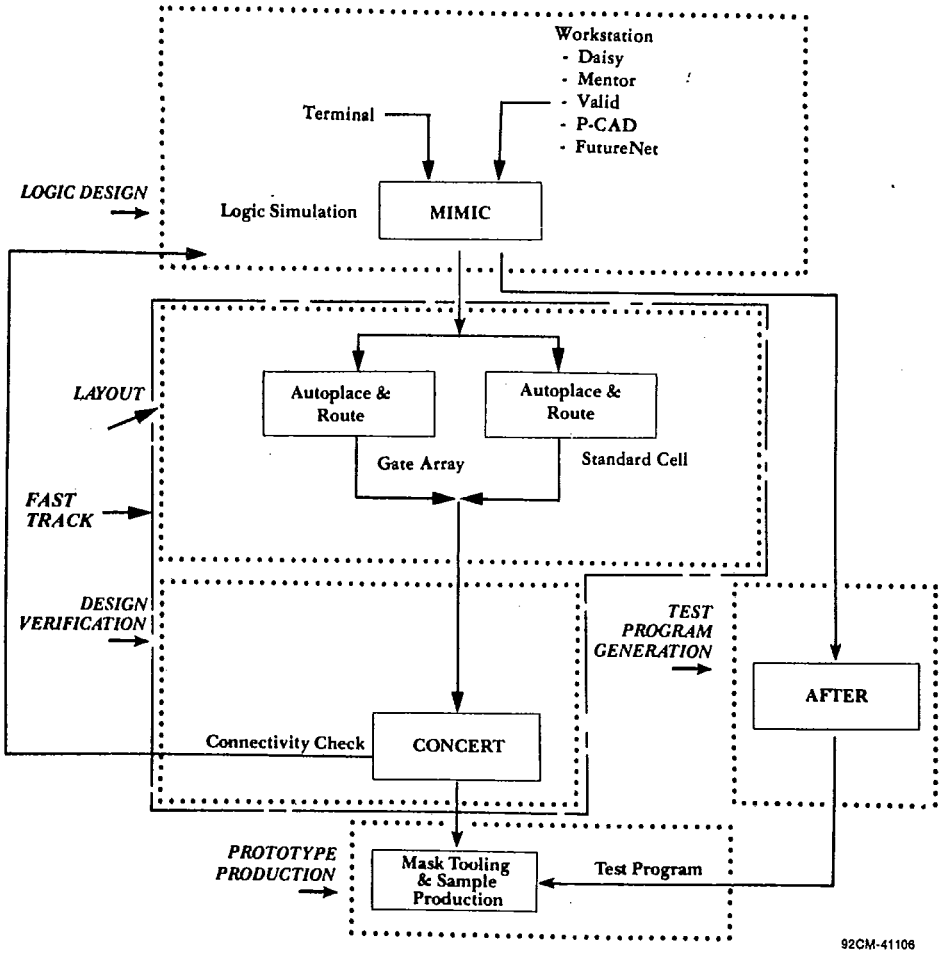
Workstations

GE/RCA gate-array designs may be developed on workstations supported by GE/RCA. Designers using such workstations are provided with a macro library containing the symbols, simulation models and software for design verification, timing calculations and netlist generation. The design is transferred to a GE/RCA design center where placement and routing are performed. The final interconnect capacitances are annotated back to the workstation for verification of circuit performance.

ASIC Design Flow

GE/RCA's CGA100 Series is supported by a complete set of design automation tools. The design flow and the highlights of the design tools that are utilized with the standard-cell library are as follows:

- **MIMIC, GE/RCA's Software Simulation Program**—A powerful software simulation program allows designers of ASIC circuits to model the logical operation of the circuits before device fabrication. Through the program, designers can discover logical flaws; race, hazard, or spike conditions; and timing uncertainties.
- **AFTER (Automatic Functional Test Encoding Routine)**—AFTER aids the designer in generating functional test patterns required for the testing of digital ICs on Automatic Test Equipment (Fairchild, Teradyne, etc.). Test Vectors are generated from the MIMIC logic simulation program.
- **CONCERT (Connectivity Certification)**—CONCERT is a layout analysis program which aids the verification of the logical and electrical correctiveness of the mask artwork produced by the APAR automatic layout program.



Fast Track uses the logic descriptions of MIMIC to implement the layout and control the connectivity verification and mask-generation routines.

Fig. 4 - ASIC design flow.