VITELIC

V61C33
HIGH PERFORMANCE LOW POWER 2K x 8 BIT CMOS DUAL PORT MEMORY

OBJECTIVE SPECIFICATIONS

Features

- 2K x 8 bit CMOS static RAM with 3-state outputs
- Dual-port with on-chip arbitration logic
- High speed
  - 90 ns access time both ports (max.) (No-Busy-Signal operation at max. access rate both ports)
  - 45 ns TURBOMODE access time either port alone (max.)
- Low-power operation
  - operating 325 mW (typ.)
  - standby 15 μW (typ.)
- VICMOS III process virtually eliminates alpha particle induced soft errors.
- Both ports fully asynchronous
- TURBOMODE operation for 45 ns access by either port
- Single 5 V power supply
- TTL compatible

Description

The Vitelic V61C33 is a CMOS 2Kx8 high-speed dual port static RAM with advanced arbitration logic to give either "no-busy-signal" or TURBOMODE operation. Fabrication with the VICMOS III technology provides a high-performance, low-power alternative to NMOS memory.

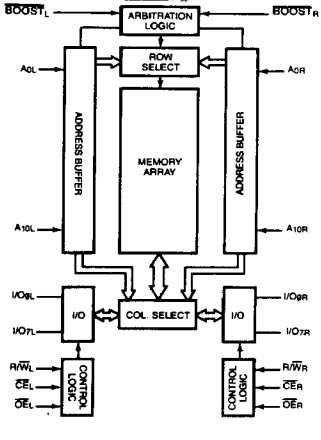
The Vitelic V61C33 provides two parallel 8-bit ports with separate controls, addresses and I/O permitting read or write access to any memory location. Automatic power-down circuitry permits a port to be placed into the standby mode when $\overline{CE}$ is high.

"No-busy" operation where no $\overline{BUSY}$ condition is necessary even at maximum access rates is standard. The normal $\overline{BUSY}$ flags which are asserted by other dual-port memory devices when both ports request service are eliminated. Replacing $\overline{BUSY}$ are two $\overline{BOOST}$ signals which may be used to activate TURBOMODE operation where either port can access memory at 45 ns access time while "locking out" the other port.

The Vitelic V61C33 offers a battery backup data retention mode where the circuit typically consumes only 2.5 μW from a 2 V battery.

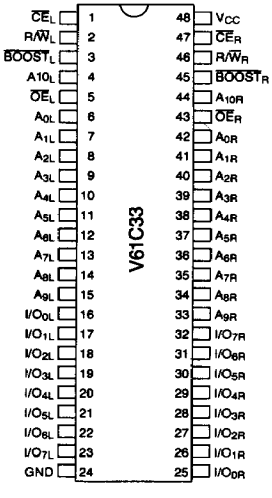
The Vitelic V61C33 is packaged in a 48-pin dual-in-line package (DIP). Mounting hole centers are 600 mils (15.24 mm). A surface mount package is also available.

BLOCK DIAGRAM



PIN CONFIGURATION

(Top View)



PIN NAMES

LEFT PORT	RIGHT PORT	FUNCTION
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
$R/\overline{W}_L$	$R/\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BOOST}_L$	$\overline{BOOST}_R$	ENABLE TURBOMODE
A_{0L}–A_{10L}	A_{0R}–A_{10R}	ADDRESS
I/O_{0L}–I/O_{7L}	I/O_{0R}–I/O_{7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND