VITELIC

V61C62 FAMILY
HIGH PERFORMANCE LOW POWER
16K x 4 BIT
CMOS STATIC RAM

Features

- High Speed
  - Maximum access time of 45/55/70 ns
  - Equal Access and Cycle Times
- Low Power
  - 20 μW typical standby
  - 275 mW typical operating
- Capable of Battery Backup Operation at 2.0 volts min.
- Single +5V Supply and High Density 22 Pin 300 mil DIP
- Completely Static Memory
  - No Clock or Timing Strobe Required
- TTL Compatible

Description

The V61C62 is a high speed, low power, 16,384-word by 4-bit CMOS static RAM fabricated using high-performance MIX-MOS process technology. This high reliability process coupled with innovative circuit design techniques, yields access times of 45 ns maximum.

When the chip select is high, the device assumes a standby mode in which the device power dissipation is reduced to 20 μW (typically). The V61C62 has a data retention mode that guarantees that data will remain valid at a minimum power supply voltage of 2.0 volts.

Device Usage Chart

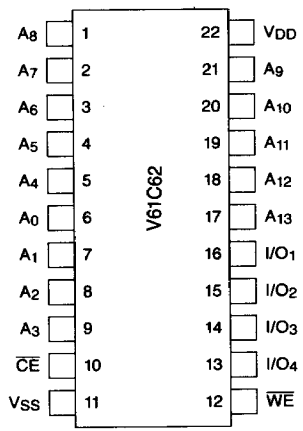
Operating Temperature Range	Package Outline	Access Time (ns)			Power		Temperature Mark
	P	45	55	70	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	Blank
–40°C to +85°C	•	•	•	•	•	•	I

Package	Std.	Pin Count
Plastic DIP	P	22

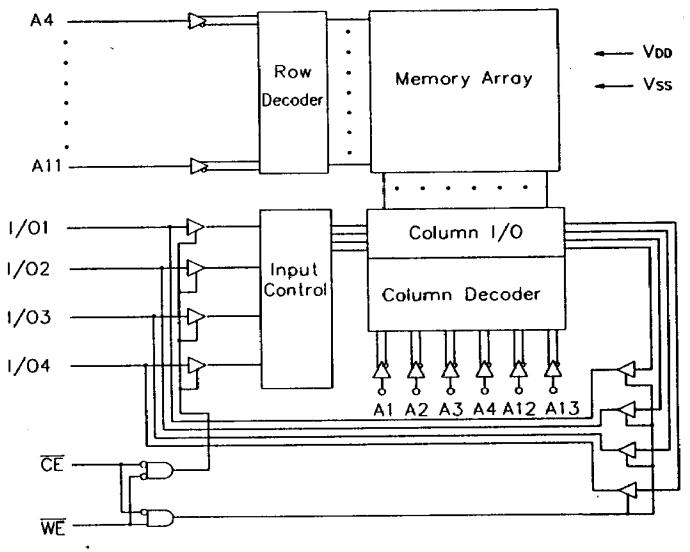
V__C___ — Family, Device, Package, Speed, Power, Temp

DIP PIN CONFIGURATION

Top View



BLOCK DIAGRAM



Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Unit
V_T	Terminal Voltage with Respect to V_{SS}	−0.5* to +7.0	V
P_T	Power Dissipation	1.0	W
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	−55 to +150	°C

*Pulse Width 20 ns, −3.5V

NOTE:
1. Operation at or near absolute maximum ratings can affect device reliability.

Recommended DC Operating Conditions Over The Operating Temperature Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}		0.0	0.0	0.0	V
V_{IH}	Input Voltage	2.2	—	V_{DD} + 0.3	V
V_{IL}		−0.3*	—	+0.8	V

*Pulse Width 20 ns, −0.3V

AC Test Loads

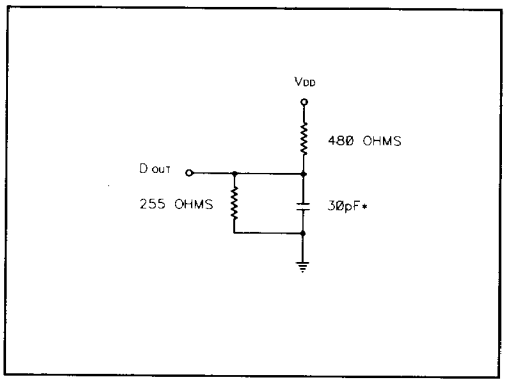


Fig. 1

*Including scope and jig

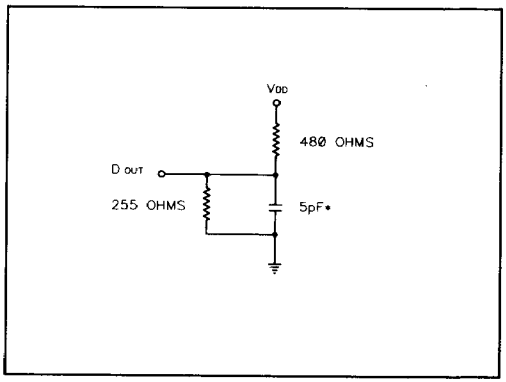


Fig. 2

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	V_{DD} Current	I/O Pin	Operation
Not Selected	H	X	Standby	High-Z	
Read	L	H	Operating	D_{OUT}	Read Cycle
Write	L	L	Operating	D_{IN}	Write Cycle

Capacitance

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	—	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	10	pF

NOTE:
This parameter is sampled and not 100% tested.

DC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = 5.5V, V_{IN} = V_{SS} to V_{DD}		0	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = V_{SS} to V_{DD}		0	—	2	µA
I_{DD}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, Output Open		—	55	80	mA
I_{SB}	Standby Power Supply Current	$\overline{CE}$ = V_{IH}		—	15	25	mA
I_{SB1}		$\overline{CE}$ ≥ V_{DD} – 0.2V V_{IN} ≤ +0.2V or V_{IN} ≥ V_{DD} –0.2V	V61C62	—	30	2000	µA
			V61C62✲✲✲L	—	4	100	
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA		2.4	—	—	V
I_{DD1}	Average Operating Current	Duty Cycle = 100%, Output Open		—	80	120	mA

NOTE:
Typical values are at V_{DD} = 5.0V, T_A = 25°C and specified loading.

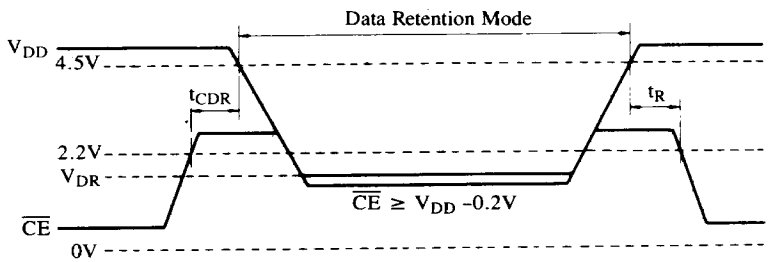
Low V_{DD} Data Retention Characteristics

T_A = 0°C to 70°C

Symbol	Parameter	Test Condition	45, 55, 70			45L, 55L, 70L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{DR}	V_{DD} for Data Retention	$\overline{CE}$ ≥ V_{DD} – 0.2V V_{IN} ≤ +0.2V or V_{IN} ≥ V_{DD} –0.2V V_{DD} = 3.0V	2.0	—	5.5	2.0	—	5.5	V
I_{DDDR}	Data Retention Current		—	18	1100	—	2.0	50	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	0	—	—	ns
t_R	Operation Recovery Time		t_{RC}*	—	—	t_{RC}*	—	—	ns

*t_{RC} = Read Cycle Time

Low V_{DD} Data Retention Waveform



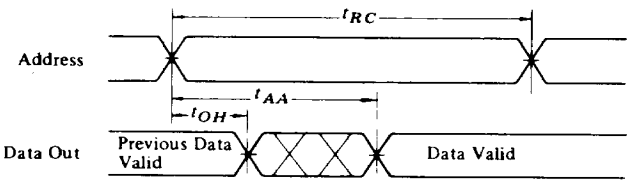
AC Characteristics

At recommended operating conditions, unless otherwise noted.

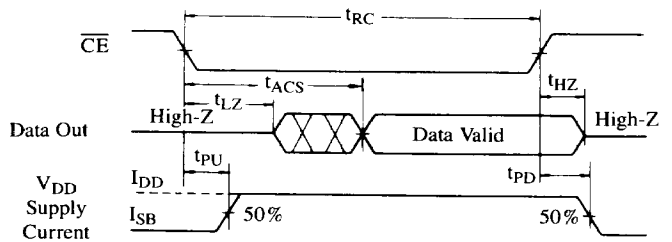
Read Cycle

Symbol	Parameter	45, 45L		55, 55L		70, 70L		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns	1
t_{AA}	Address Access Time	—	45	—	55	—	70	ns	
t_{ACS}	Chip Select Access Time	—	45	—	55	—	70	ns	
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns	
t_{LZ}	Chip Selection to Output in Low-Z	20	—	20	—	20	—	ns	2, 3, 7
t_{HZ}	Chip Selection to Output in High-Z	0	20	0	20	0	20	ns	2, 3, 7
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	ns	
t_{PD}	Chip Deselection to Power Down Time	—	30	—	30	—	30	ns	

Timing Waveform of Read Cycle 1 (4, 5)



Timing Waveform of Read Cycle 2 (4, 6)



NOTES:

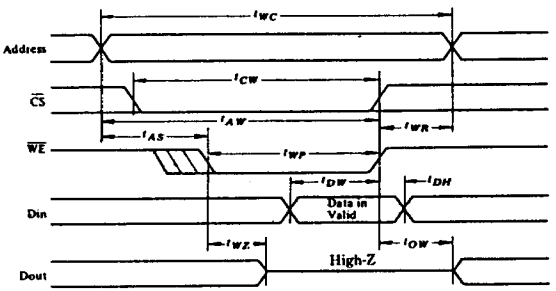
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for read cycle.
5. Device is continuously selected, $\overline{CE}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
7. This parameter is sampled and not 100% tested.

AC Characteristics (Cont'd.)

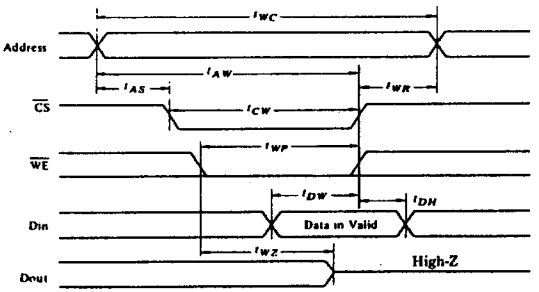
Write Cycle

Symbol	Parameter	45, 45L		55, 55L		70, 70L		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns	
t_{CW}	Chip Selection to End of Write	35	—	45	—	55	—	ns	
t_{AW}	Address Valid to End of Write	35	—	45	—	55	—	ns	
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns	
t_{WP}	Write Pulse Width	35	—	45	—	55	—	ns	1
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns	2
t_{DW}	Data Valid to End of Write	20	—	25	—	30	—	ns	
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns	5
t_{WZ}	Write Enable to Output in High-Z	0	15	0	15	0	15	ns	3, 4, 6, 7
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	ns	5, 6, 7

Timing Waveform of Write Cycle 1 ($\overline{WE}$ Controlled)



Timing Waveform of Write Cycle 2 ($\overline{CE}$ Controlled)



NOTES:

1. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$, (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer buffers remain in a high impedance state.
5. If $\overline{CE}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied.
6. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
7. This parameter is sampled and not 100% tested.

Package Outline

22 Pin Plastic

Item	Inches	Millimeters
A	1.202 max.	30.531 max.
B	.11 max.	2.75 max.
C	.100	2.54
D	.020	.5
E	1.00	25.4
F	.040/.065	1.016/1.651
G	.125/.150	3.175/3.810
H	.005/.050	.127/1.27
J	.130/.180	3.302/4.572
K	.300 typ.	7.62 typ.
L	.24/.27	6.3/6.7
M	.009/.012	.229/.305