V61C64
HIGH PERFORMANCE LOW POWER 8K x 8 BIT CMOS STATIC RAM

PRELIMINARY

Features

- Fast Access Time . . . .V61C64P45/45L 45ns (max)
  . . . .V61C64P55/55L 55ns (max)
  . . . .V61C64P70/70L 70ns (max)
- Low Power
  - Standby 20μW (typ)
  - Operating 220mW (typ)
- Capable of Battery Back-up Operation at 2.0 volts min.
- Output Enable and two Chip Enable inputs for easy application
- Single +5V Supply and 28 pin 600 mil Package
- Completely Static Memory
  - No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible . . .All Inputs and Outputs
- Pin Compatible with standard 64K Static RAMS and EPROMS in 28 pin DIP.

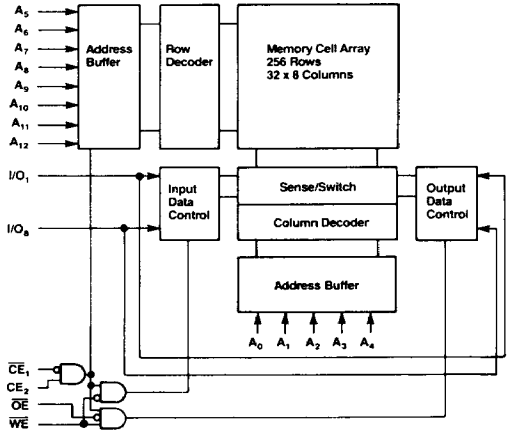
Description

The V61C64 is a high speed, low power, 8,192-word by 8-bit static CMOS RAM fabricated using high-performance MIX-MOS process technology. This high reliability process coupled with innovative circuit design techniques, yields access times of 45 ns. maximum.

When the chip select is brought high, the device assumes a standby mode in which the device power dissipation is reduced to 20 μW (typically). The V61C64 has a data retention mode that guarantees data will remain valid at a minimum power supply voltage of 2.0 volts.

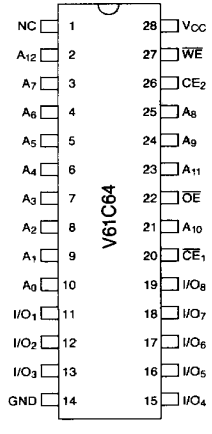
Part Number	Access Time (ns, max)	Active (mA, max)	Standby (μA, max)	Data Retention (μA, max)
V61C64P45	45	120	2000	1100
V61C64P55	55	120	2000	1100
V61C64P70	70	120	2000	1100
V61C64P45L	45	120	100	50
V61C64P55L	55	120	100	50
V61C64P70L	70	120	100	50

FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT

(Top View)



Absolute Maximum Ratings (1)

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	−0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*Pulse Width 20ns, −3.5V

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

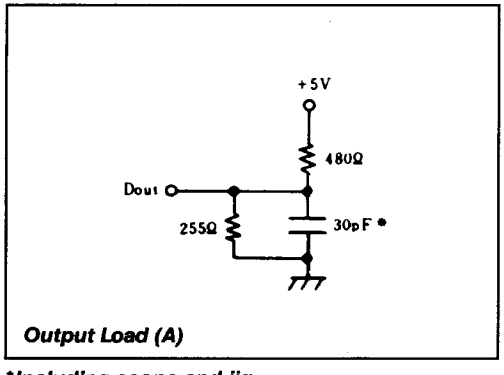
Recommended DC Operating Conditions

(T_a = 0 to +70°C)

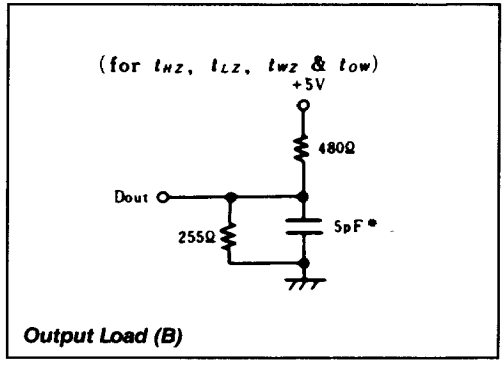
Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	−0.5*	—	0.8	V

*Pulse Width 20ns, −3.5V

AC Test Loads



Output Load (A)



Output Load (B)

*Including scope and jig

Capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Typ.	Max.	Unit	Conditions
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	—	10	pF	V_{OUT} = 0V

NOTE:
This parameter is sampled and not 100% tested.

Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	X	X	Not selected	High-Z	Standby
X	L	X	X	Not selected	High-Z	Standby
L	H	H	H	D_{OUT} disable	High-Z	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

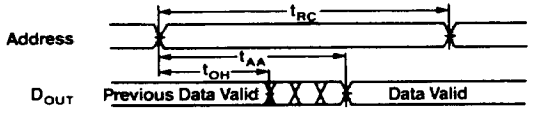
AC Characteristics

(Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading per Load A, T_a = 0°C to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

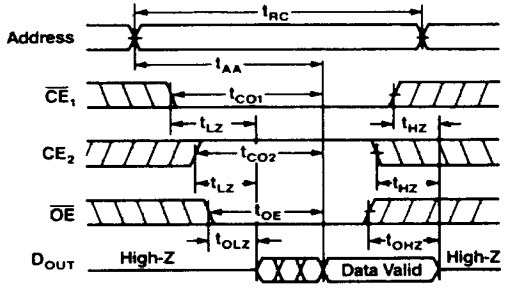
Read Cycle

Item	Symbol	V61C64P45 V61C64P45L		V61C64P55 V61C64P55L		V61C64P70 V61C64P70L		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	45	—	55	—	70	—	ns	
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	
Chip Enable Access Time ($\overline{CE}_1$)	t_{CO1}	—	45	—	55	—	70	ns	
Chip Enable Access Time (CE_2)	t_{CO2}	—	45	—	55	—	70	ns	
Output Enable to Output Valid	t_{OE}	—	30	—	40	—	50	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Enable to Output in Low Z ($\overline{CE}_1$, CE_2)	t_{LZ}	5	—	5	—	5	—	ns	5,6
Output Enable to Output in Low Z ($\overline{OE}$)	t_{OLZ}	0	—	0	—	5	—	ns	
Chip Deselection to Output in High Z ($\overline{CE}_1$, CE_2)	t_{HZ}	—	25	—	30	—	35	ns	5,6
Chip Disable to Output in High Z ($\overline{OE}$)	t_{OHZ}	—	25	—	30	—	35	ns	

Read Cycle No. 1 (Address Access) (1,2)



Read Cycle No. 2 (Chip Enable Access) (1,3,4)



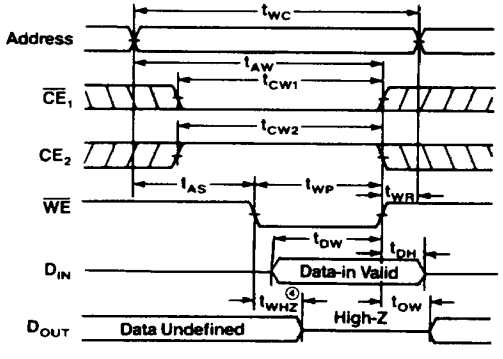
NOTES:

1. $\overline{WE}$ is high for read cycles.
2. Device is continuously selected, $\overline{CE}_1$ = $\overline{OE}$ = V_{IL}; CE_2 = V_{IH}.
3. Addresses valid prior to or coincident with CE_1 transition low; CE_2 transition high.
4. t_{OH} limits valid data, regardless of $\overline{CE}$, $\overline{OE}$.
5. Transition is measured ± 500mV from steady state voltage with specified loading in Load B.
6. This parameter is sampled and not 100% tested.

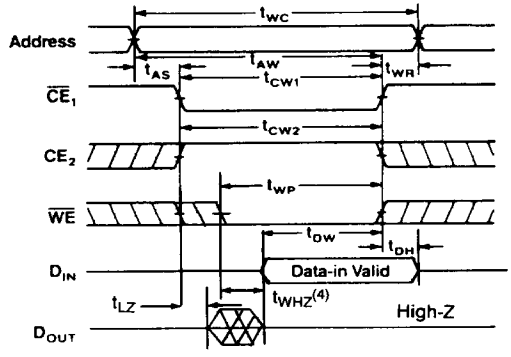
Write Cycle

Item	Symbol	V61C64P45 V61C64P45L		V61C64P55 V61C64P55L		V61C64P70 V61C64P70L		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	45	—	55	—	70	—	ns	
Address Valid to End of Write	t_{AW}	40	—	50	—	65	—	ns	
Chip Enable to End of Write	t_{CW}	40	—	50	—	65	—	ns	
Data to Write Time Overlap	t_{DW}	20	—	25	—	30	—	ns	
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Recovery Time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns	
Write Recovery Time ($\overline{CE}_1$, CE_2)	t_{WR_1}	5	—	5	—	5	—	ns	
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	ns	(5,6)
Write to Output in High Z	t_{WHZ}	—	15	—	20	—	25	ns	(5,6)

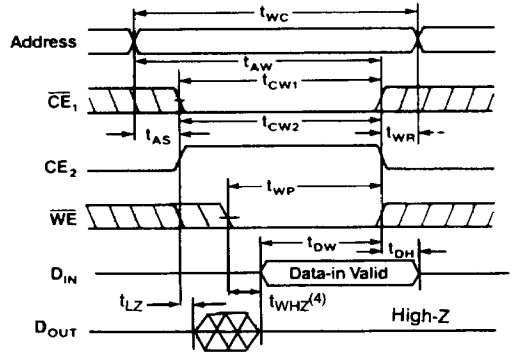
Write Cycle No. 1 ($\overline{WE}$ Controlled) (1,2,3)



Write Cycle No. 2 ($\overline{CE}_1$ Controlled) (1,2)



Write Cycle No. 3 (CE_2 Controlled) (1,2)



NOTES:

1. A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
2. $\overline{CE}_1$ or $\overline{WE}$ (or CE_2 must be high (low) during address transition.
3. If $\overline{OE}$ is high, I/O pins remain in a high impedance state.
4. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.
5. Transition is measured ± 500mV from steady state voltage with specified loading in Load B.
6. This parameter is sampled and not 100% tested.

DC and Operating Characteristics

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Parameter	V61C64P45 V61C64P55 V61C64P70			V61C64P45L V61C64P55L V61C64P70L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{in} = GND to V_{CC}	-2	—	2	-2	—	2	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	-2	—	2	-2	—	2	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	—	55	80	—	55	80	mA
Average Operating Current	I_{CC2}	cycle = min., duty = 100%, I_{OUT} = 0mA	—	80	120	—	80	120	mA
Standby Current	I_{SB1}	CE_2 < 0.2V or $\overline{CE}_1$ ≥ V_{CC} - 0.2V and CE_2 ≥ V_{CC} - 0.2V	—	30	2000	—	2	100	μA
	I_{SB2}	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL}	—	15	25	—	15	25	mA
Output High Voltage	V_{OH}	I_{OUT} = -4.0 mA	2.4	—	—	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OUT} = 8.0 mA	—	—	0.4	—	—	0.4	V

Low V_{CC} Data Retention Characteristics

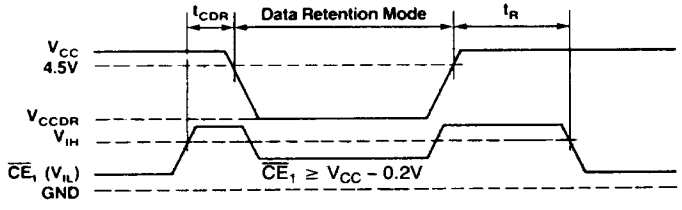
(T_a = 0°C to 70°C)

Parameter	Symbol	Test Condition	V61C64			V61C64-L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC} for Data Retention	V_{CCDR}		2.0	—	5.5	2.0	—	5.5	V
Data Retention Current	I_{CCDR}	$\overline{CE}_2 \le -0.2V$ or $CE_1 \ge V_{CC}-0.2$ and $CE_2 \ge V_{CC}-0.2$ V_{IN} = 0V to V_{CC}, V_{CC} = 3V	—	18	1100	—	2	50	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*	—	—	t_{RC}*	—	—	ns

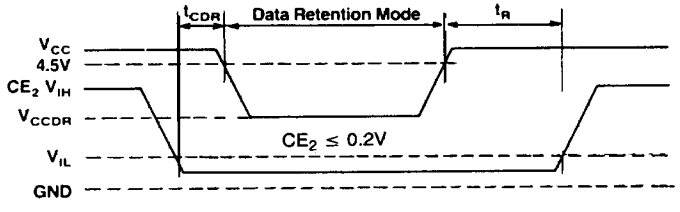
*t_{RC} = Read Cycle Time

Data Retention Timing Waveforms

$\overline{CE}_1$ Controlled (1)



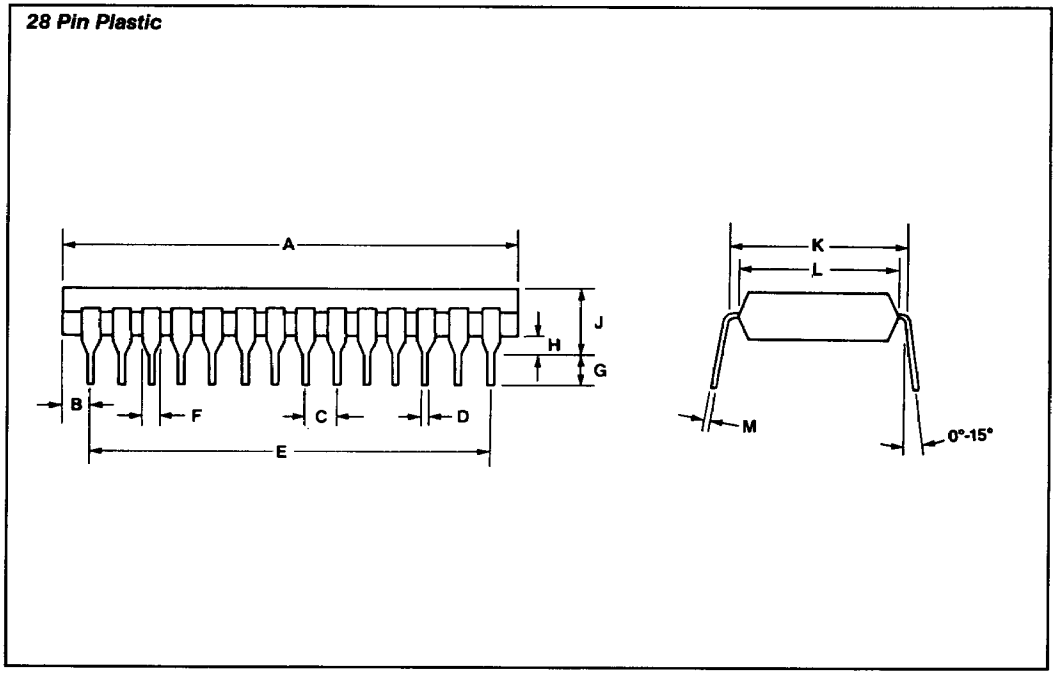
CE_2 Controlled (2)



NOTES:
1. CE_2 must be equal to or higher than V_{CC} – 0.2V. The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.
2. The inputs (Addresses, $\overline{CE}_1$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance state.

Package Outline

28 Pin Plastic



Item	Millimeters	Inches
A	38.2 max.	1.50 max.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.2 ± 0.15	0.05 ± .005
G	3.0 min.	0.12 min.
H	0.5 min.	0.02 min.
J	5.5 max.	0.22 max.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$