National Semiconductor

PRELIMINARY
August 1994

CGS701V
Commercial Low Skew PLL 1 to 8 CMOS Clock Driver
CGS701TV
Industrial Low Skew PLL 1 to 8 CMOS Clock Driver

General Description

CGS701 is an off the shelf clock driver specifically designed for today's high speed designs. It provides low skew outputs which are produced at different frequencies from three fixed input references. The XTALIN input pin is designed to be driven from a 25 MHz–40 MHz crystal oscillator.

The PLL, using a charge pump and an internal loop filter, multiplies this input frequency to create a maximum output frequency of four times the input.

The device includes a TRI-STATE® control pin to disable the outputs. This feature allows for low frequency functional testing and debugging.

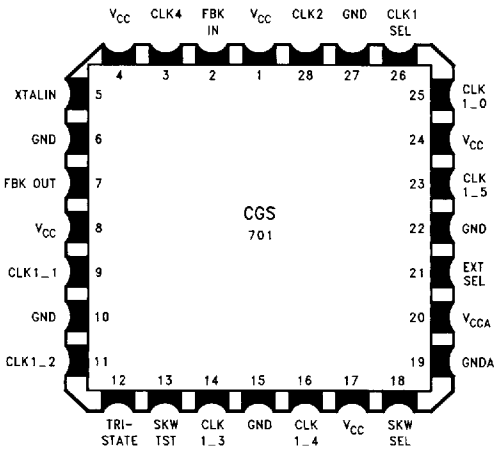
Also included, is an EXTSEL pin to allow testing the chip via an external source. The EXTSEL pin, once set to high, causes the External-Clock_MUX to change its input from the output of the VCO and Counter to the external clock signal provided via SKWTST input pin. (continued)

Features

- Guaranteed:
  400 ps pin-to-pin skew (t_{OSHL} and t_{OSLH}) on 1X outputs.
- Pentium™ and PowerPC™ compatible
- ±500 ps propagation delay
- Output buffer of eight drivers for large fanout
- 25 MHz–160 MHz output frequency range
- Outputs operating at 4X, 2X, 1X of the reference frequency for multifrequency bus applications
- Selectable output frequency
- Internal loop filter to reduce noise and jitter
- Separate analog and digital V_{CC} and ground pins
- Low frequency test mode by disabling the PLL
- Implemented on National's Core CMOS process
- Symmetric output current drive: +30/−30 mA I_{OL}/I_{OH}
- Industrial temperature of −40°C to +85°C
- 28-pin PCC for optimum skew performance
- Guaranteed 2k volts ESD protection

Connection Diagram

Pin Assignment for PLCC



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See NS Package Number V28A

Pin Description

PLCC Package

Pin	Name	Description
1	V_{CC}	Digital V_{CC}
2	FBK IN	Feedback Input Pin
3	CLK4	4X Clock Output
4	V_{CC}	Digital V_{CC}
5	XTALIN	Crystal Oscillator Input
6	GND	Digital Ground
7	FBK OUT	Feedback Output Pin
8	V_{CC}	Digital V_{CC}
9	CLK1_1	1X Clock Output
10	GND	Digital Ground
11	CLK1_2	1X Clock Output
12	TRI-STATE	Output TRI-STATE Control
13	SKWTST	Skew Testing Pin
14	CLK1_3	1X Clock Output
15	GND	Digital Ground
16	CLK1_4	1X Clock Output
17	V_{CC}	Digital V_{CC}
18	SKWSEL	Skew Test Selector Pin
19	GNDA	Analog Ground
20	V_{CCA}	Analog V_{CC}
21	EXTSEL	External Clock MUX Selector
22	GND	Digital Ground
23	CLK1_5	1X Clock Output
24	V_{CC}	Digital V_{CC}
25	CLK1_0	1X Clock Output
26	CLK1SEL	CLK1 Multiplier Selector
27	GND	Digital Ground
28	CLK2	2X Clock Output

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CGS701V Commercial Low Skew PLL 1 to 8 CMOS Clock Driver
CGS701TV Industrial Low Skew PLL 1 to 8 CMOS Clock Driver

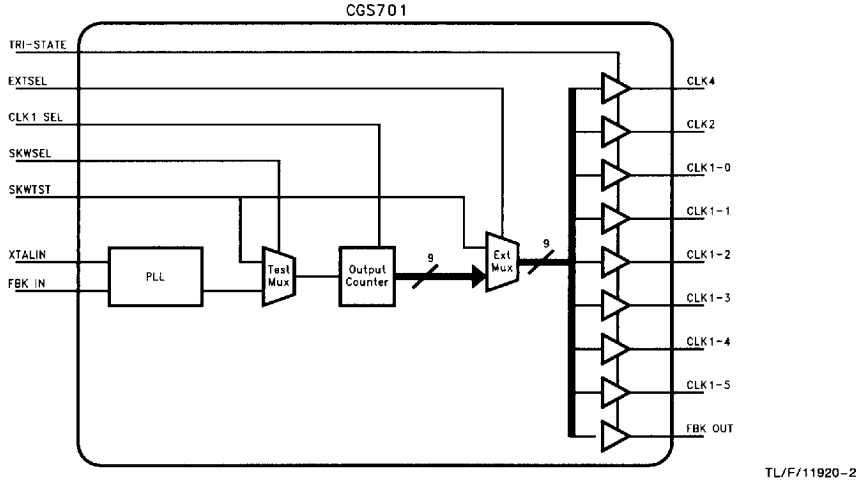
General Description (Continued)

CLK1SEL pin changes the output frequency of the CLK1__0 thru CLK1__5 outputs. During normal operation, when CLK1SEL pin is high, these outputs are at the same frequency as the input crystal oscillator, while CLK2 and CLK4 outputs are at twice and four times the input frequency respectively.

Once CLK1SEL pin is set to a low logic level, the CLK1 outputs will be at twice the input frequency, the same as the CLK2 output, with CLK4 output still being at four times the input frequency.

In addition, another pin is added for increasing the test capability. SKWSEL pin allows testing of the counter's output and skew of the output drivers by bypassing the VCO. In this test mode CLK4 frequency is the same as SKWTST input frequency, while CLK2 is 1/2 and CLK1 frequencies are 1/4 respectively (refer to the Truth Table). In addition CLK1SEL functionality is also true under this test condition.

Block Diagram



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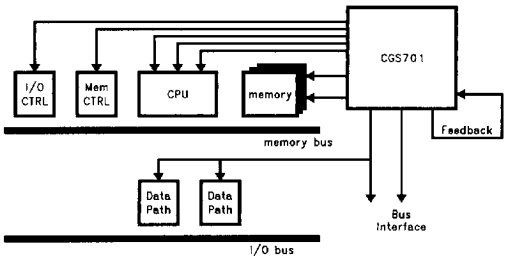
Truth Table

Input						Output		
CLK1 SEL	EXT SEL	EXT CLK	SKW SEL	SKW TST	TRI-STATE	CLK4	CLK2	CLK1
*H	L	X	L	X	H	4 x f in	2 x f in	f in
*L	L	X	L	X	H	4 x f in	2 x f in	2 x f in
X	H	⎍	X	X	H	⎍	⎍	⎍
H	L	X	H	⎍	H	1 x f tst	½ x f tst	¼ x f tst
L	L	X	H	⎍	H	1 x f tst	½ x f tst	½ x f tst
X	X	X	X	X	L	Z	Z	Z

*Steady state phase, frequency lock

Typical Application



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Absolute Maximum Ratings (Note A)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage Diode Current (I_{IK})	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_O)	
$V = -0.5V$	−20 mA
$V = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±60 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±60 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Static and Dynamic) (Note B)	1400 mW

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Input Crystal Frequency	25 MHz–40 MHz
Operating Temperature (T_A)	0°C to +70°C
External Clock Frequency (EXTCLK Pin)	1 MHz–10 MHz
Input Rise and Fall Times (0.8V to 2.0V)	
Crystal Input	5 ns max
All Other Inputs	10 ns max

Typical Theta JA	LFM	C/W
	0	54
	225	45
	500	38
	900	34

Note A: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Note B: Power dissipation is calculated using 49°C/W as the thermal coefficient for the PCC package at 225 LFM airflow. The input frequency is assumed at 33 MHz with CLK4 at 132 MHz and CLK2 and CLK1 being at 66 MHz. In addition, the ambient temperature is assumed 70°C.

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V_{CC} = 4.5V–5.5V, T = 0°C to 70°C			Units	Conditions
		Min	Typ	Max		
V_{IH}	Minimum Input High Level Voltage	2.0			V	
V_{IL}	Maximum Input Low Level Voltage			0.8	V	
V_{OH}	Minimum Output High Level Voltage	V_{CC} − 0.1			V	I_{OUT} = −50 μA
		V_{CC} − 0.6				I_{OH} = −30 mA
V_{OL}	Maximum Output High Level Voltage			0.1	V	I_{OUT} = −50 μA
				0.6		I_{OL} = 30 mA
I_{OHD}	High Level Output Current	50	110	170	mA	$V_{OH} = V_{CC} - 1.0V$
I_{OLD}	Low Level Output Current	50	110	170	mA	V_{OL} = 1.0V
I_{IN}	Leakage Current	−50		50	μA	V_{IN} = 0.4V or 4.6V
$I_{OZL/H}$	Output Leakage Current					
C_{IN}	Input Capacitance			10.0	pF	
I_{CC}	Quiescent digital + analog Current (No Load)		3.0	5.0	mA	$V_{IN} = V_{CC}$, GND
I_{CCT}	I_{CC} per TTL Input			2.5		$V_{IN} = V_{CC} - 2.1$, GND

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter				V_{CC} = 4.5V–5.5V F_{IN} = 25 to 40 MHz T = 0°C to +70°C C_L = Circuit 1 R_L = Circuit 1			Units	Notes
					Min	Typ	Max		
t_{rise}	Output Rise	CLK4 CLK2 CLK1	0.8V to 2.6V 1.0V to V_{CC} − 1.0V 1.0V to V_{CC} − 1.0V				1.5	ns	(Note 1)
		All	0.8V to 2.0V				1.5		
t_{fall}	Output Fall	CLK4 CLK2 CLK1	2.6V to 0.8V V_{CC} − 1.0V to 1.0V V_{CC} − 1.0V to 1.0V				1.5	ns	(Note 1)
		All	0.8V to 2.0V				1.5		
t_{SKEW}	Maximum Edge-to-Edge Output Skew		+ to + Edges + to + Edges + to + Edges	CLK1__CLK1 CLK1__CLK4 CLK2__CLK4		100 300 300	400 500 500	ps	(Note 2)
t_{LOCK}	Time to Lock the Output to the Synch Input						1.0	ms	
t_{CYCLE}	Output Duty Cycle			CLK1 Outputs CLK2 Output CLK4 Output	49 49 35		51 51 65	%	(Note 3)
Jitter	Output Jitter						0.3	ns	(Note 4)
t_{PD}	Propogation Delay from XTALIN to FBKOUT				−0.3		+0.3	ns	(Notes 2, 4, 5, 6)

Note 1: t_{rise} and t_{fall} parameters are measured at the pin of the device.

Note 2: Skew is measured at 50% of V_{CC} for CLK1 and CLK2 while it is being measured at 1.4V for CLK4. Limits are guaranteed by design.

Note 3: Output duty cycle is measured at $V_{DD}/2$ for CLK1 and CLK2 while it is being measured at 1.4V for CLK4. Limits are guaranteed by design.

Note 4: Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge over 1000 cycles. It is also measured at output levels of $V_{CC}/2$. Refer to *Figure 2* for further explanation.

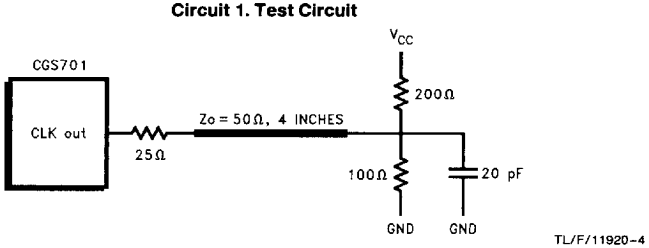
Note 5: Measured from the ref. input to any output pin. The length of the feedback and XTALIN traces will impact this delay time.

Note 6: This parameter includes pin-to-pin skew, longterm jitter over 1000 cycles, part-to-part variation as well as propagation delay thru the device.

Note 7: The GNDA pins of the 701 must be as free of noise as possible for minimum jitter. Separate analog ground plane is recommended for the PCB. Also the V_{CCA} pin requires extra filtering to further reduce noise. Ferrite beads for filtering and bypass capacitors are suggested for the V_{CCA} pin.

Note 8: All parameters are being measured at the device pin.

Circuit 1. Test Circuit



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AC Electrical Characteristics (Continued)

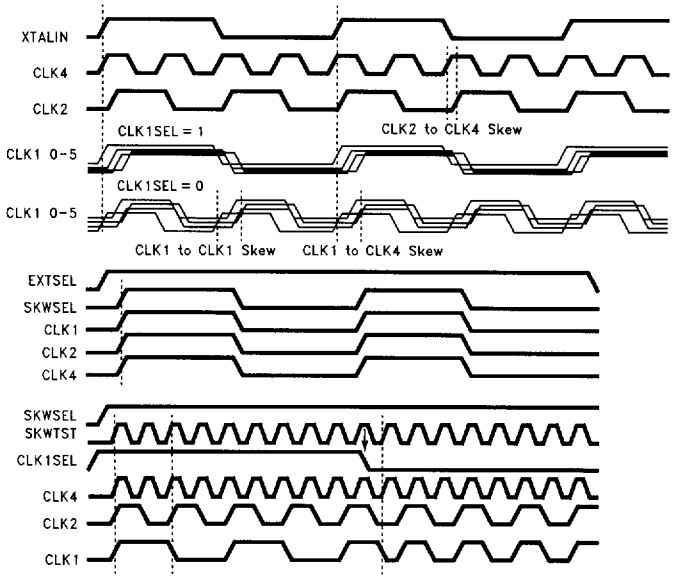

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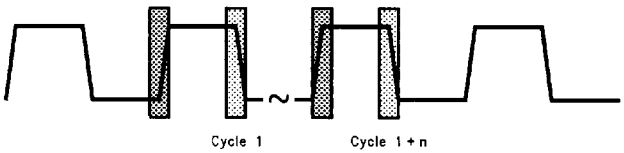
FIGURE 1. Waveforms



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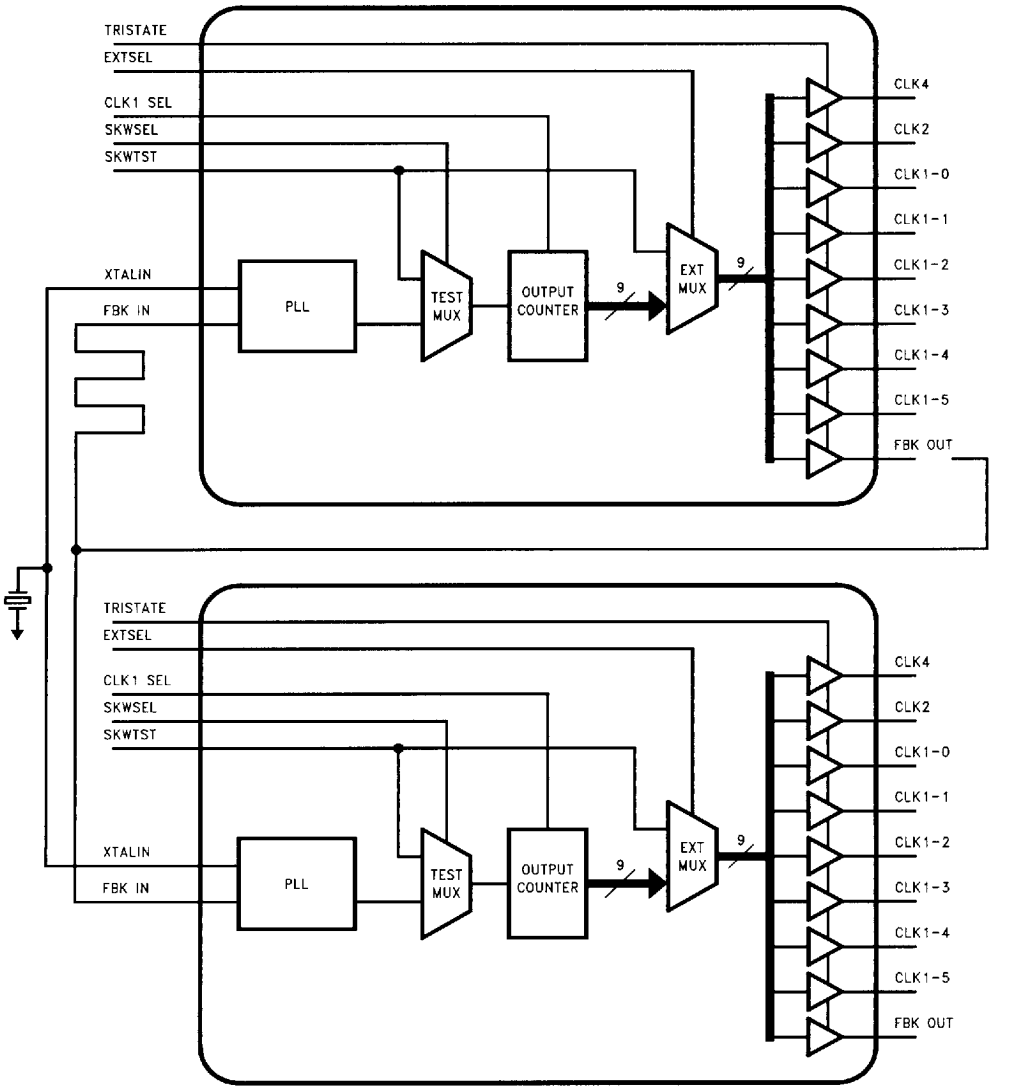
P(n) − P(n+1) = 300 ps for either the rising or falling edge.

FIGURE 2. Jitter

Application Example: Cascading CGS701



TL/F/11920–7

High Speed Clock Sources and Their Effect on Electromagnetic Compatibility

System clocks of 100 MHz and above are becoming not uncommon in today's desktop personal systems. These higher speed personal computers will generate more unwanted noise due to their faster frequencies and edge rates.

This noise can be in many forms, but the most common one is EMI. EMI, ElectroMagnetic Interference can be defined as a form of noise pollution. This noise occurs when changes in electric fields which are created by the transitioning voltage signals combine with the magnetic field changes which are created by the changing current directions. This Electromagnetic field can either be conducted via the printed circuit traces or even at the same time radiated through the board material and space to the outside world.

EMI is of interest to everyone. For this reason many governments and their agencies have issued specifications requiring compliance by all the electro, electro-mechanical and electronic equipment and their manufacturers. These specifications are to ensure that certain techniques are applied so that the products can interoperate in a common environment such that no degradation of performance would exist due to internally or externally conducted or radiated EM emissions. This is defined as the Electromagnetic Compatibility or simply the EMC.

National's *Clock Generation and Support* product family consists of clock drivers and generators which are designed to operate above 50 MHz. At such speeds, the use of these products requires many design consideration for noise reduction.

Below is a brief tutorial aimed at such purpose. In order to minimize and contain possible electromagnetic radiation one must first understand its causes and sources.

THE SOURCE, VICTIM AND THE COUPLING PATH THEORY:

This theory simply states that within each system there exists a source (typically a high frequency component) that generates the noise, and then there is a victim or receptor of the same high frequency signal or noise *(Figure 3)*.

The coupling path can take two forms. If there is an actual connection between the source and the receptor this coupling path causes the interference to take a conductive form. A typical example would be ribbons, cables and traces. If the source and the receptor are separated by space and no physical connections exist between the two, then the interference takes the form of radiation.

In practice most systems have both forms of interference, conducted and radiated, and they co-exist at the same time.

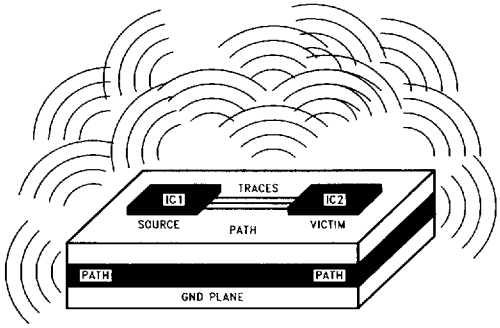


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FIGURE 3. Source, Path and Receptor

This theory can also be looked at differently. EMI sources, paths and victims can be further separated into three categories within each system:

1. Power Plane/loop for all or individual components.

This consists of the power supply (receptor), power/ground planes and traces (paths) and components (sources). This loop can take the form of conducted interference since there exists an actual connection between the power pins of every component and the power supply via either power planes or power traces *(Figure 4)*.

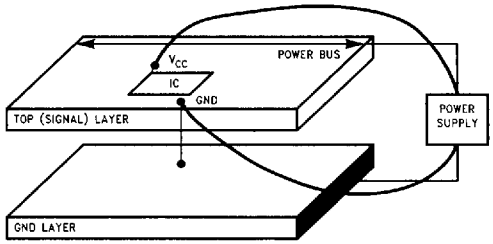

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FIGURE 4. Power Distribution Loop

2. Signal paths.

These paths are typically signal traces or cables that are carrying high frequency signals thoughout the board, either from point to point or in a bus fashion. The sources in this case are the drivers or their outputs, while the victims are the receivers or other components inputs. The path includes the termination network as well as signal traces.

High Speed Clock Sources and Their Effect on Electromagnetic Compatibility (Continued)

The EMI that is associated with these paths are both conducted and radiated. Conducted since there are actual connections between the sources and the receptors, while there will be radiation as well since there exists a decoupling path thru different layers and their mutual inductances to the power planes as well as outside of the enclosure.

Minimizing the coupled inductance between these paths helps to minimize the overall radiated noise from the system. The coupled loop area between the adjacent traces and characteristic impedance of the interconnect lines also play an important role in the overall level of the created noise.

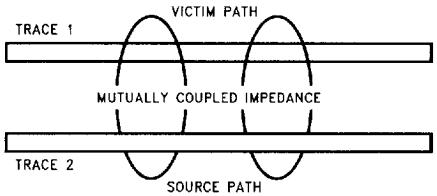

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FIGURE 5. Signal Path

3. Package radiation.

This form of EMI can be caused within the high speed components which are radiating outside as well as within the system's enclosure itself. This form can be classified as radiated EMI.

In this case the sources or the emitters are internal to the components. This radiation is caused by electromagnetic wave propagation through space or material. This is the most important (least desired) form of EMI since it not only involves other equipments, but also is the most difficult one to contain.

Below are some recommendations that can help to minimize the electomagnetic interference. These suggestions are common practices during the device and board level system design. There are also some suggestions for decoupling the power planes and shielding the system.

DEVICE LEVEL RECOMMENDATIONS:

These recommendations need to be implemented during the chip level design. The primary task at this point is to design the components in a way that not only they meet the system's timing requirements, but also they produce the least amount of radiated and decoupled noise as well.

Figure 6 reflects a time domain translation of a trapezoidal signal to its frequency domain. In order to reduce any emissions both the amplitude and slopes of this signal must be minimized.

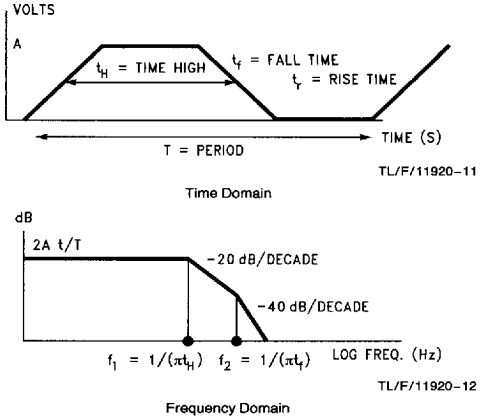

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FIGURE 6. Time to Frequency Domain

As it is shown the frequency component of any signal can be represented by the amplitude, period, rise and fall time of the same signal in real time. Reducing the amplitude (i.e. from 5V to 3V signal swing) can reduce the total power associated with the signal, while slowing the edge rates helps to decrease the rate (slope) at which the energy is dissipated.

Here are some suggestions in order to accomplish such:

- Rounded-off edges contain less high frequency components
- Minimizing output voltage swing reduces noise. Low Voltage technologies such as TTL, LVDS and 3.3V supply will help to lower emissions.
- The edge rate must be as slow as they can be allowed without violating overall system timing.

BOARD LAYOUT RECOMMENDATIONS:

As the frequencies increase the parasitic effects of the printed circuit boards become more visible. Some common practice for minimizing such effects are listed below. Employing these guidelines can help to reduce the overall EMI levels. *Figure 7* represents some of these suggestions.

- Multi-layer Printed Circuit board should be used.
- Wire-wraps should be avoided since they can act as antennas.
- Power and ground PLANES must be used instead of traces when possible.
- The effective distance between these planes should be as small as possible to increase the bulk decoupling capacitance.
- No sockets!
- Multi-via pads for power and ground pad connections can help to reduce the effective impedance.
- Trace lengths should be as short as possible.

High Speed Clock Sources and Their Effect on Electromagnetic Compatibility (Continued)

- If Analog sections exist, use of Islands for both the power and ground busses are preferred for Isolation techniques.
- High frequency signal traces must be sandwiched between ground traces or planes for minimizing cross talk.
- Avoid using sharp corners/bends on traces carrying high frequency signals.

POWER DISTRIBUTION DECOUPLING RECOMMENDATIONS:

One of the most susceptible victims of EMI is the power supply. This path (loop) includes the power supply, planes (V_{CC} and Ground) as well as the device power pins. Minimizing the size of this loop helps to reduce EMI since it helps to contain the noise in a smaller area.

- Bypass caps must be used, sometimes in multiples and should be as close as possible to the device V_{CC} pin and the ground plane.
- Bypassing must be done for ALL power pins.
- Multiple value bypass capacitors must be used in order to filter out the right analog V_{CC} will help to filter some high frequency noise components.
- Electrolytic capacitors are more preferred for decoupling.

SYSTEM LEVEL/GENERAL RECOMMENDATIONS:

And finally some suggestions to be observed throughout the whole system design. These suggestions, no matter how large the amount of noise, will help to contain the interferences within the system.

- Twisted pairs of Coax (rigid, semi-rigid or flexable) cable must be used for lines that can not be placed on the printed circuit board.
- All I/O cables must be shielded and tied to chassis ground with a low impedance connection.
- All the enclosure's opening must be minimized in number and size.
- Number of outputs that need to be switching simultaneously must be kept at minimum for reduced X-talk.
- Terminations must be used for minimizing reflections.

Summary and Conclusion:

In order to meet the Electromagnetic standards, many design guidelines and practices must be followed. These practices if done properly will help to minimize the level of the noise that is generated by the system.

In addition, it is preferred to spend the time and money prior to production commitment compared to a costly last minute fix to become EMI compliant.

References

1. Cocovich, Joe, EMI/RFI Board Design. National Semiconductor Application Note 643. Dec. 1989.
2. Gerke, Darryl & Kimmel, William. Designer's Guide to Electromagnetic compatibility. EDN Supplement Jan 20, 1994.

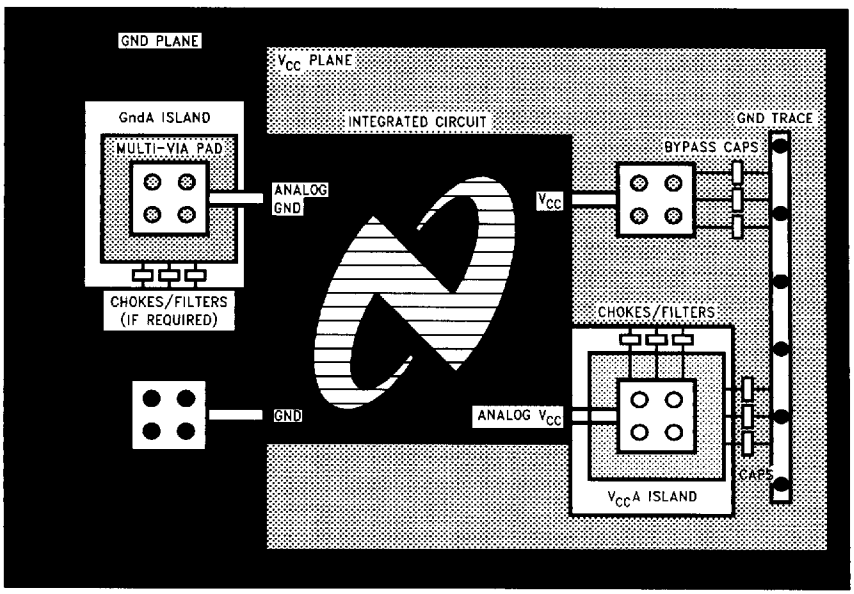

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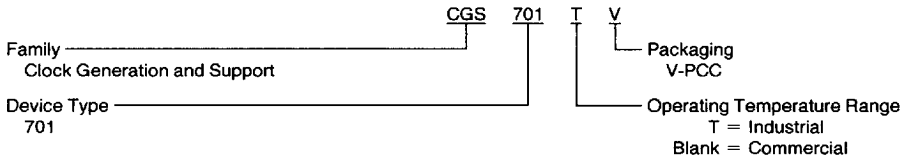
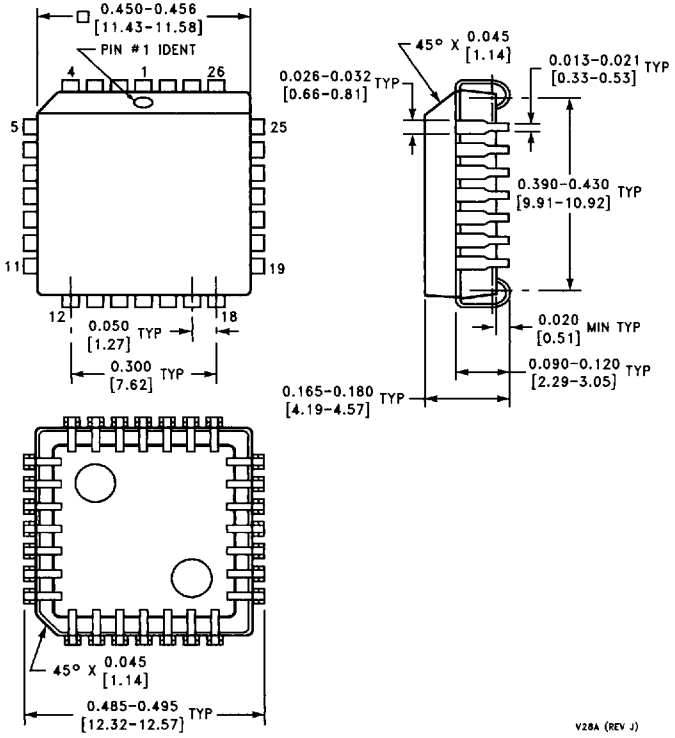
FIGURE 7. Suggested Printed Circuit Layout

Ordering Information (Contact NSC Marketing for Specific Date of Availability)



Lit # 101812-002

Physical Dimensions inches (millimeters)



28-Lead Molded Plastic Leaded Chip Carrier
Order Number CGS701V or CGS701TV
NS Package Number V28A

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