64MB- 8Mx72 SDRAM W/ PLL, REGISTER AND SPD

FEATURES

- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3 volt ± 0.3v Power Supply
- 168- Pin DIMM JEDEC

DESCRIPTION

The WED3DG728V is a 8Mx72 synchronous DRAM module which consists of nine 8Meg x 8 SDRAM components in TSOP-11 package, two 18- bit Drive ICs for input control signal and one 2K EEPROM in an 8- pin TSSOP package for Serial Presence Detect which are mounted on a 168 Pin DIMM multilayer FR4 Substrate.

* *This datasheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	$\overline{CS0}$	58	DQ19	86	DQ32	114	*$\overline{CS1}$	142	DQ51
3	DQ1	31	DNU	59	VDD	87	DQ33	115	$\overline{RAS}$	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DNU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{CS2}$	73	VDD	101	DQ45	129	*$\overline{CS3}$	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DNU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

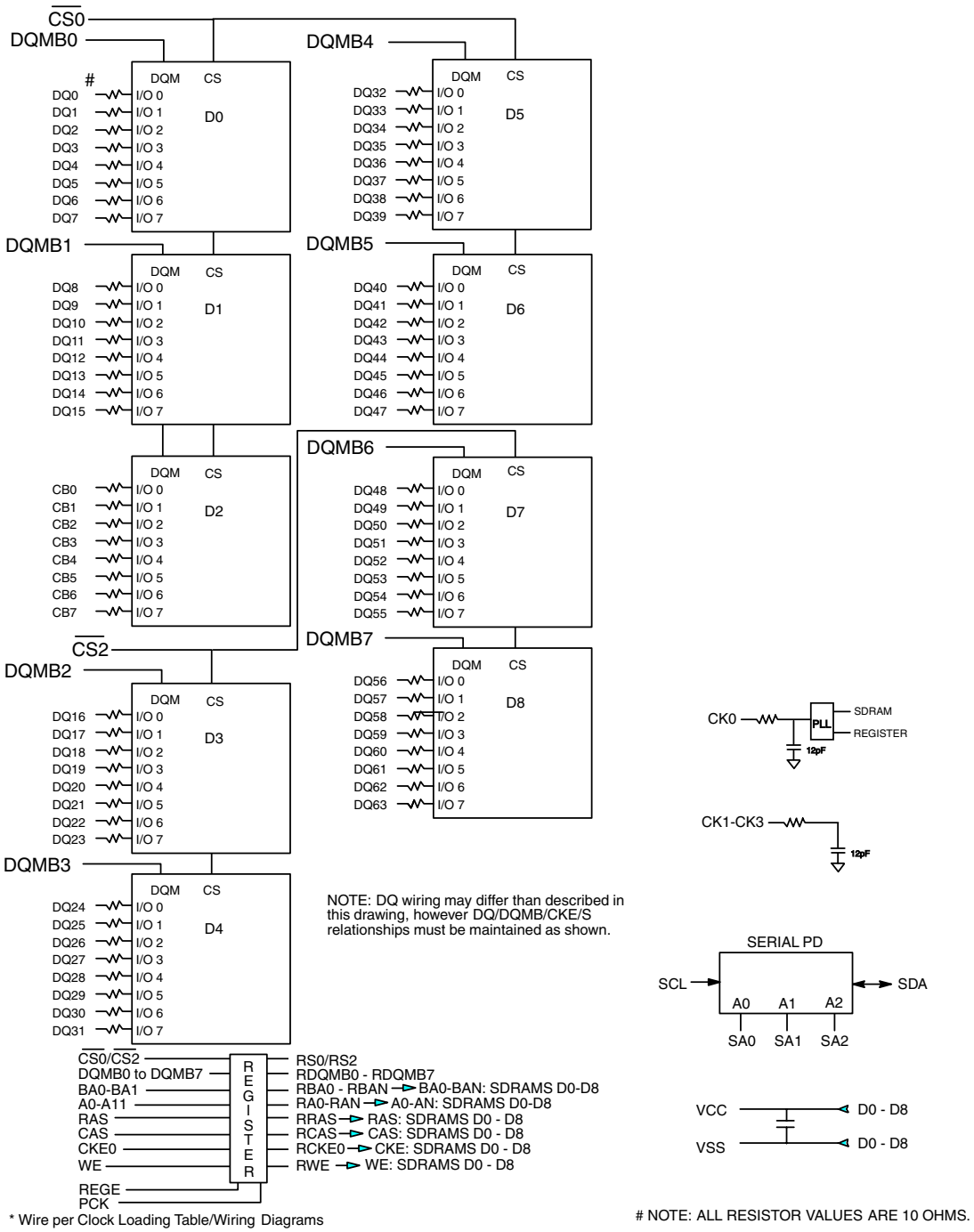
PIN NAMES

A0 – A11	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CB0-7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock Enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0-7	DQM
VDD	Power Supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0-2	Address in EEPROM
DNU	Do not use
NC	No Connect

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



NOTE: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

* Wire per Clock Loading Table/Wiring Diagrams

NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to VSS	V_{IN}, Vout	-1.0 ~ 4.6	V
Voltage on VDD supply relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Storage Temperature	TSTG	-55 ~ +150	°C
Power Dissipation	PD	9	W
Short Circuit Current	IOS	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage Referenced to: V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input High Voltage	VIH	2.0	3.0	VDDQ+0.3	V	1
Input Low Voltage	VIL	-0.3	—	0.8	V	2
Output High Voltage	VOH	2.4	—	—	V	IOH= -2mA
Output Low Voltage	VOL	—	—	0.4	V	IOL= -2mA
Input Leakage Current	ILI	-10	—	10	µA	3

Note: 1. VIH (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. VIL (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(T_A = 23°C, f = 1MHz, V_{DD} = 3.3V, VREF=1.4V ± 200mV)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12)	CIN1	-	15	pF
Input Capacitance ($\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	CIN2	-	15	pF
Input Capacitance (CKE0)	CIN3	-	15	pF
Input Capacitance (CLK0)	CIN4	-	23	pF
Input Capacitance ($\overline{CS0}$,$\overline{CS2}$)	CIN5	-	15	pF
Input Capacitance (DQM0-DQM7)	CIN6	-	15	pF
Input Capacitance (BA0-BA1)	CIN7	-	15	pF
Data input/output capacitance (DQ0-DQ63)	Cout	-	16	pF
Data input/output capacitance (CB0-CB7)	Cout1	-	16	pF

OPERATING CURRENT CHARACTERISTICS

(V_{CC} = 3.3V, T_A = 0°C to +70°C)

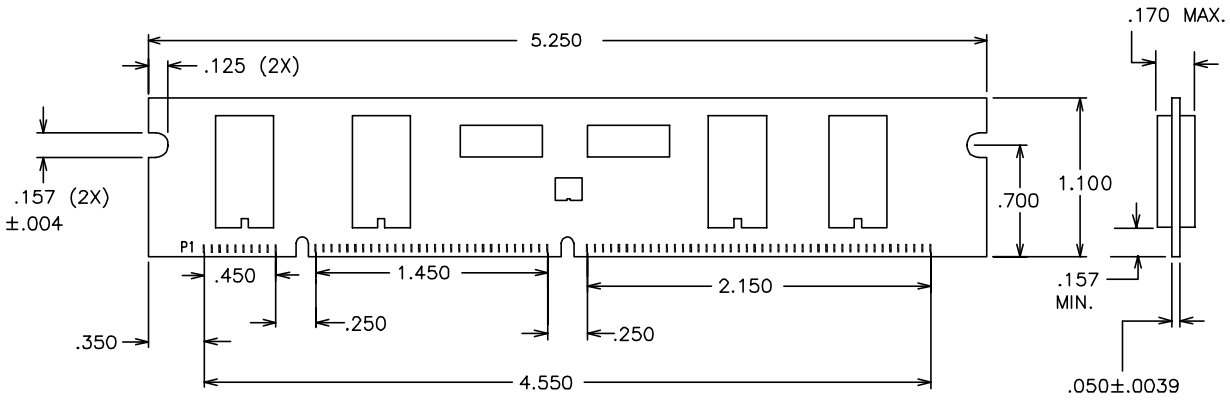
Parameter	Symbol	Conditions	Version 133	Version 100	Units	Note
Operating Current (One bank active)	ICC1	Burst Length = 1 tRC ≥ tRC(min) IOL = 0mA	1,175	1,060	mA	1
Precharge Standby Current in Power Down Mode	ICC2P	CKE ≤ VIL(max), tCC = 10ns	360		mA	3
	ICC2PS	CKE & CLK ≤ VIL(max), tCC = ∞	15			
Precharge Standby Current in Non-Power Down Mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are charged one time during 20	485			
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	60		mA	3
Active standby current in power-down mode	ICC3P	CKE ≥ VIL(max), tCC = 10ns	380		mA	3
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	30			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	575		mA	3
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ input signals are stable	140		mA	3
Operating current (Burst mode)	ICC4	Io = mA Page burst 4 Banks activated tCCD = 2CLK	1,535	1,350	mA	1
Refresh current	ICC5	tRC ≥ tRC(min)	1,715	1,520	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	360		mA	3

Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 2 Drive ICs.

ORDERING INFORMATION

Part Number	Speed	CAS Latency
WED3DG728V10D2	100MHz	CL=2
WED3DG728V7D2	133MHz	CL=2
WED3DG728V75D2	133MHz	CL=3

PACKAGE DIMENSIONS



ALL DIMENSIONS ARE IN INCHES

REV.	DATE	REQUESTED BY	DETAILS
A	10-25-01	PAUL MARIEN	HISTORY PAGE
B	1-15-02	PAUL MARIEN	-CHANGE BLOCK DIAGRAM -CHANGE MODULE HEIGHT TO 1.100"
0	9-19-02	PAUL MARIEN	-CHANGED FROM ADVANCED TO FINAL