HEADLINE

FEATURES:

- 8M x 32 and 2 x 8m x 32 Densities
- Based on Intel's Strataflash (J3) family of Flash Devices
  - E28F640J3
- (64) 128Kb Erase Blocks (Symetrical)
- High Performance Interface Async Page Mode Reads
  - 120/25 ns Read Access Time
- 2.7V -3.6V Vcc Operation
- 128 bit Protection Register;
  - 64 bit Unique Device Identifier
  - 64 bit User Programmable OTP Cells
- Common Flash Interface (CFI)
- Scaleable Command Set (SCS)
- 32 byte Write Buffer, 64M Total Erase Cycles
  - 100,000 Erase Cycles per Block
- Package
  - 80 pin SIMM

CAPACITANCE

		8M x32	2 x 8M x 32	
Parameter	**Sym**	**Max**	**Max**	**Unit**
Address Lines	CA	35	70	pF
Data lines	CDQ	15	30	pF
Chip & Write Enable Lines	CG	15	30	pF
Output Enable Lines	CG	35	70	pF

DESCRIPTION:

The WED7F328XDNSN and WED7F2328XDNSN are organized as one and two banks of 8M x 32 respectively. The modules are based on Intel's E28F640J3, 8M x 8 / 4M x 16 device family. Both modules offer access times of 120-150ns.

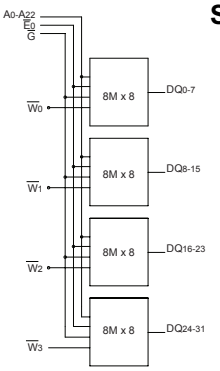
PIN CONFIGURATIONS

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	V_{SS}	21	NC	41	A_{11}	61	DQ_9
2	V_{CC}	22	NC	42	A_{10}	62	DQ_8
3	NC	23	*	43	A_9	63	DQ_7
4	$\overline{G}$	24	*	44	A_8	64	DQ_6
5	$\overline{W}_0$	25	V_{SS}	45	A_7	65	DQ_5
6	$\overline{W}_1$	26	DQ_{29}	46	A_6	66	DQ_4
7	NC	27	DQ_{30}	47	A_5	67	DQ_3
8	DQ_{16}	28	DQ_{31}	48	A_4	68	DQ_2
9	DQ_{17}	29	$\overline{W}_2$	49	A_3	69	DQ_1
10	DQ_{18}	30	NC	50	A_2	70	DQ_0
11	DQ_{19}	31	A_{21}	51	A_1	71	NC
12	DQ_{20}	32	A_{20}	52	A_0	72	V_{CC}
13	DQ_{21}	33	A_{19}	53	$\overline{W}_3$	73	PD_1
14	DQ_{22}	34	A_{18}	54	V_{SS}	74	PD_2
15	DQ_{23}	35	A_{17}	55	DQ_{15}	75	PD_3
16	DQ_{24}	36	A_{16}	56	DQ_{14}	76	PD_4
17	DQ_{25}	37	A_{15}	57	DQ_{13}	77	PD_5
18	DQ_{26}	38	A_{14}	58	DQ_{12}	78	PD_6
19	DQ_{27}	39	A_{13}	59	DQ_{11}	79	PD_7
20	DQ_{28}	40	A_{12}	60	DQ_{10}	80	V_{SS}

** SIMM DENSITY*
32MB PIN 24= $\overline{E}_0$ PIN 23= NC
64MB PIN 24= $\overline{E}_0$ PIN 23= $\overline{E}_1$

FIG. 1 BLOCK DIAGRAMS

WED7F328XDNSN: 8M x 32 STRATAFLASH



WED7F2328XDNSN: 2 x 8M x 32 STRATAFLASH

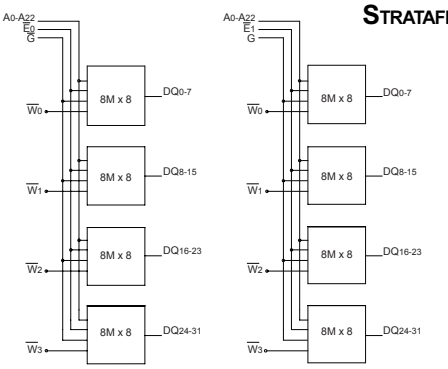
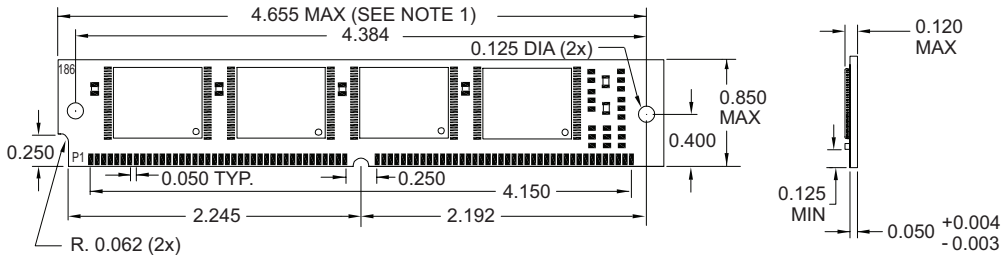
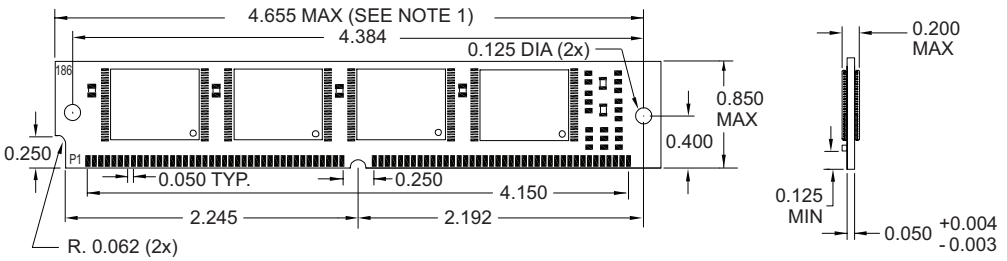


FIG. 2 MECHANICAL PACKAGE



NOTE: THE MAXIMUM DIMENSION TO BE MEASURED WITHOUT INCLUDING THE BREAKAWAY AREA.

FIG. 3 MECHANICAL PACKAGE



NOTE: THE MAXIMUM DIMENSION TO BE MEASURED WITHOUT INCLUDING THE BREAKAWAY AREA.

MODULE SPEED VIA PRESENCE DETECT

Module Speed Identification			
Max Access Time	Presence Select Pin		
	PD5	PD6	PD7
Not Def.	1	1	1
120ns	0	1	0
150ns	1	0	0

ORDERING INFORMATION

Part Number	Speed (ns)	Density
WED7F328XDNSN120C	120	32MB
WED7F328XDNSN150C	150	32MB
WED7F2328XDNSN120C	120	64MB
WED7F2328XDNSN150C	150	64MB