VITELIC

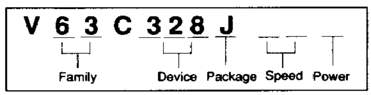
V63C328
HIGH PERFORMANCE, LOW POWER 8K x 16 BIT CACHE CMOS STATIC RAM

Features

- High speed
  - Designed for 80386 Systems up to 33/25/20 MHz
  - Directly interfaces with 82385 Cache Controller
  - Maximum access time of 30/40/45 ns
  - Output Enable access time of 10/12/13 ns
- High Output driveability - 80 pF
- Low Power
  - Full CMOS design offers lowest standby power
  - Internal Automatic Power Down feature provides low operating current
- Supports Direct Mapped and 2-way Set Associative Cache Schemes
- Two $\overline{WE}$ and two $\overline{OE}$ control pins
- Two $\overline{CE}$ pins for byte control
- Multiple power buses for optimum noise reduction
- Fully static operation
- Available in 52 pin PLCC

Description

The V63C328 is a high performance, full CMOS, 8K x 16, 128K bit cache memory. This highly integrated solution is specifically designed to provide direct interface to the 80386 32-bit CPU and the 82385 cache controller. Built-in Mode Control allows the user to configure the memory internally as either one 8K x 16 memory, or two 4K x 16 memories through the use of a programmable MODE pin. Two V63C328 chips may be used in parallel to provide 32K bytes of cache memory for high performance 32-bit personal computers and CAD/CAM engineering workstations that use the Intel 82385 cache controller. The Cache RAM works with 80386 systems running at speeds of 33, 25 and 20 MHz.



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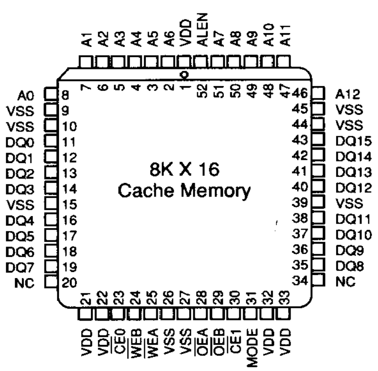
PLCC PIN CONFIGURATION Top View



80386 Speed	*V63C328 Speed*
20 MHz	01
25 MHz	02
33 MHz	03

Package	*Sym*	*Pin Count*
Plastic LCC	J	52

Operating Temperature Range	Package Outline	Access Time (ns)			Power	Temperature Mark
	J	30 (03)	40 (02)	45 (01)	Std.	
0°C to 70°C	•	•	•	•	•	Blank

Functional Block Diagrams

Direct Map Mode (Mode = Low)
8K x 16

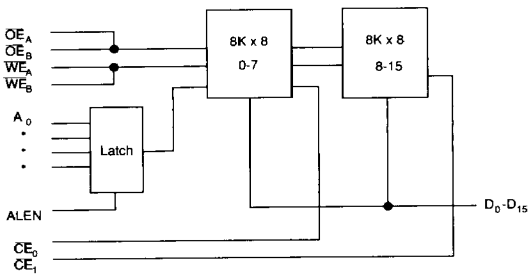


Figure 1.

Two-Way Set-Associative Mode (Mode = High)
4K x 16

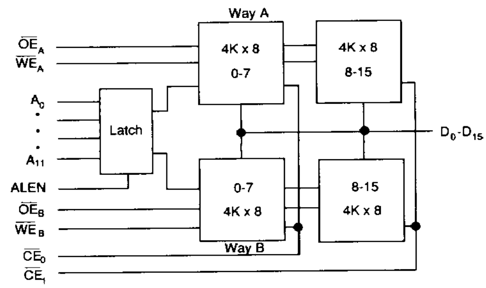


Figure 2.

Functional Description

The 8K x 16 Cache Memory consists of eight 2K x 8 SRAMs (see Fig. 1 and Fig. 2) which can function as:

(1) 8K x 16 direct mapped cache, or
(2) 4K x 16 2-way set associative cache.

The operation of the 8K x 16 cache memory is controlled by the MODE control, $\overline{WE}$ and $\overline{OE}$ as shown in Table 1.

Table 1.

Description	Mode	$\overline{WE}$ (A, B)	$\overline{OE}$ (A, B)
Direct Map	0	tied together as $\overline{WE}_1$	tied together as $\overline{OE}_1$
2-way Set Associative	1	$\overline{WE}$ (A) = $\overline{WE}_1$ $\overline{WE}$ (B) = $\overline{WE}_2$	$\overline{OE}$ (A) = $\overline{OE}_1$ $\overline{OE}$ (B) = $\overline{OE}_2$

The mode control alters the addresses to the internally configured 2K x 8 SRAMs through the on-chip address logic as follows:

MODE = 0, A_0–A_{12} same as chip address inputs
MODE = 1, A_{12} always grounded, others same

Two 8K x 16 cache memories may be used in parallel to provide 32K bytes of cache to the Intel 82385 with double word, word, and byte transfers controlled by Chip Enable $\overline{CE}_0$ and $\overline{CE}_1$ pairs. The V63C328 can be interfaced directly to the 80386/82385 system without external address latches or data tranceivers. It is designed for 80386 systems operating at speeds up to 33 MHz. In a 2-way set associative 32 KB cache configuration, two V63C328 replaces sixteen 4K x 4 SRAMs, two 74F373s, and eight 74F245 devices.

Pin Description

A_0–A_{12}	Addresses
DQ_0–DQ_{15}	Data Inputs/Outputs
ALEN	Address Latch Enable
MODE	Mode
$\overline{CE}_0$, $\overline{CE}_1$	Chip Enables
$\overline{OE}_A$, $\overline{OE}_B$	Output Enables
$\overline{WE}_A$, $\overline{WE}_B$	Write Enables
V_{DD}	+5V Power
V_{SS}	Ground

Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	–0.5* to +7.0	V
V_T	Terminal Voltage with Respect to V_{SS}	–0.5* to V_{DD} +0.5	V
P_D	Power Dissipation 100% Duty Cycle	1.4	W
P_D	Power Dissipation 40% Duty Cycle	0.75	W
t_{OPR}	Operating Temperature	0 to +70	°C
t_{STG}	Storage Temperature	–55 to +125	°C

NOTE: 1. Operation at or near absolute maximum rating can affect device reliability.

*Truth Table**

$\overline{CE}_0$	$\overline{CE}_1$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	Operation
H	H	X	X	X	X	Standby, all outputs High-Z
X	X	H	H	H	H	All outputs High-Z
L	H	L	H	H	H	Read low byte, select Way A
L	H	H	L	H	H	Read low byte, select Way B
L	H	X	X	L	H	Write low byte, select Way A
L	H	X	X	H	L	Write low byte, select Way B
H	L	L	H	H	H	Read high byte, select Way A
H	L	H	L	H	H	Read high byte, select Way B
H	L	X	X	L	H	Write high byte, select Way A
H	L	X	X	H	L	Write high byte, select Way B
L	L	L	H	H	H	Read word, select Way A
L	L	H	L	H	H	Read word, select Way B
L	L	X	X	L	H	Write word, select Way A
L	L	X	X	H	L	Write word, select Way B

* **NOTES:** In direct mapped cache mode, A_{12} is used to control Reads and Writes from Way A and Way B.

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*Capacitance**

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	—	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	8	pF

* **NOTE:** These parameters are sampled and not 100% tested.

Recommended DC and Operating Characteristics (1)

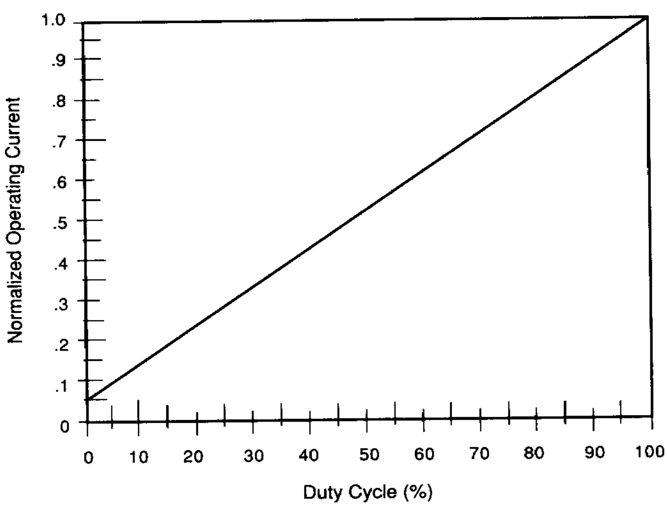
T_A = 0°C to 70°C, V_{DD} = 5.0V ± 5%, V_{SS} = 0V, unless otherwise noted.

Parameter	Symbol	Min.	Max.	Units	Test Condition
Supply Voltage	V_{DD}	4.75	5.25	V	
Supply Voltage	V_{SS}	0.0	0.0	V	
Input High Voltage	V_{IH}	2.2	V_{DD}+.3	V	
Input Low Voltage	V_{IL}	–0.5*	+0.8	V	
Input Leakage Current	I_{LI}	–10	10	µA	V_{DD} = 5.25V, $V_{IN} = V_{SS}$ to V_{DD}
Output Leakage Current	I_{LO}	–10	10	µA	$\overline{CE}_0 = V_{IH}$, $\overline{CE}_1 = V_{IH}$ $V_{OUT} = V_{SS}$ to V_{DD}
Dynamic Operating Current	I_{CC}		275	mA	$\overline{CE}_0 = V_{IL}$, $\overline{CE}_1 = V_{IL}$ Outputs Open 100% Duty Cycle, 60 ns Cycle Time
CMOS Standby Current	I_{SB2}		6	mA	$\overline{CE}_0$ & $\overline{CE}_1 \geq V_{DD}$–0.2V, $V_{IN} \geq V_{DD}$–0.2V or $V_{IN} \leq V_{SS}$+0.2V Active Outputs Open (Note 2)
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = –1.0 mA

* –3.5V for 20 ns pulse.

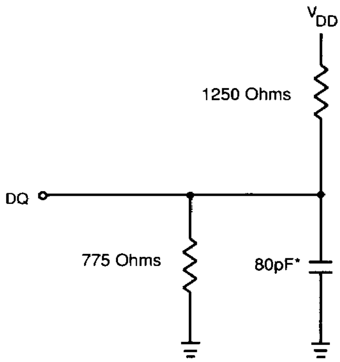
NOTE: 1. Measurement based on AC operating conditions of 25 MHz 82385.
2. All inputs should be in the DC condition.

Normalized Current vs. Duty Cycle



AC Test Loads

Signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0.0V to 3.0V, output loading as shown in the diagrams below.



*Value Includes Scope and Jig Capacitance

Figure 3. Output Load

AC Test Conditions

(Applies to READ and WRITE Cycle Timing)

Input Pulse High Level	V_{IH} = 3.0V
Input Pulse Low Level	V_{IL} = 0.0V
Input Rise Time	t_R = 3 ns
Input Fall Time	t_F = 3 ns
Input and Output Reference Level	1.5V
Output Load	C_L = 80pF, 1 TTL
V_{DD}	5V ± 5%
T_A	0° to +70°C

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AC Characteristics

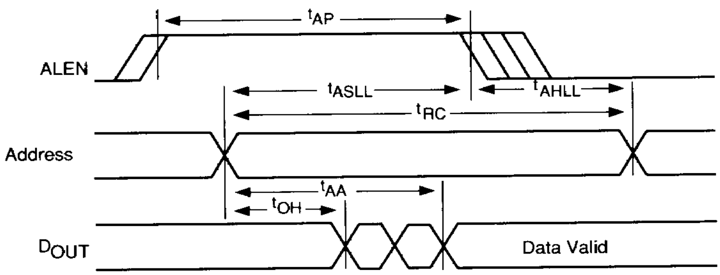
At recommended operating conditions, unless otherwise noted.

Read Cycle (4)

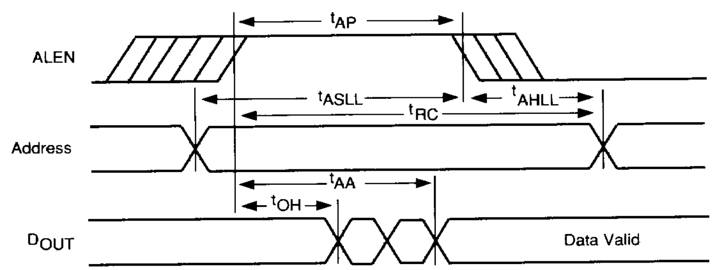
Symbol	Parameter	01		02		03		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	45		40		30		ns	1
t_{AA}	Address Access Time/ ALEN Access Time		45		40		30	ns	
t_{ACS}	Chip Enable Access Time		45		40		30	ns	
t_{OE}	Output Enable to Output Valid		13		12		10	ns	
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Enable to Output in Low-Z	5		5		5		ns	2, 3
t_{OLZ}	Output Enable to Output in Low-Z		0		0		0	ns	2, 3
t_{HZ}	Chip Disable to Output in High-Z		30		25		15	ns	2, 3
t_{OHZ}	Output Disable to Output in High-Z		10		7		7	ns	2, 3
t_{AP}	Address Latch Enable Pulse Width	15		10		8		ns	
t_{ASLL}	Address Setup to Latch Low	8		6		4		ns	
t_{AHLL}	Address Hold after Latch Low	5		5		5		ns	

NOTES:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 500mV from tristate voltage level at the output load (see figure 3).
4. $\overline{WE}$ is High for read cycle.

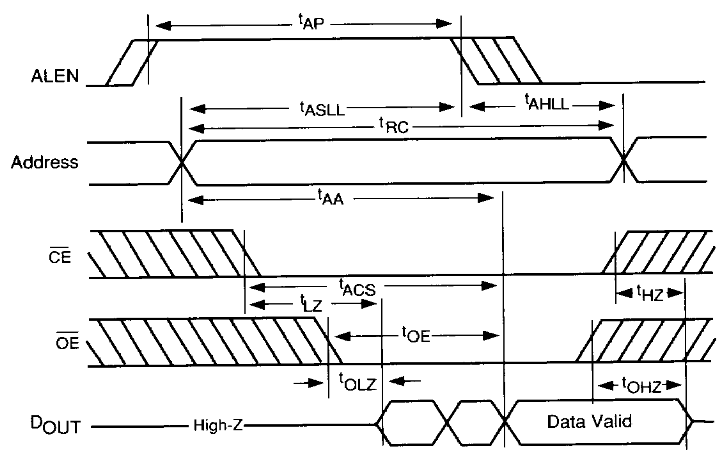
Timing Waveforms of Read Cycle No. 1 (Address Controlled) (4)



Timing Waveforms of Read Cycle No. 2 (ALEN Controlled) (4)



Timing Waveforms of Read Cycle No. 3 (4)



AC Characteristics (continued)
At recommended operating conditions, unless otherwise noted.

Write Cycle (1, 4, 5, 6)

		01		02		03			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Notes**
t_{WC}	Write Cycle Time	45		40		30		ns	
t_{AW}	Address Valid to End of Write	45		35		30		ns	
t_{CW}	Chip Enable to End of Write	30		25		18		ns	
t_{DW}	Data Valid to End of Write	12		12		10		ns	
t_{WP}	Write Pulse Width	20		20		18		ns	
t_{DH}	Data Hold Time	2		2		2		ns	
t_{AS}	Address Setup Time	5		3		2		ns	
t_{WR}	Write Recovery Time ($\overline{WE}$)	2		2		2		ns	
t_{LZ}	Chip Enable to Output in Low-Z	5		5		5		ns	2, 3
t_{AP}	Address Latch Enable Pulse Width	15		10		8		ns	
t_{ASLL}	Address Setup to Latch Low	8		6		4		ns	
t_{AHLL}	Address Hold after Latch Low	5		5		5		ns	
t_{OHZ}	Output Disable to Output in High-Z		10		7		7	ns	2, 3
t_{OLZ}	Output Enable to Output in Low-Z		0		0		0	ns	2, 3

NOTES:
1. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 500mV from low or high voltage with load (see Figure 3).
4. $\overline{CE}$ or $\overline{WE}$ must be high during address transition.
5. If $\overline{OE}$ is high, I/O pins remain in an high impedance state.
6. $\overline{CE}$ must remain static during the Write Cycle, i.e. when $\overline{WE}$ is low. The Write Cycle can only be controlled by the $\overline{WE}$ pulse.

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Timing Waveforms of Write Cycle (1, 4, 5)