VITELIC

V63C329
HIGH PERFORMANCE, LOW POWER 8K x 16 BIT CACHE CMOS STATIC RAM

PRELIMINARY

Features

- Designed for 64KB and 128KB Cache Implementation
- Directly interfaces with 82385 Cache Controller
- High speed
  - Designed for 80386 Systems at 33/25/20 MHz
  - Maximum access time of 30/40/45 ns
  - Output Enable access time of 10/12/13 ns
- Access time in Burst Mode 17/22/25 ns
- High Output driveability - 80 pF
- Low Power
  - Full CMOS design offers lowest standby power
  - Internal Automatic Power Down feature provides low operating current
- Supports 2-way Set Associative Cache Scheme
- $\overline{WE}$ and $\overline{OE}$ control pins
- Two $\overline{CE}$ pins for byte control
- Burst Mode Control supports 64KB and 128KB
- Multiple power buses for noise reduction
- Fully static operation
- Available in 52 pin PLCC

Description

The V63C329 is a high performance, full CMOS, 8K x 16, 128KB cache memory. This highly integrated solution is specifically designed to provide direct interface to the 80386 32-bit CPU and the 82385 Cache Controller. The V63C329 provides compatible signal interfaces and a highly integrated solution for 64K and128K byte cache schemes. With 128K bit memory density and built-in Burst Mode control, four V63C329 chips can be configured in parallel as a 16K X 32 memory to provide 64K bytes of Cache memory. Eight V63C329 chips organized as two banks of 16K x 32 provides 128K bytes of Cache. The Cache RAM works with 80386 systems running at speeds of 33, 25 and 20 MHz.

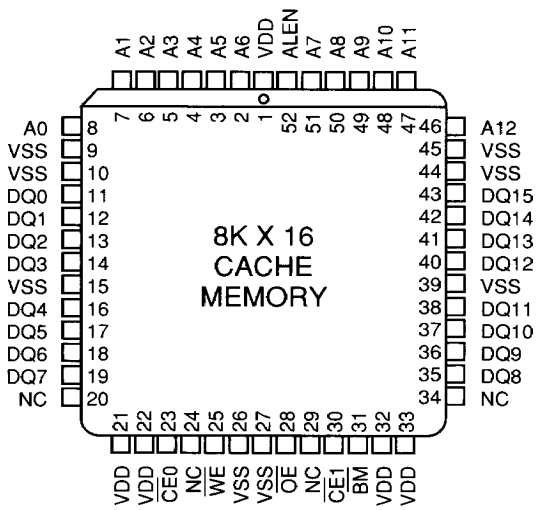
The V63C329 provides several distinct features such as fast output enable access, short data set-up time in WRITE operation, fast Burst Mode operation, and built-in transparent address latches.

Package	Sym	Pin Count
Plastic LCC	J	52

V 6 3 C 3 2 9 J

Family | Device | Package | Speed | Power

PLCC PIN CONFIGURATION Top View



Speed Selection Guide

80386 Speed	V63C329 Speed
20 MHz	01
25 MHz	02
33 MHz	03

Functional Block Diagram

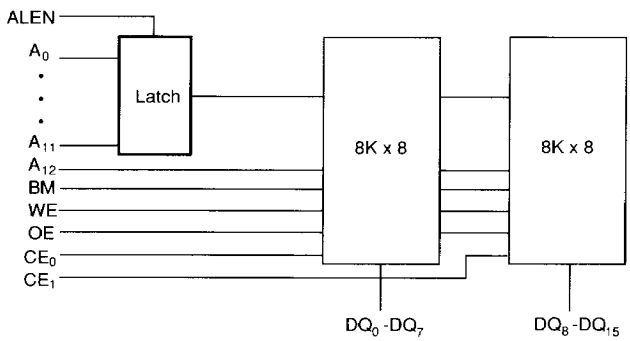


Figure 1

Functional Description

The 8K x 16 Cache Memory consists of two 8K x 8 SRAMs which function as an 8K x 16 Cache. The operation of the V63C329 is controlled by the $\overline{BM}$, $\overline{WE}$, $\overline{OE}$, and $\overline{CE}$ pins as shown in the Truth Table below.

Four V63C329 chips may be used in parallel to provide 64K bytes of Cache operating up to 33 MHz for the Intel 82385, with double word, word, and byte transfers controlled by the Chip Enable, $\overline{CE0}$ and $\overline{CE1}$ pairs. The four chips can be configured as either a 16K x 32 direct mapped Cache or an 8K x 32 two-way set associative Cache. Two banks of 16K x 32 can provide 128K bytes of cache using the $\overline{BM}$ pins to provide bank decoding.

The V63C329 can interface directly with the 80386/82385 system without the use of external data latches and tranceivers. The ALEN signal is used to latch the A0 through A11 address signals into the chip. Address A12 is not latched with ALEN, allowing it to be used as the unlatched least significant bit in 64K and 128K byte cache systems.

The Burst Mode pin ($\overline{BM}$) is gated with the $\overline{WE}$ and $\overline{OE}$ signals internally to provide very high speed read access and write data operations.

The V63C329 has been designed with multiple VSS and VDD pins to improve the noise immunity of the chip. All VSS and VDD pins should be connected to the appropriate ground or power plane.

Truth Table

$\overline{BM}$	$\overline{CE0}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	Operation
L	H	H	X	X	Standby, All Outputs High-Z
L	X	X	H	H	All Outputs High-Z
L	L	H	L	H	Read low byte
L	L	H	X	L	Write low byte
L	H	L	L	H	Read high byte
L	H	L	X	L	Write high byte
L	L	L	L	H	Read word
L	L	L	X	L	Write word
H	X	X	X	X	No operation, all outputs High-Z

Pin Description

A_0–A_{12}	Addresses
DQ_0–DQ_{15}	Data Inputs/Outputs
ALEN	Address Latch Enable
$\overline{BM}$	Burst Mode Control
$\overline{CE_0}$, $\overline{CE_1}$	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{DD}	+5V Power
V_{SS}	Ground

Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	−0.5* to +7.0	V
V_T	Terminal Voltage with Respect to V_{SS}	−0.5* to V_{DD} +0.5	V
P_D	Power Dissipation 100% Duty Cycle	2.0	W
t_{OPR}	Operating Temperature	-10 to +85	°C
t_{STG}	Storage Temperature	−65 to +150	°C

* −3.5V for 20 ns pulse.

NOTE: 1. Operation above absolute maximum rating can affect device reliability.

Capacitance (1)

T_A = 25°C, f = 1MHz

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	—	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	8	pF

NOTE: 1. These parameters are sampled and not 100% tested.

Recommended DC and Operating Characteristics (1)

T_A = 0°C to 70°C, V_{DD} = 5.0V ± 5%, V_{SS} = 0V, unless otherwise noted.

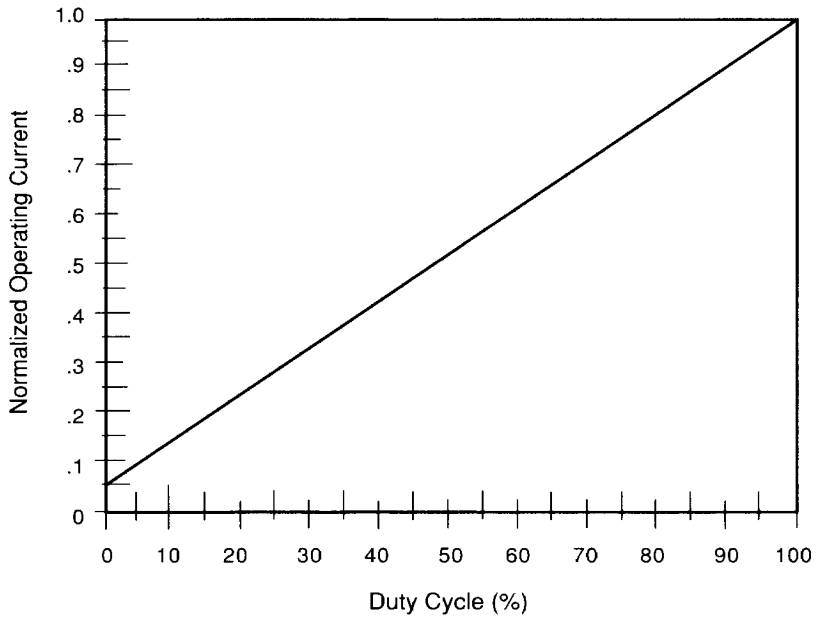
Parameter	Symbol	Min.	Max.	Units	Test Condition
Supply Voltage	V_{DD}	4.75	5.25	V	
Supply Voltage	V_{SS}	0.0	0.0	V	
Input High Voltage	V_{IH}	2.2	V_{DD}+.3	V	
Input Low Voltage	V_{IL}	−0.5*	+0.8	V	
Input Leakage Current	I_{LI}	−10	10	µA	V_{DD} = 5.25V, V_{IN} = V_{SS} to V_{DD}
Output Leakage Current	I_{LO}	−10	10	µA	$\overline{CE}_0 = V_{IH}$, $\overline{CE}_1 = V_{IH}$ $V_{OUT} = V_{SS}$ to V_{DD}
Dynamic Operating Current	I_{CC}		275	mA	$\overline{CE}_0 = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BM} = V_{IL}$ Outputs Open 100% Duty Cycle, 60 ns Cycle Time
Standby Current	I_{SB1}		12	mA	$\overline{CE}_0 = V_{IH}$, $\overline{CE}_1 = V_{IH}$
CMOS Standby Current	I_{SB2}		6	mA	$\overline{CE}_0$ & $\overline{CE}_1 \geq V_{DD}-0.2V$, $V_{IN} \geq V_{DD}-0.2V$ or $V_{IN} \leq V_{SS}+0.2V$
Output Low Voltage	V_{OL}		0.4	V	Active Outputs Open (Note 2) I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −1.0 mA

* −3.5V for 20 ns pulse.

NOTE: 1. Measurement based on AC operating conditions of 33 MHz 82385.

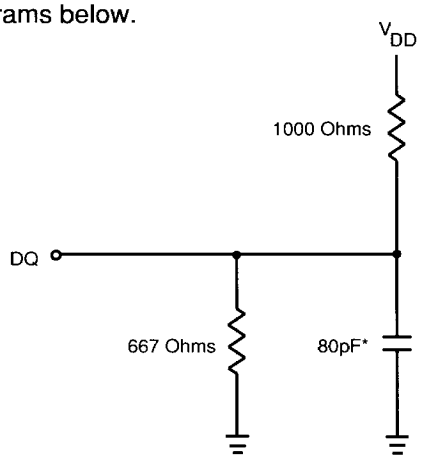
2. All inputs should be in the DC condition.

Normalized Current vs. Duty Cycle



AC Test Loads

Signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0.0V to 3.0V, output loading as shown in the diagrams below.



*Value Includes Scope and Jig Capacitance

Figure 2. Output Load

AC Test Conditions

(Applies to READ and WRITE Cycle Timing)

Input Pulse High Level	V_{IH} = 3.0V
Input Pulse Low Level	V_{IL} = 0.0V
Input Rise Time	t_R = 3 ns
Input Fall Time	t_F = 3 ns
Input and Output Reference Level	1.5V
Output Load	C_L = 80pF, 1 TTL
V_{DD}	5V ± 5%
T_A	0° to +70°C

AC Characteristics

At recommended operating conditions, unless otherwise noted.

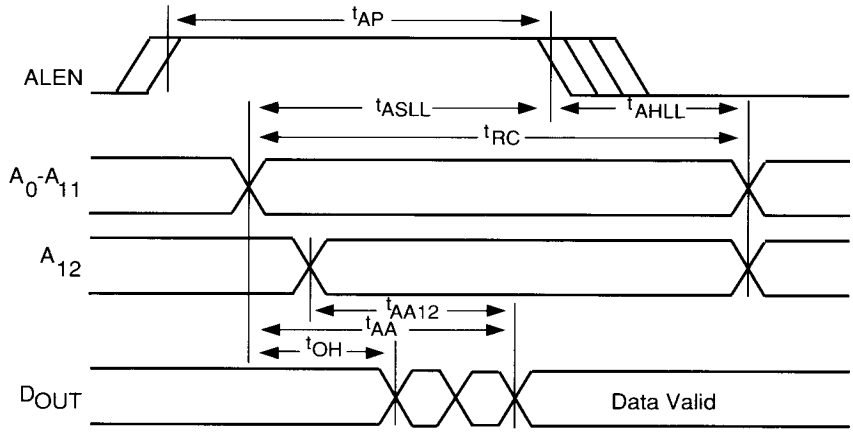
Read Cycle (4)

Symbol	Parameter	01		02		03		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	45	—	40	—	30	—	ns	1
t_{AA}	Address Access Time / ALEN Access Time A_0 - A_{11}	—	45	—	40	—	30	ns	
t_{AA12}	Address Access Time A_{12}	—	25	—	22	—	17	ns	
t_{ACS}	Chip Select Access Time	—	45	—	40	—	30	ns	
t_{OE}	Output Enable to Output Valid	—	13	—	12	—	10	ns	
t_{BMR}	Burst Mode Low to Output Valid	—	25	—	20	—	15	ns	
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns	
t_{LZ}	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns	2, 3
t_{OLZ}	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns	2, 3
t_{HZ}	Chip Disable to Output in High-Z	—	30	—	25	—	15	ns	2, 3
t_{OHZ}	Output Disable to Output in High-Z	—	10	—	7	—	7	ns	2, 3
t_{AP}	Address Latch Enable Pulse Width	15	—	10	—	8	—	ns	
t_{ASLL}	Address Setup to Latch Low	8	—	6	—	4	—	ns	
t_{AHLL}	Address Hold to Latch Low	5	—	5	—	5	—	ns	

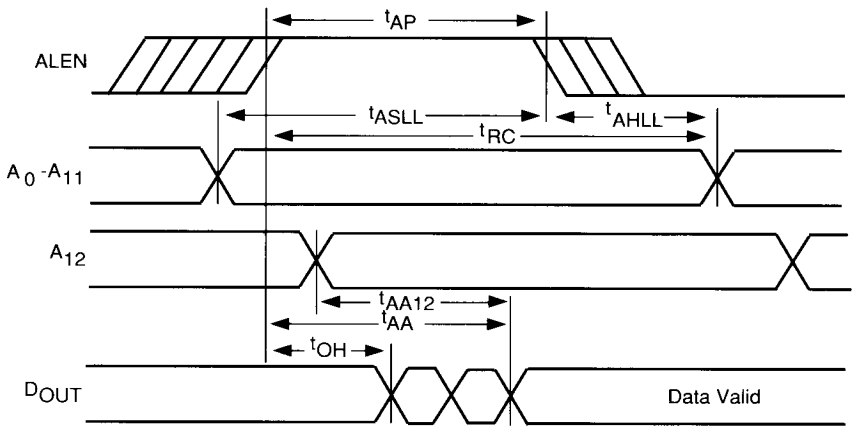
NOTES:

1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 500mV from low or high voltage with load (see figure 2).
4. $\overline{WE}$ is High for read cycle.

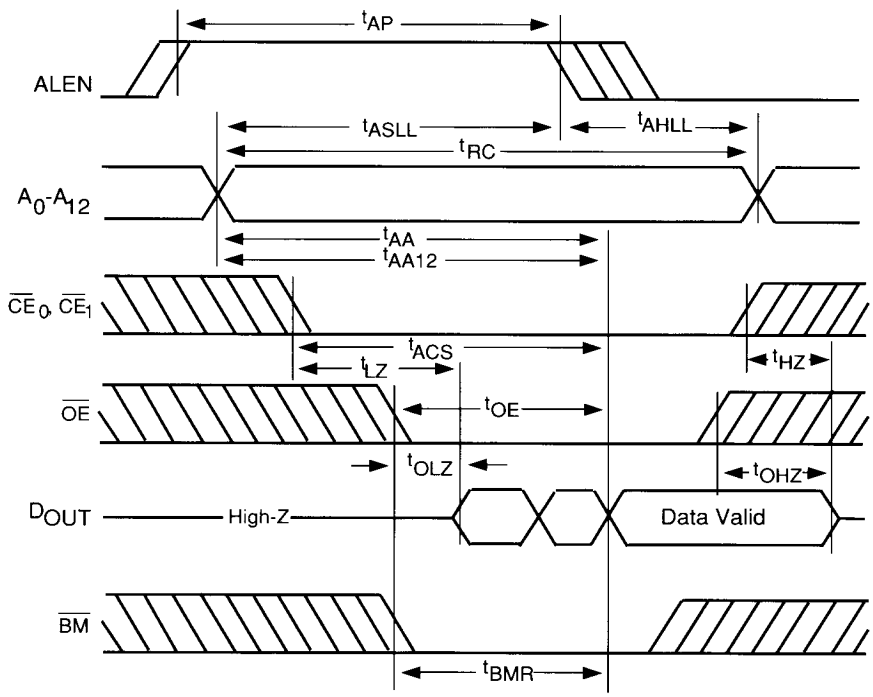
Timing Waveforms of Read Cycle No. 1 (Address Controlled) (4)



Timing Waveforms of Read Cycle No. 2 (ALEN Controlled) (4)



Timing Waveforms of Read Cycle No. 3 (Chip Enable Controlled) (4)



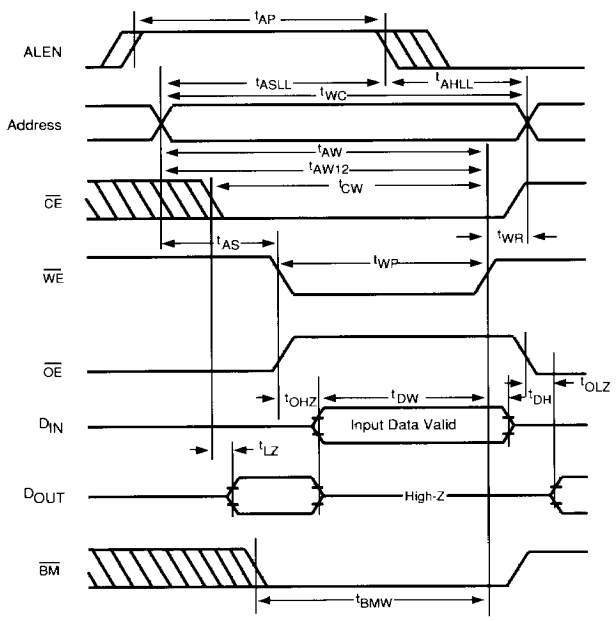
AC Characteristics (continued)
At recommended operating conditions, unless otherwise noted.

Write Cycle (1, 4, 5, 6)

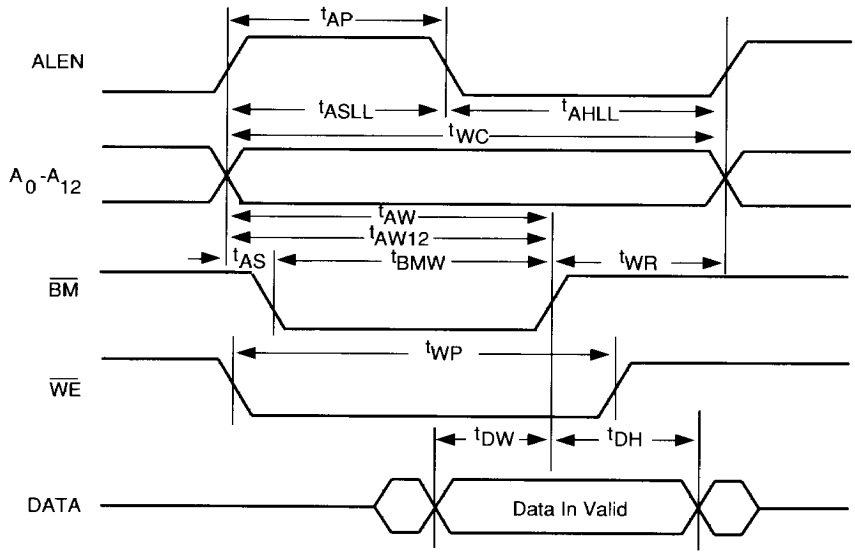
Symbol	Parameter	01		02		03		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	45	—	40	—	30	—	ns	
t_{AW}	Address Valid to End of Write A_0-A_{11}	45	—	35	—	30	—	ns	
t_{AW12}	Address Valid to End of Write A_{12}	25	—	20	—	17	—	ns	
t_{BMW}	Burst Mode to End of Write	25	—	20	—	15	—	ns	
t_{CW}	Chip Select to End of Write	30	—	25	—	18	—	ns	
t_{DW}	Data Valid to End of Write	12	—	12	—	10	—	ns	
t_{WP}	Write Pulse Width	20	—	20	—	18	—	ns	
t_{DH}	Data Hold Time	2	—	2	—	2	—	ns	
t_{AS}	Address Setup Time	5	—	3	—	2	—	ns	
t_{WR}	Write Recovery Time	2	—	2	—	2	—	ns	
t_{LZ}	Chip Enable to Output in Low-Z	5	—	5	—	5	—	ns	2, 3
t_{AP}	Address Latch Enable Pulse Width	10	—	8	—	8	—	ns	
t_{ASLL}	Address Setup to Latch Low	6	—	4	—	4	—	ns	
t_{AHLL}	Address Hold to Latch Low	5	—	5	—	5	—	ns	

NOTES:
1. A write occurs during the overlap of low $\overline{CE}$, low $\overline{BM}$, and low $\overline{WE}$.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 500mV from low or high voltage with load (see Figure 2).
4. $\overline{WE}$ must be high during address transition.
5. If $\overline{OE}$ is high, I/O pins remain in an high impedance state.
6. $\overline{CE}$ must remain static during the Write Cycle, i.e. when $\overline{WE}$ is low. The Write Cycle can only be controlled by the $\overline{WE}$ and $\overline{BM}$ pulse.

Timing Waveforms of Write Cycle No. 1 ($\overline{WE}$ Controlled) (1, 4, 5)

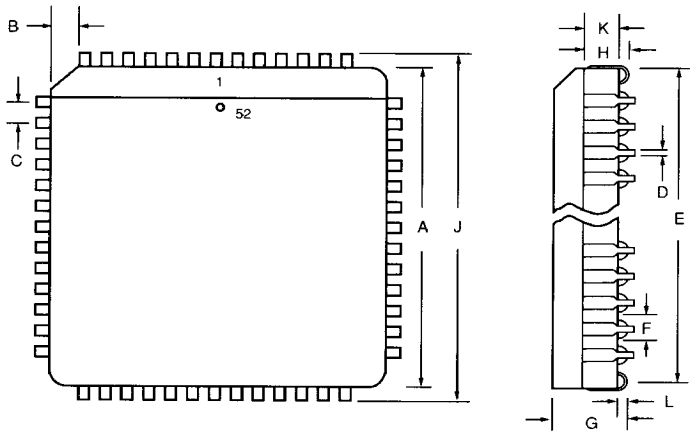


Timing Waveforms of Write Cycle No. 2 ($\overline{BM}$ Controlled) (1, 4, 5)



52 Pin PLCC - J

Dimension	Inches	Millimeters
A	.760 max.	19.30 max.
B	.045	1.14
C	.05.0 typ.	1.27 typ.
D	.017 typ.	.43 typ.
E	.730 max.	18.54 max.
F	.026/.032	.66/.81
G	.180 max.	4.57
H	.098 nom.	2.49
J	.795	20.19
K	.055 nom.	1.40
L	.030/0.45	.76/1.14



(ADJUSTED VIEW)

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