True-Color *Chron*DAC™ with 8-Bit Interface

Features

- Three high speed 8-bit 110/135 MHz DACs
- Three high speed 256 x 6-bit color palette RAMs
- Compatible with ATT20C490 / 491 / 492 display modes
- MIX-COLOR®: true on-the-fly mode switching
- 16.7M, 64K, 32K, and 256 color modes
- Supports: 128/256 pseudo color, 64K LUT and bypass, 32K LUT and HICOLOR™1 & 2, XGA™ mode 2, 16.7M bypass, and MIX-COLOR®
- Internal voltage or external current reference
- Single or dual edge pixel transfer at full speed
- Drives singly and doubly terminated 75 Ω loads
- ID register for software identification
- Power down features for "Green PC" applications
- Anti-sparkle circuitry
- On-chip loop filters for PLL clocks
- Low power CMOS technology in 44-pin PLCC
- 5V supply

Description

The CH8391 *Chron*DAC™ integrates dual-programmable PLLs, a triple 256 x 6-bit color palette RAM, and a triple 8-bit 110/135 MHz DAC. The video clock PLL provides 16 programmable frequencies, and the memory clock PLL provides 8 programmable frequencies.

Upon power up, the video clock is preset to 28.322 MHz, and the memory clock is preset to 40 MHz. After power up, video BIOS or driver software initializes the PLL RAM entries to the desired values.

CH8391 is fully compatible with VGA, Super-VGA, XGA™, TARGA™, and 8514 graphics standards while providing many other enhanced features.

When VCLK is 135 MHz, CH8391 can directly drive a high resolution monitor of 1280 x 1024 pixels at 75 Hz.

MIX-COLOR® mode is Chrontel's unique, true on-the-fly, pixel-by-pixel mode switching. It allows 128 pseudo-color mode mixed with 32K color 5-5-5 bypass mode, or 128 pseudo-color mode mixed with 32K color 5-5-5 LUT mode.

CH8391 is available in two versions: CH8391v and CH8391i. CH8391v has an internal voltage reference, and requires only one resistor to set the full scale current of the DAC. CH8391i requires an external current reference.

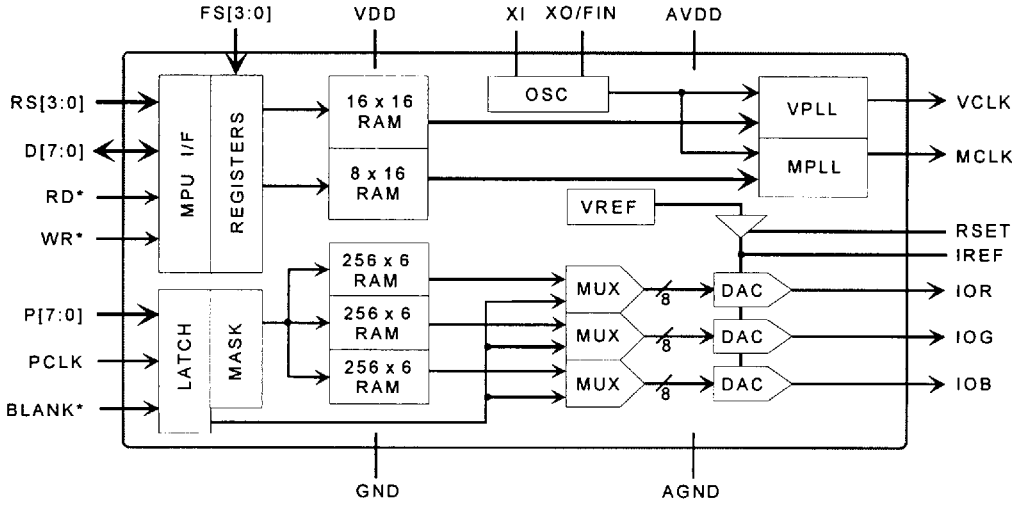

Figure 1: Block Diagram

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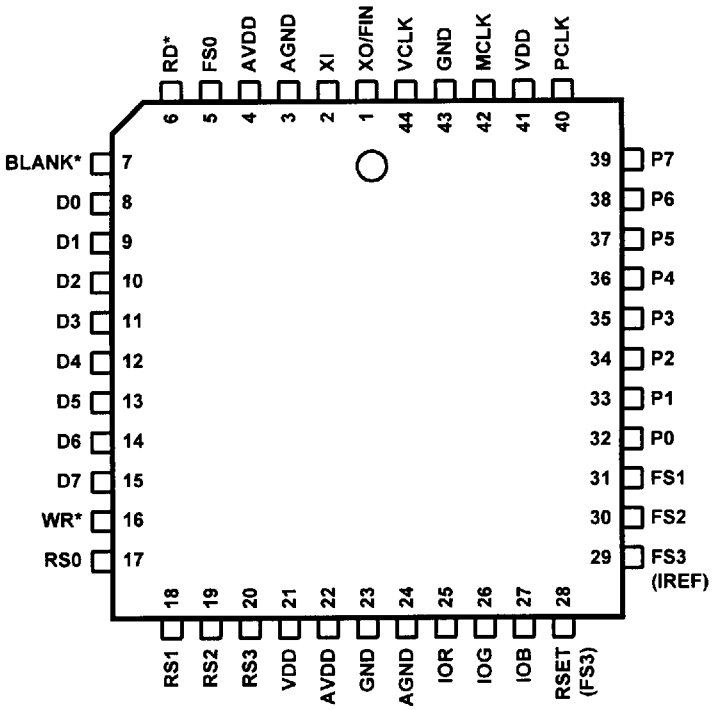

Figure 2: CH8391v

Note: Items in parentheses refer to CH8391i

Table 1 • Pin Description

Pin	Type	Symbol	Name/Description
1	I/O	XO / FIN	**Crystal Oscillator or External Frequency.** 14.318 MHz crystal or external reference clock input.
2	IT	XI	**Crystal Oscillator.** 14.318 MHz crystal or connect to GND if XO / FIN is connected to an external reference clock.
3, 24	P	AGND	**Analog Ground.** AGND pins must be connected to ground.
4, 22	P	AVDD	**Analog Power.** AVDD pins must be connected to 5V.
5, 30, 31	IT	FS0, FS1, FS2	**External Video Clock Select.** TTL compatible with internal pull-down resistor.
6	IT	RD*	**Read (Active Low).** RS[3:0] is latched on the falling edge of RD*.
7	IT	BLANK*	**Blank (Active Low).** Active low composite blanking signal. A logic '0' drives the DAC outputs to the blank level, the pixel inputs are ignored. BLANK* is latched on the rising edge of PCLK.
8 – 15	IT/OT	D0 – D7	**Data Bus.** Bi-directional data bus, should be connected to the MPU data bus.
16	IT	WR*	**Write (Active Low).** RS[3:0] is latched on the falling edge of WR*, and D[7:0] is latched on the rising edge of WR*.
17 – 20	IT	RS0 – RS3	**Register Select.** RS[3:0] is latched on the falling edge of WR* or RD*. They select the type of read or write operation being performed, as illustrated in **Table 3** on page 4-10.
21, 41	P	VDD	**Digital Power.** VDD pins must be connected to 5V.
23, 43	P	GND	**Digital Ground.** GND pins must be connected to ground.
25 – 27	O	IOR, IOG, IOB	**Color Signals Output.** Red, green, and blue DAC outputs; high impedance current sources capable of driving singly or doubly terminated 75 Ω load directly.
28	A	RSET	**Reference Resistor** (CH8391v). This pin should be connected through a resistor to ground. The resistor should be 147 Ω, 1%, 1/4W.
	IT	FS3	**External Video Clock Select** (CH8391i). TTL compatible with internal pull-down resistor. External FS[3:0] is logically "OR"ed with the internal VS[3:0], bits 3 – 0 of clock select register.
29	IT	FS3	**External Video Clock Select** (CH8391v). TTL compatible with internal pull-down resistor. External FS[3:0] is logically "OR"ed with the internal VS[3:0], bits 3 – 0 of clock select register.
	A	IREF	**External current reference source** (CH8391i). See **Figure 16** on page 4-23 for more details.
32 – 39	IT	P0 – P7	**Pixel Data or Address Input.** In pseudo or LUT mode, P[7:0] is the address to the look up table. In bypass mode, the pixel data represents the actual color used to drive the DACs directly. P0 is the LSB, P7 is the MSB.
40	IT	PCLK	**TTL Compatible Pixel Clock.** On dual-edge transfer (HICOLOR™1) pixel data is latched on both the rising and falling edge of PCLK. On single-edge transfer, pixel data is latched on the rising edge of the PCLK. Whether it is a dual- or single-edge transfer, BLANK* is sampled on the rising edge of PCLK.
42	OT	MCLK	**Memory Clock.** Memory clock generator output.
44	OT	VCLK	**Video Clock.** Video clock generator output.

Note: I/O = Input or output signal; IT = TTL compatible input; OT = TTL compatible output; IT/OT = TTL compatible bi-directional signal; I = Input signal; P = Power pins; A = Analog signal; O = Output signal

Display Modes

CH8391 can be used in any of eight different display modes by setting bits 7 through 5 of the Control Register (CR). There are four basic modes: pseudo, Look Up Table (LUT), bypass, and MIX-COLOR®. In pseudo-color mode, the pixel data (P[7:0]) is used to address all red, green, and blue palette RAM. In the LUT mode, 15 or 16 bits of pixel data are required: 5 bits each are the address for each red and blue palette RAM address, 5 or 6 bits for the green palette RAM. In the bypass mode, the pixel data is used to drive the DAC directly bypassing the palette RAM and the Read Mask Register (RMR). MIX-COLOR® mode allows mixing 128 colors in pseudo-color mode with either 5-5-5 LUT or 5-5-5 bypass mode.

All operations, except in bypass mode, use the RMR. The RMR content is "AND"ed with the pixel address, and the result is used to address the color palette RAM. In a multiple byte operation, the first byte after BLANK* goes high (BLANK* = "1") is the Least Significant Byte (LSB).

For dual-edge transfer, the first byte is latched on the next rising edge of PCLK after BLANK* = "1." When using 15- or 16-bit bypass modes (modes 4, 5, and 6), the lowest 2 or 3 bits of the DACs are padded with zeros. See **Figures 4** and **5** on page 4-8.

Table 2 • Display Modes

	CR				
Mode	**7**	**6**	**5**	**Description**	**Number of colors**
0	0	0	0	8-bit pseudo color	256
1	0	0	1	15-bit 5-5-5 LUT	32K
2	0	1	0	MIX-COLOR®	128 + 32K
3	0	1	1	16-bit 5-6-5 LUT	64K
4	1	0	0	15-bit 5-5-5 bypass dual-edge transfer (HICOLOR™1)	32K
5	1	0	1	15-bit 5-5-5 bypass single-edge transfer (HICOLOR™2)	32K
6	1	1	0	16-bit 5-6-5 bypass	64K
7	1	1	1	24-bit 8-8-8 bypass	16.7M

Mode 0: 8-bit Pseudo color

Mode 0 requires: CR[7:5] = 000, one byte per pixel, and one PCLK. P[7:0] pixel data is "AND"ed with the pixel address mask register, resulting in the address for each red, green, and blue LUT. Since P[7:0] data is latched on every rising edge of PCLK, DAC output is updated on every video clock cycle. In this mode, the palette (LUT) contains 256 colors out of 256K possible colors (6 bits for each of the IOR, IOG, and IOB outputs).

Mode 1: 15-bit (5-5-5) LUT

Mode 1 requires: CR[7:5] = 001, two bytes per pixel, and two PCLKs. It provides a palette of 32K colors. The LSB is latched on the first rising edge of PCLK, the Most Significant Byte (MSB) is latched on the next rising edge of PCLK, and bit 15 is ignored. The data is organized as follows: B[14:10] = red address, B[9:5] = green address, and B[4:0] = blue address. These 5 bits of data are padded with 000 on the lowest 3 bits to make the 8-bit address for the LUT. Data is valid when BLANK* is high.

MSB								LSB							
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
X	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B

Mode 2: MIX-COLOR®

Mode 2 requires CR[7:5] = 010, one or two bytes per pixel, and one or two PCLKs. Masking operation is enabled in this mode. To disable the masking operation, write FFH into the Read Mask Register (RMR).

MIX-COLOR® mode is the mixing of 128 colors (7-bit pseudo color) with 32K colors (5-5-5 LUT or 5-5-5 bypass). This enables MIX-COLOR® to provide mixing in two modes: higher spatial resolution with lower color depth, and lower spatial resolution with higher color depth. For example, a simultaneous display of a higher resolution / lower color display (such as word processing or a spread sheet) can be mixed with a lower resolution / higher color display (such as a picture, painting, or photograph).

Bit 0 of the pixel data LSB is used as a signaling bit to the *Chron*DAC™. B0 = 0 indicates a 5-5-5 mode, while B0 = 1 indicates pseudo mode. Control register bit 2 selects the 5-5-5 bypass and LUT modes. CR2 = 0 mixes 128 pseudo color with 5-5-5 bypass mode, and CR2 = 1 mixes 128 pseudo color with 5-5-5 LUT.

B0 = 1 Pseudo-color mode

Pseudo-color mode requires one byte. In MIX-COLOR® mode, the LSB (bit 0) is used for mode change between pseudo and 5-5-5. Although similar to mode 0, this default mode supports only 128 colors (7 bits) instead of 256 colors. The pixel data is latched on every rising edge of PCLK and the DAC is updated on every PCLK.

B0 = 0 5-5-5 LUT / Bypass mode

5-5-5 LUT mode requires 2 bytes of data. Bit 0 of the LSB is "0" for this mode. The LSB is latched first, followed by the MSB. LUT mode uses the data to address the color look up table, whereas bypass mode uses the data to drive the DAC directly. The data is presented in the table below.

	MSB								LSB							
	B7	B6	B5	B4	B3	B2	B1	**B0**	B7	B6	B5	B4	B3	B2	B1	**B0**
Pseudo	P	P	P	P	P	P	P	**1**	P	P	P	P	P	P	P	**1**
5-5-5	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B	**0**

Pseudo to 5-5-5 mode change

When B0 is changed from "1" to "0," the mode changes from pseudo to 5-5-5. Since it takes one byte to change, the current byte is repeated (i.e., the DAC remains the same on the next PCLK). On the subsequent byte the mode is changed to 5-5-5. To remain in 5-5-5 mode, keep B0 of the LSB as "0."

5-5-5 LUT/ bypass to pseudo mode change

To change from 5-5-5 LUT to pseudo mode, set B0 of the next pixel data to "1." The DAC will change on the next PCLK, thus the current byte is shortened. See **Figure 3** below.

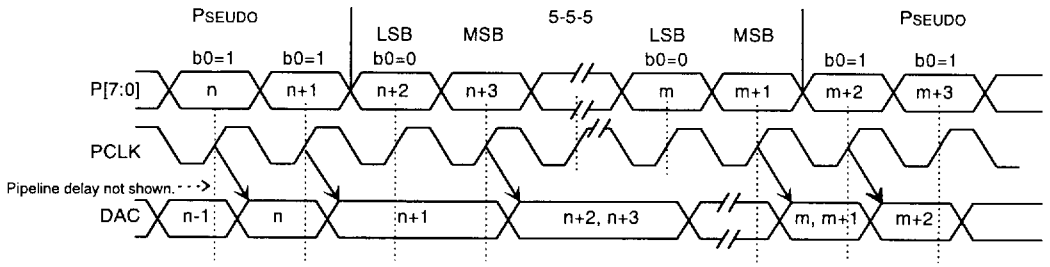

Figure 3: 5-5-5 LUT/Bypass to Pseudo Mode Change

Mode 3: 16-bit (5-6-5) LUT

Mode 3 requires: CR[7:5] = 011, two bytes per pixel, and two PCLKs. Mode 3 is similar to mode 1, except the green data is expanded to 6 bits. The data is organized as follows: B[15:11] = red address, B[10:5] = green address, B[4:0] = blue address. All 16 bits are used, providing 64K colors.

MSB								LSB							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B

Mode 4: 15-bit (5-5-5) Bypass, Dual-edge transfer (HICOLOR™1)

Mode 4 requires: CR[7:5] = 100, two bytes per pixel, dual-edge transfer, and one PCLK. In bypass mode, both the pixel address mask register and look up table are bypassed, with the pixel data directly driving the DAC. Data organization is as follows: B[14:10] = red, B[9:5] = green, B[4:0] = blue, B[15] is ignored. The lowest 3 bits of DAC input is padded with 000. The first LSB is latched on the first rising edge after BLANK* = "1," the MSB is latched on the next falling edge of PCLK. Fifteen bits of pixel data produce 32K possible color combinations. See **Figure 4** below.

MSB								LSB							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B

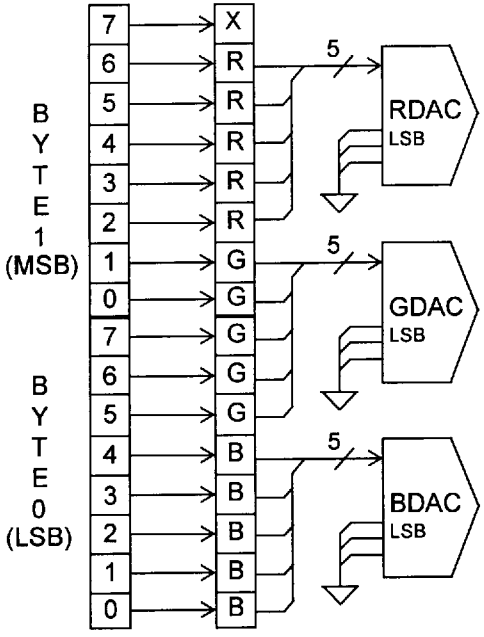

Figure 4: 15-bit Bypass Mode (Mode 4)

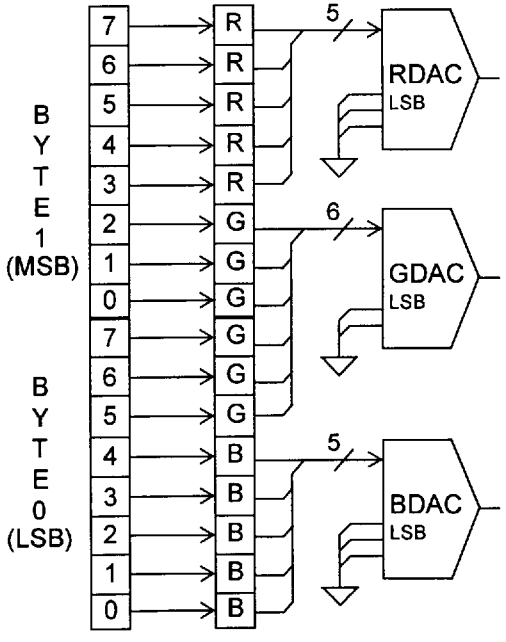

Figure 5: 16-bit Bypass Mode (Mode 6)

Mode 5: 15-bit (5-5-5) Bypass, Single-edge transfer (HICOLOR™2)

Mode 5 requires: CR[7:5] = 101, two bytes per pixel, and two PCLKs. Mode 5 is similar to Mode 4, except in mode 5 the data transfer requires two PCLKs. The LSB and MSB are latched on rising edge of the PCLKs. This mode provides 32K colors. See **Figure 6** below.

MSB								LSB							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B

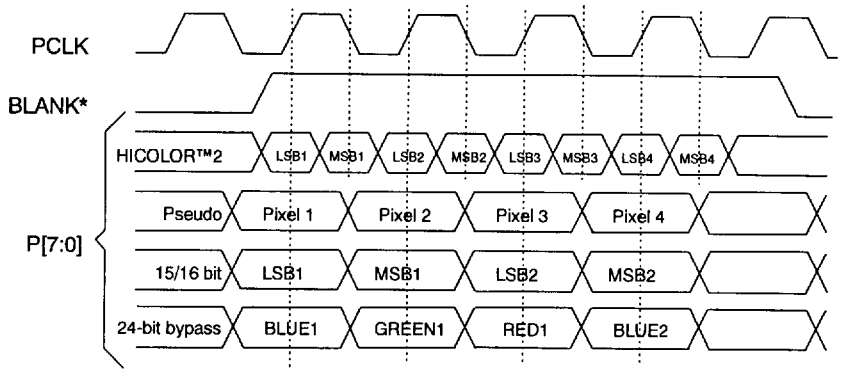

Figure 6: Synchronization of PCLK and P[7:0] of Various Display Modes

Mode 6: 16-bit (5-6-5) Bypass

Mode 6 requires: CR[7:5] = 110, two bytes per pixel, and two PCLKs. Mode 6 is similar to Mode 5, except in Mode 6 the green DAC has 6 bits of color content, resulting in 64K of possible color combinations. The data is organized as follows: B[15:11] = red, B[10:5] = green, B[4:0] = blue. See **Figure 5** on page 4-8.

MSB								LSB							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B

Mode 7: 24-bit (8-8-8) Bypass

Mode 7 requires: CR[7:5] = 111, 3 bytes per pixel, and 3 PCLKs. This is the highest color resolution with 8 bits per DAC, for a total of 24 bits (16.7 million colors). The first valid byte, the blue byte, is latched first after BLANK* goes high. The green byte is latched on the next rising edge, and the red byte is latched on the following rising edge. The sequence starts again with blue, green, and red repeating for each rising edge while BLANK* is still high.

	B7	B6	B5	B4	B3	B2	B1	B0
Byte 0	B	B	B	B	B	B	B	B
Byte 1	G	G	G	G	G	G	G	G
Byte 2	R	R	R	R	R	R	R	R

Table 3 • Register Maps and Definitions

	RS3 (opt)	RS2	RS1	RS0	Description	Default on Power Up
PWA	0	0	0	0	Palette RAM Write Address Register	N/A
PDR	0	0	0	1	Palette RAM Data Register	N/A
RMR	0	0	1	0	Pixel Read Mask Register (IDR, alternate access to control register)	IDR = B3H
PRA	0	0	1	1	Palette RAM Read Address Register	N/A
CWA	0	1	0	0	Clock RAM Write Address Register (alternate access to clock select register)	N/A
CDR	0	1	0	1	Clock RAM Data Register	N/A
CR	0	1	1	0	Control Register	00H
CRA	0	1	1	1	Clock RAM Read Address Register	N/A
CSR	1	0	0	0	Clock Select Register	00H
RSV	1	0	0	1	Reserved	N/A

PWA: Palette RAM Write Address Register

PWA specifies the address to the palette RAM for write access.

PDR: Palette RAM Data Register

PDR contains the data read from the palette RAM or the data to be written to the RAM. The read address is specified by PRA, the write address is specified by PWA.

RMR: Read Mask Register

RMR is used in pseudo, look up table, and MIX-COLOR® modes. Each bit of RMR is logically "AND"ed with each corresponding address bit of the red, green, and blue palette from P[7:0]. The DAC uses the result to address the palette RAM. This register is not initialized upon power up, therefore it should be written upon power up.

IDR: Identification Register

IDR is a read only register with a predefined value of B3H.

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	1	0	0	1	1

PRA: Palette RAM Read Address Register

PRA specifies the address to the palette RAM for read access.

CWA: PLL Clock RAM Write Address Register

CWA specifies the address to the PLL RAM for write access.

CDR: PLL Clock RAM Data Register

CDR contains the data read from the PLL RAM or the data to be written to the RAM. The read address is specified by CRA, the write address is specified by CWA.

CR: Control Register

CR determines the display modes, power down modes, and MPU interface to the color palette RAM.

B7	B6	B5	B4	B3	B2	B1	B0
DM2	DM1	DM0	RSVD	PD1	MXC	8/6*	PD0

B0: **PD0 = Power Down control bit 0.**

For a description, refer to page 4-11, **"B3: PD1 = Power Down control bit 1."**

B1: **8 / 6* = 8-bit or 6-bit MPU interface to color palette RAM**

0 = 6-bit mode

1 = 8-bit mode

For further details, refer to page 4-13, **"MPU Access."**

B2: **MXC = MIX-COLOR® mode select**

0 = 128 pseudo color mixed with 5-5-5 bypass mode

1 = 128 pseudo color mixed with 5-5-5 LUT

For an explanation of MIX-COLOR® (Mode 2), refer to page 4-7, **"Mode 2: MIX-COLOR®."**

B3: **PD1 = Power Down control bit 1**

These power down modes are suited for both LCD and CRT applications. CH8391 *Chron*DAC™ supports both LCD graphics-only controller and LCD graphics controller with simultaneous CRT and LCD display. For CRT/GUI engine applications, power consumption of the graphics subsystem can be greatly reduced, meeting "Green PC" requirements.

B3	B0	
PD1	PD0	Description
0	0	MPLL, VPLL, and LUTDAC are ON; Normal operation mode
0	1	MPLL is ON, VPLL is ON, LUTDAC is OFF For flat panel controller where LUTDAC is not required
1	0	MPLL is ON, LUTDAC and VPLL are OFF MPLL is on, retaining memory image, for both CRT and flat panel applications
1	1	MPLL, VPLL and LUTDAC are OFF Complete power down of graphics subsystem.

B4: **Rsvd = Reserved**

This bit is reserved for future use

B[7:5]: Display Mode control bits

B7	B6	B5	
DM2	DM1	DM0	Description
0	0	0	8-bit pseudo color, 1 PCLK per pixel
0	0	1	5-5-5 LUT, 2 PCLKs per pixel
0	1	0	MIX-COLOR® mode, 1 or 2 PCLKs per pixel
0	1	1	5-6-5 LUT, 2 PCLKs per pixel
1	0	0	5-5-5 bypass, dual edge, 1 PCLK per pixel
1	0	1	5-5-5 bypass, 2 PCLKs per pixel
1	1	0	5-6-5 bypass, 2 PCLKs per pixel
1	1	1	8-8-8 bypass, 3 PCLKs per pixel

CRA: PLL Clock RAM Read Address Register

CRA specifies the address to the PLL RAM for read access.

CSR: Clock Select Register

CSR internally selects MPLL and VPLL frequencies.

CSR[3:0]: VS[3:0] = VPLL select, selects 1 of 16 entries.

These bits are logically "OR"ed with the external FS[3:0].

CSR[6:4]: MS[2:0] = MPLL select, selects 1 of 8 entries.

CSR[7]: PH* = PLL Frequency Holds

CSR[7] = 0, PLL frequency is held at the current value. No change to MCLK or VCLK, regardless of the value written to B[6:0] of this register or the state of external FS[3:0].

CSR[7] = 1, PLL frequency is released, MCLK output depends on the value of CSR[6:4]. VCLK frequency depends on the "OR"ed value of external FS[3:0] with the internal VS[3:0] (CSR[3:0]).

B7	B6	B5	B4	B3	B2	B1	B0
PH*	MS2	MS1	MS0	VS3	VS2	VS1	VS0

RSV: Reserved

This register is for internal use only.

MPU Access

All MPU access is through D[7:0] bus, with RD* and WR* control signals, and RS[3:0] to select which register is to be accessed. Some registers have an alternate access method for graphics controllers that do not provide an RS3 output signal.

8-bit vs. 6-bit Access to the Palette RAM

CR[1] (8/6*) determines the type of interface to the MPU bus only during palette read or write accesses, without affecting other MPU accesses. The default mode, CR[1] = 0, selects the 6-bit mode, whereas CR[1] =1 selects the 8-bit mode. Some mapping and padding are required during read and write accesses for both 6-bit and 8-bit modes, since the MPU bus is 8 bit, the palette RAM is 6 bit, and the DAC is 8 bit.

Since CR[1] controls MPU access to the palette RAM, DAC operations are unaffected. Regardless of the CR[1] value, the palette content is always transferred to the most significant 6 bits of the DAC.

6-bit Access:

Write mode: bits 7 and 6 are ignored, the lower bits are written into palette RAM.

Read mode: bits [5:0] are loaded with palette RAM data; bits 6 and 7 are padded with zeroes.

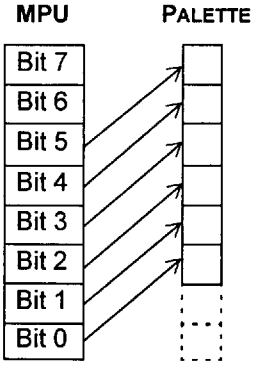

Figure 7: 6-bit Write Mode

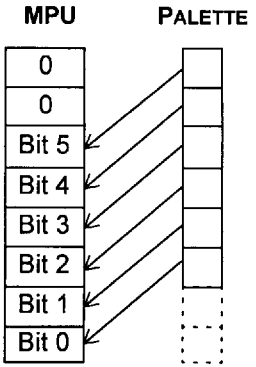

Figure 8: 6-bit Read Mode

8-bit Access:

Write mode: bits [7:2] are written into palette RAM, bits 0 and 1 are ignored.

Read mode: palette RAM data is loaded into the higher 6 bits; bits 0 and 1 are padded with zeroes.

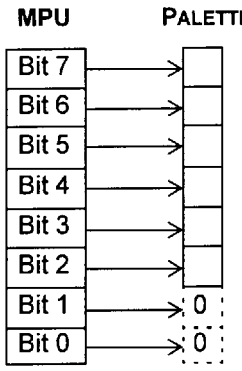

Figure 9: 8-bit Write Mode

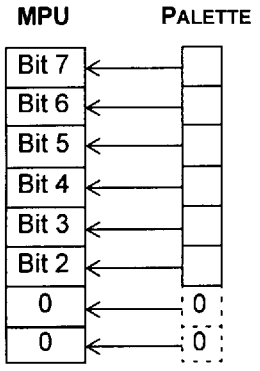

Figure 10: 8-bit Read Mode

Access to the Palette RAM

To write the palette RAM:

Step 1. Load the initial RAM write address to PWA.

Step 2. Write PDR with the red, green, and blue values. The first write is for data to be stored in the red temporary register, the second is the green, and the third is the blue. Internally there is a modulo 3 counter. After the third (blue) write to the PDR, the red, green, and blue data is written to the palette RAM and the address is incremented. The entire palette RAM can be written by sequential writes to PDR. The address rolls over to 00H after reaching FFH. The modulo 3 counter resets after each write to PRA or PWA.

To read the palette RAM:

Step 1. Load the initial RAM read address to PRA. This action triggers a fetch from the palette RAM, transferring the red, green, and blue data to the temporary register. The address is automatically incremented after the fetch.

Step 2. Read the PDR for the red, green, and blue values. The first read is for data stored in the red temporary register, the second to green, and the third to blue. Internally there is a modulo 3 counter. After the third (blue) access, the device triggers another fetch followed by an address increment. The entire palette RAM can be read by sequential reads of the PDR. The address rolls over to 00H after reaching FFH. The modulo 3 counter resets after each write to PRA or PWA.

Table 4 • Palette RAM and PLL RAM Data Organization

Palette RAM			
Address	Byte 0	Byte 1	Byte 2
00H	Red	Green	Blue
01H	Red	Green	Blue
...	...	...	...
...	...	...	...
FEH	Red	Green	Blue
FFH	Red	Green	Blue

PLL RAM			Clock Select	
Address	LSB	MSB	FS[3:0] or VS[3:0]	MS[2:0]
00H	VPLL	VPLL	00H	N/A
...	...	...	...	...
0FH	VPLL	VPLL	0FH	N/A
10H	MPLL	MPLL	N/A	00H
...	...	...	...	...
17H	MPLL	MPLL	N/A	07H

Access to the PLL Clock RAM

Access to PLL clock RAM is similar to the palette RAM, except the modulus counter is modulo 2. Each PLL is two bytes wide: the first access is the LSB, the second is the MSB value. VPLL has 16 locations, occupying the first 32 bytes, while MPLL occupies the next 16 bytes with 8 locations.

To write the PLL clock RAM:

Step 1. Load the initial RAM write address to the CWA.

Step 2. Write CDR with the PLL values. The first write is for the LSB, the second is the MSB. After the MSB write, the PLL data is written to the PLL clock RAM and the address is incremented. The entire PLL RAM can be written by sequential writes to CDR. The internal modulo 2 counter resets after each write to the CRA or CWA.

To read the PLL clock RAM:

Step 1. Load the initial RAM read address to the CRA. This triggers a fetch from the PLL clock RAM, and the data transfers to the temporary register. The address automatically increments after the fetch.

Step 2. Read the CDR for the PLL values. The first read is the access to the LSB, the second is the MSB. After the MSB access, the device triggers another fetch followed by an address increment. The entire PLL RAM can be read by sequential reads of the CDR. The internal modulo 2 counter resets after each write to CRA or CWA.

Access to the ID Register

Step 1. Read the RMR three consecutive times, without accessing any other register between reads.

Step 2. The fourth read returns the content of the ID register, B3H.

Access to the Clock Select Register

There are two methods of accessing the CSR. The first method requires RS[3:0] to be driven to "1000." The alternate method is for controllers that do not have an RS3 output. Alternate access to CSR is as follows:

Step 1. Read the CWA four consecutive times without accessing any other register between reads.

Step 2. The fifth access (read or write) is the CSR. Only one access is allowed for each sequence.

Access to the Control Register

There are two methods of accessing the CR. The first method requires RS[3:0] to be driven to "0110." The alternate access is as follows:

Step 1. Read the RMR four consecutive times without accessing any other register between reads. The fourth read access returns the value of the IDR.

Step 2. The fifth access (read or write) is the CR. Only one access is allowed for each sequence.

PLL Clock Generator

CH8391 incorporates Chrontel's proprietary PLL technology, which is capable of generating any frequency from 8 MHz to 135 MHz by writing the appropriate values to the PLL RAM. By connecting an external crystal to the on-chip parallel mode crystal oscillator, the reference frequency can be generated easily. The internal crystal oscillator range is from 10 MHz to 20 MHz. Typically, a 14.318 MHz crystal is used.

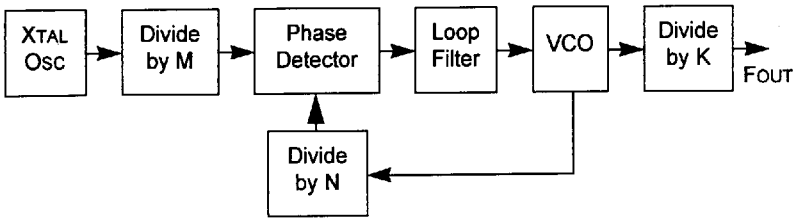

Figure 11: PLL Block Diagram

The formula for calculating the output frequency is as follows:

$$F_{OUT} = F_{REF} \times \frac{n}{m \times k}$$

where:
F_{REF} = 14.318 MHz (for normal operation)
m = M + 2
n = N + 8
$k = 2^K$

Data Format:

	B7	B6	B5	B4	B3	B2	B1	B0
LSB	N7	N6	N5	N4	N3	N2	N1	N0
MSB	K1	K0	M5	M4	M3	M2	M1	M0

Certain values of N are restricted, including: 0-7, 10-15, 19-23, 28-31, 37-39, 46, 47, 55. For frequencies not listed below please contact Chrontel.

Table 5 • Sample Frequency Coefficients (reference frequency = 14.318 MHz)

FOUT	M	N	K
14.318	8	72	3
25.06	3	27	2
25.20	23	168	2
25.95	6	50	2
27.44	7	61	2
28.28	8	71	2
28.33	21	174	2
28.64	2	24	2
30.07	3	34	2
31.50	8	80	2
32.57	8	83	2
33.75	5	58	2
35.89	3	17	1
37.59	6	34	1
38.48	6	35	1
40.09	8	48	1
43.98	5	35	1
44.74	6	42	1
47.25	3	25	1
50.11	3	27	1
51.90	6	50	1
54.89	7	61	1

FOUT	M	N	K
56.56	8	71	1
57.27	2	24	1
60.14	3	34	1
63.00	8	80	1
65.15	8	83	1
67.50	5	58	1
71.59	3	17	0
75.17	6	34	0
76.96	6	35	0
80.18	8	48	0
87.95	5	35	0
89.49	6	42	0
94.50	3	25	0
100.23	4	34	0
105.00	7	58	0
108.18	7	60	0
109.77	7	61	0
118.12	2	25	0
120.27	3	34	0
130.91	5	56	0
135.00	5	58	0

Note: Use M values of 10 or less for best circuit performance

Electrical Specifications

Table 6 • Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	VDD relative to GND			7.0	V
	Input voltage of all digital pins[1]	GND – 0.5		VDD+0.5	V
	Analog output short circuit duration			Indefinite	Sec
TSTOR	Storage temperature	–65		150	°C
TJ	Junction temperature			150	°C
TVPS	Vapor phase soldering (one minute)			220	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1 The device is fabricated using high-performance CMOS technology. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5V can induce destructive latchup.

Table 7 • Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VDD	Supply voltage	4.75	5.00	5.25	V
TA	Ambient operating temperature	0	25	70	°C
RL	Output load to DAC outputs		37.5		Ω
IREF	Reference current RS-343A output PS/2™ compatible	–3.0 –3.0	–8.39 –8.88	–10.0 –10.0	mA mA

Table 8 • DC Characteristics (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ± 5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
	Resolution (each DAC)		8	8	8	Bits
	Accuracy (each DAC):					
LI	Integral linearity error				±1	LSB
LD	Differential linearity error				±1	LSB
	Gray scale error				±5	%
	Monotonicity	Guaranteed				
	Coding	Binary				

Table 9 • Digital Inputs / Outputs

Symbol	Description	Test Condition @ T_A = 25°C	Min	Typ	Max	Units
V_{OH}	Output high voltage	I_{OH} = –400µA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 3.2 mA			0.4	V
V_{IH}	Input high voltage		2.0		V_{DD} + 0.5	V
V_{IL}	Input low voltage		GND – 0.5		0.8	V
I_{LK}	Input leakage current (except for FS[3:0])		–10		10	µA
I_{PLD}	Input pull down current (FS[3:0])	V_{IN} = 0.5V			20	µA
C_{DIN}	Input capacitance (except for XI, XO / FIN)	f = 1 MHz, V_{IN} = 2.4V			7	pF
C_{DIN}	Input capacitance (XI, XO / FIN)	f = 1 MHz, V_{IN} = 2.4V		20		pF
I_{OZ}	Tri-state current				50	µA
C_{DOUT}	Output capacitance				7	pF

Table 10 • Analog Outputs (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ± 5%)

Symbol	Description	Test Condition @ TA = 25°C	Min	Typ	Max	Units
I_{GRAY}	Gray scale current range				20	mA
I_{WB}	White level relative to black RS-343A PS/2™		 16.74 18.00	 17.62 18.65	 18.50 20.00	mA
	Black level relative to blank			0		mA
I_{BLNK}	Blank level			0		mA
	DAC-to-DAC matching			2	5	%
V_{OC}	Output compliance		–1.0		+1.5	V
Z_{AOUT}	Output impedance			10		kΩ
C_{AOUT}	Output capacitance	f = 1 MHz, I_{OUT} = 0 mA			30	pF
I_{VREF}	Voltage reference input current			10		µA
PSRR	Power supply rejection ratio				0.5	%/% VDD

Table 11 • AC Characteristics

Symbol	Description	110	135	Units
F_MAX	Single-edge data clock rate	110	135	MHz
F_MAX	Dual-edge data clock rate	110	135	MHz
t1_MIN	RS[2:0] setup time	10	10	ns
t2_MIN	RS[2:0] + hold time	10	10	ns
t3_MIN	RD* active to data asserted	5	5	ns
t4_MAX	RD* active to data valid	30	30	ns
t5_MAX	RD* inactive to data tristated	15	15	ns
t6_MIN	Read data hold time	5	5	ns
t7_MIN	Write data setup time	10	10	ns
t8_MIN	Write data hold time	10	10	ns
t9_MIN	RD*, WR* low pulse width	50	50	ns
t10_MIN	RD*, WR* high pulse width	7	7	PCLK cycles
t11_MIN	Pixel and control setup time	2	2	ns
t12_MIN	Pixel and control hold time	2	2	ns
t11_MIN	BLANK* setup time	2	2	ns
t12_MIN	BLANK* hold time	2	2	ns
t13_MIN	Clock cycle time	9.09	7.4	ns
t14_MIN	Clock pulse width high	3.5	3	ns
t15_MIN	Clock pulse width low	3.5	3	ns
t16_MAX	Analog output delay	30	30	ns
t17_TYP	Analog output rise / fall time	2	2	ns
t18_MAX	Analog output settling time	9	7.4	ns
TYP	Glitch impulse energy[1]	75	75	pV – sec
TYP	DAC-to-DAC crosstalk	–23	–23	dB
MAX	Analog output skew	2	1.5	ns
MIN MAX	Pipeline delay	5 7	5 7	PCLK cycles PCLK cycles
IDD_TYP	VDD supply current[1]	180	180	mA
IPD1_TYP IPD2_TYP IPD3_TYP	Power down mode[1] Mode 1: MPLL & VPLL ON, LUTDAC OFF Mode 2: MPLL ON, VPLL & LUTDAC OFF Mode 3: MPLL, VPLL, & LUTDAC OFF	 55 35 2	 55 35 2	 mA mA mA

Note: 1 MCLK = 40 MHz and VCLK = 28.32 MHz

Test Conditions: Unless otherwise specified, the testing conditions are the same as in **Table 7, "Recommended Operating Conditions,"** on page 4-18. TTL input values are 0 – 3V, with input rise / fall times < 3 ns, measured between the VIL and VIH. Timing reference points at 50% for non-TTL inputs and outputs. TTL reference points at 1.5V for inputs and outputs. Analog output load < 10 pF, D[7:0] output load < 45 pF.

Timing Diagrams

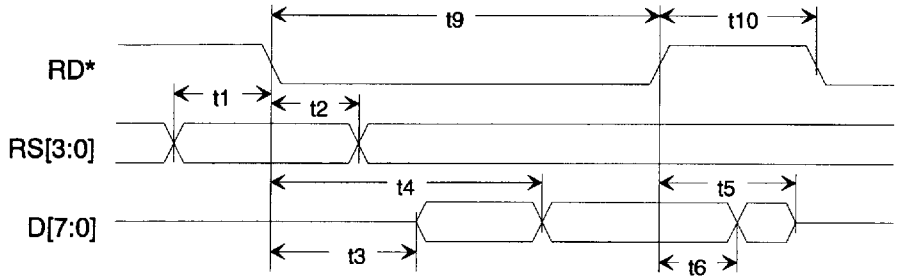

Figure 12: MPU Read Timing Diagram

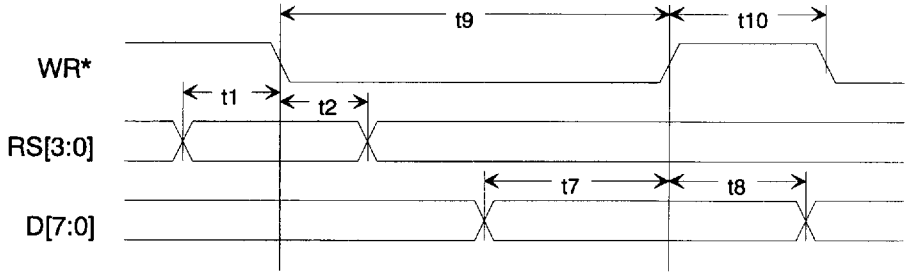

Figure 13: MPU Write Timing Diagram

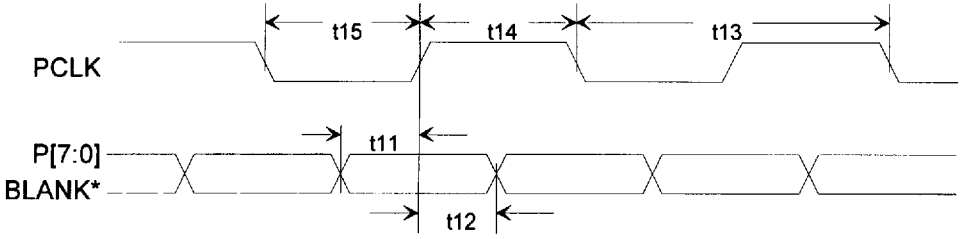

Figure 14: Pixel Data and BLANK* Timing

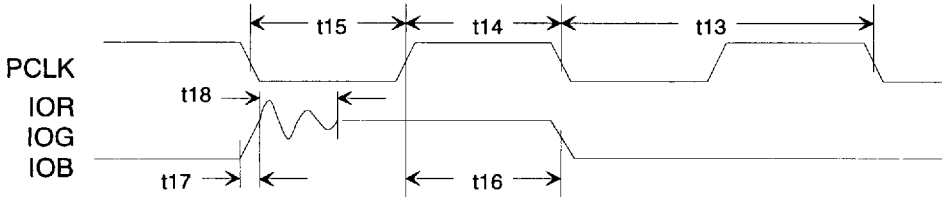

Figure 15: DAC Output Timing

PC Board Layout Considerations

CH8391 is a high performance mixed signal IC containing precision analog and digital circuits. In order to achieve high performance, it is important to optimize the PC board layout (PCB) for the CH8391. Care should be taken in laying out the power and ground planes to ensure good decoupling. In general, analog outputs should be short and wide to minimize inductive ringing, and analog signal traces crossover to digital signals should be minimized. When operating the device at high frequencies (> 50 MHz), the pixel data bus (P[7:0]) and the clock signals should have dedicated drivers. These signal traces should be kept short and placed beside each other so the signal delays through the interconnects are matched, to minimize clock and data skew of the pixel bus.

Ground Planes

For four-layer PCBs with a uniform ground plane, CH8391 and its associated analog components (e.g., decoupling circuitry, current reference, and voltage reference) can be connected to the ground plane directly. The connections to the ground plane should be made with wide traces to minimize inductance. Connecting the analog and digital ground pins directly to the ground plane is highly recommended.

Supply Decoupling

For the digital power supply, bypass capacitors (0.1 µF) are recommended. Make leads as short as possible and place the capacitor as close as possible to the device. Connect the ground side of the capacitors directly to the ground plane.

For AVDD pin 22, a pi-filter configuration is recommended, with a 10 µF tantalum capacitor to GND, followed by a ferrite bead in series, then a 0.1 µF ceramic capacitor close to the AVDD pin.

For AVDD pin 4, a 5.1V zener diode with a 0.1 µF ceramic capacitor for supply conditioning would result in optimal performance.

In general, short leads and direct connection to the power supply and ground planes are highly desirable. For further details, refer to **Figure 18** on page 4-25.

Clock Signals

In applications where either the video or memory clock frequencies are pushed toward the performance limit of the system, AC coupling circuitries should be used. This will allow for minor duty cycle adjustments for these high frequency signals. For additional information, please refer to **Application Notes, AN-O3.**

Digital Signal Interconnect

Place digital signals of the pixel bus, P[7:0] and PCLK, alongside each other to minimize data and clock skew. At high frequencies, these signals should have short traces, dedicated drivers, and series termination damping resistors to minimize signal reflections.

Analog Signal Interconnect

In general, analog signal traces should be as short as possible. Therefore, CH8391 should be located as close as possible to the VGA controller and output connector to minimize the amount of noise and transmission-line reflection due to impedance mismatch between the PCB and cable. Video outputs should overlay the analog ground plane to maximize supply rejection. To cut down the amount of transmission-line reflection, connect a 75 Ω resistor with short leads between each video output and ground. Make the connection as close to the device as possible.

Some designs, such as VESA local bus, may have restrictions on component placement. For further discussion of this issue, please refer to **"Component Placement"** on page 4-26.

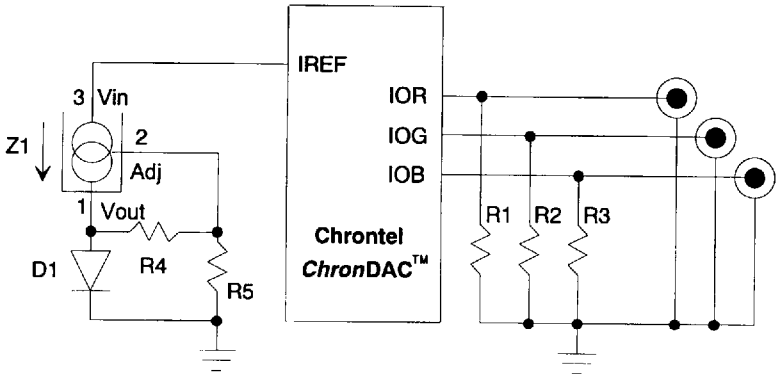

Figure 16: Typical Connection Using External Current Reference

4

Table 12 • Parts List for Figure 16

Symbol	Description
D1	1N914 small signal diode
R1, R2, R3	75 Ω, metal film resistor
R4	18 Ω, 1/4W resistor
R5	180 Ω, 1/4W resistor
Z1	LM334Z or equivalent current reference

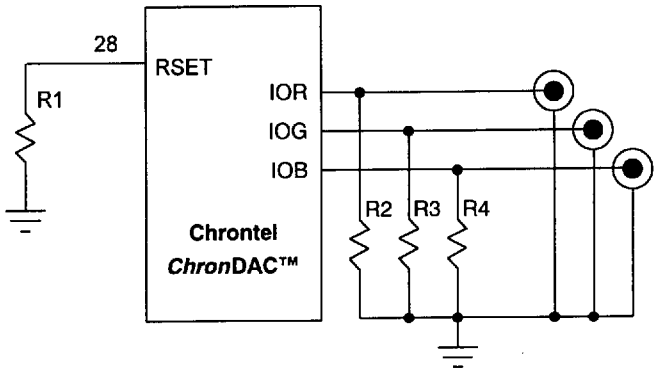

Figure 17: Typical Connection Using Internal Current Reference

Table 13 • Parts List for Figure 17

Symbol	Description
R1	147 Ω, 1/4W resistor
R2, R3, R4	75 Ω, 1/4W resistor

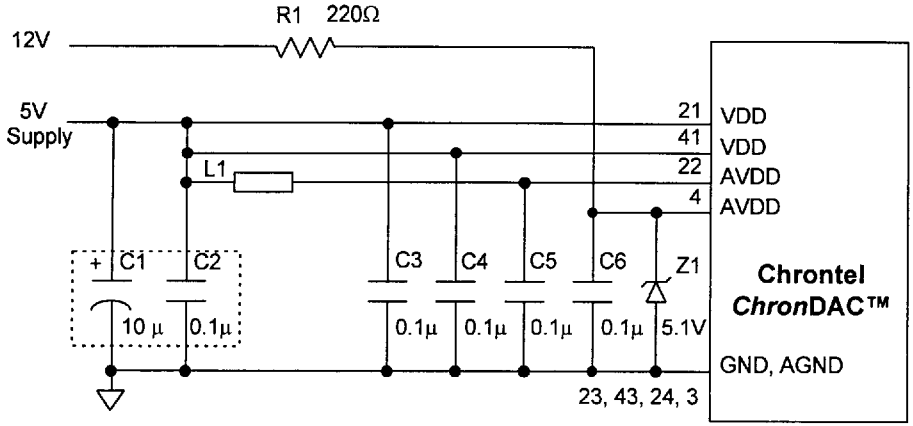

Figure 18: Recommended Supply Decoupling

4

Table 14 • Parts List for Figure 18

Symbol	Description
C1	10 µF tantalum capacitor
C2, C3, C4, C5, C6	0.1 µF ceramic capacitor
L1	Ferrite bead
R1	220 Ω, 1/4W resistor
Z1	1N4733A 5.1V zener or equivalent current reference

Component Placement

Figure 19 is an example of typical placement of VGA components on a local bus VGA adapter. CH8391 should be placed as close as possible to the VGA controller, since there are high speed signals between these two devices. For most local bus implementation, the VGA controller will be placed in close proximity to the local bus connector. Due to the low impedance nature of the CH8391 RGB outputs, they can be located farther from the VGA monitor connector. Micro-strips or strip lines with characteristic impedance of 75 Ω should be used to route these outputs to the video connector.

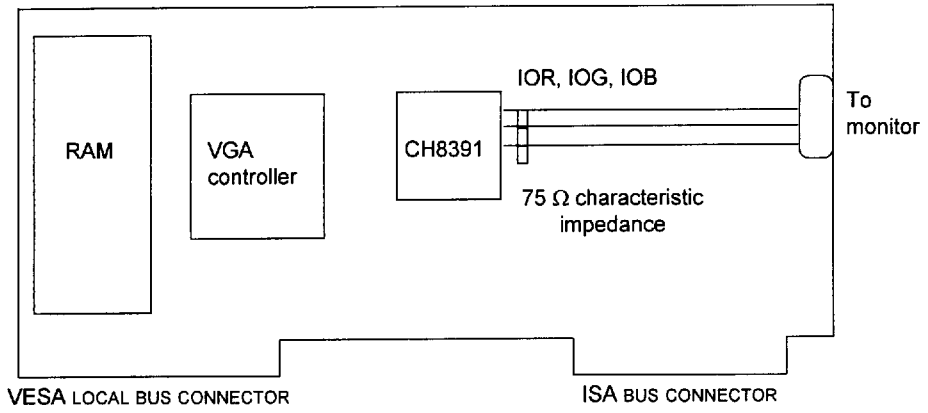

Figure 19: Example of Component Placement for Local Bus VGA Adapter

ORDERING INFORMATION				
Part number	Package type	Number of pins	Voltage supply	Description
CH8391v	PLCC	44	5V	Internal voltage reference
CH8391i	PLCC	44	5V	External voltage reference