VITELIC

V63C64
HIGH PERFORMANCE, LOW POWER 8K x 8 BIT CMOS STATIC RAM

Features

- High speed
  - Maximum access times of 25, 30, 35, 45, and 55 ns
- Equal access and cycle times
- Fully static operation
  - No clock or refresh required
- Output enable and two chip enable inputs for ease in application
- Output Enable time as fast as 9 ns
- TTL compatible inputs and outputs
- Low Power Consumption
  - Standard Power (typ)
    - Active 600 mW
    - Standby 500 µW
  - Low Power (typ)
    - Active 500 mW
    - Standby 25 µW
- Battery Backup
  - 2 volt data retention
- Six transistor memory cell for greater reliability

Description

The V63C64 is a high speed, low power, 8192-word by 8-bit CMOS static RAM fabricated using high performance CMOS technology. This high reliability process coupled with innovative circuit design techniques, yields access times as low as 25 ns maximum.

Two Chip Enable inputs, $\overline{CE}_1$ and CE_2 provide flexibility in system design and make memory expansion easy. When $\overline{CE}_1$ is high, the device assumes a low-power standby mode in which device power dissipation is reduced. Operation is from a single 5V (±10%) power supply. A low-power (L) version is offered with standby current as low as 5µA.

The V63C64 is available in a space-saving 300 mil plastic DIP. The pinout is compatible with 2764 type EPROMs and other industry standard 8K x 8 SRAMs.

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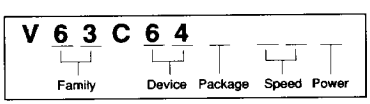
Package	*Symbol*	*Pin Count*
Plastic DIP	S	28

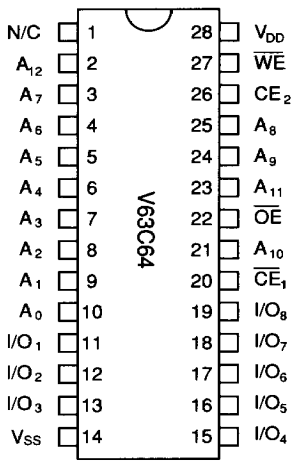


Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)					Power		Temperature Mark
	S	25	30	35	45	55	Std.	Low	
0°C to 70°C	•	•	•	•	•	•	•	•	Blank

V63C64 Rev. 04 6/90

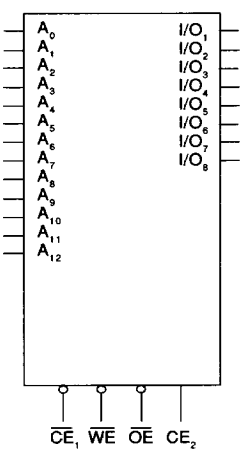
DIP PIN CONFIGURATION
Top View



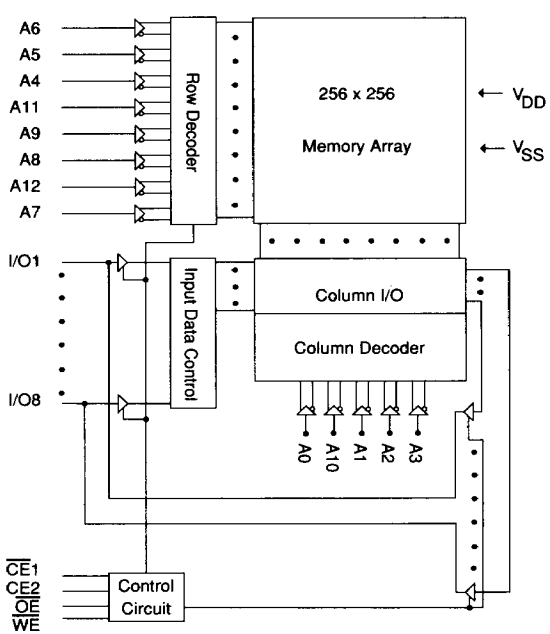
Truth Table

Mode	$\overline{OE}$	$\overline{CE_1}$	CE_2	$\overline{WE}$	I/O	I_{DD}
Not Selected Power Down	X	H	X	X	High-Z	Standby
Not Selected	X	X	L	X	High-Z	Active
Outputs Disabled	H	L	H	H	High-Z	Active
Read	L	L	H	H	D_{OUT}	Active
Write	X	L	H	L	D_{IN}	Active

Logic Symbol



Block Diagram



Absolute Maximum Ratings*

Storage Temperature .....-65°C to +150°C
Ambient Temperature
Under Bias .....-55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} Voltage ..... -0.5 to +7.0V
Maximum V_{DD} Voltage 7.0V
Data Out Current 20mA
Power Dissipation 1.0W

* **NOTE:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

AC Test Conditions

Input pulse levels ..... 0 to 3.0V*
Input rise/fall time ..... 5 ns max.*
Input/Output timing levels 1.5V
Output Load—As specified in Figure 2 or Figure 3 (includes jig and/or scope capacitance)
*Refer to Figure 1

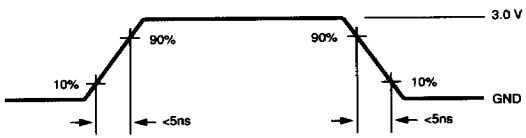


Figure 1. Input Pulse Specification for AC Testing

Recommended Operating Conditions

(T_A = 0° to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{DD}	V
V_{IL}	Input Low Voltage	-0.5		0.8	V

Capacitance*

(T_A = 25°C, f = 1 MHz, V_{DD} = 0 V)

Symbol	Parameter	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	5	pF
$C_{I/O}$	I/O Capacitance	—	7	pF

* Capacitance is sampled and not 100% tested.

6

AC Test Conditions

Signal transition of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0.0 to 3.0V, output loading as shown in diagrams below.

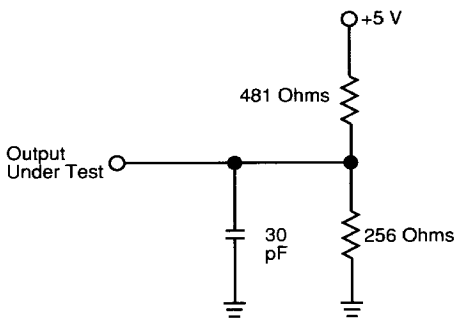


Figure 2. AC Test Load

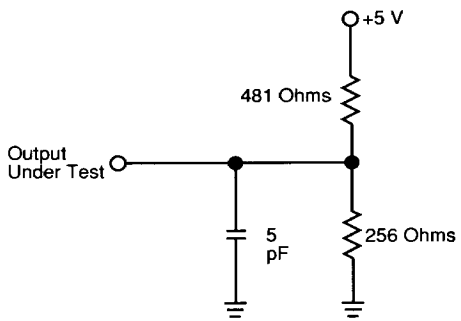


Figure 3. AC Test Load

D.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	V63C64			V63C64L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$	-10		10	-10		10	µA
I_{LO}	I/O Leakage Current	$V_{SS} \le D_{OUT} \le V_{DD}$ Outputs Disabled	-10		10	-10		10	µA
I_{SB1}	TTL Standby Current	V_{DD} = 5.5 V, $\overline{CE}_1 \ge V_{IH}$		15	25		15	25	mA
I_{SB2}	CMOS Standby Current	V_{DD} = 5.5V, $\overline{CE}_1 > V_{DD}$ -0.3 or $CE_2 < V_{SS}$ +0.3		100	2000		5	100	µA
V_{OH}	Output High Voltage	V_{DD} = 4.5 V I_{OH} = -4.0 mA	2.4			2.4			V
V_{OL}	Output Low Voltage	V_{DD} = 4.5 V I_{OL} = 8.0 mA		0.4				0.4	V

Symbol	Parameter	Test Conditions	V63C64					V63C64L			Unit
			25	30	35	45	55	35	45	55	
I_{DD}	Operating Current	V_{DD} = 5.5V 100% Duty Cycle I_{OUT} = 0	150	145	140	120	120	120	120	120	mA

AC Characteristics (1)

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V unless otherwise specified.

Read Cycle

Symbol	Parameter	25		30		35		45		55		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Read Cycle Time	25		30		35		45		55		ns	
t_{AA}	Address Access Time		25		30		35		45		55	ns	
t_{OH}	Output Hold Time	5		5		5		5		5		ns	
t_{ACE1}	$\overline{CE}_1$ Access Time		20		25		30		35		45	ns	
t_{ACE2}	CE_2 Access Time		20		22		25		30		40	ns	
t_{OE}	$\overline{OE}$ Access Time		9		12		15		20		25	ns	
t_{OLZ}	$\overline{OE}$ to Low-Z Output	0		0		0		0		0		ns	
t_{OHZ}	$\overline{OE}$ to High-Z Output		9		12		15		20		25	ns	2
t_{LZCE1}	$\overline{CE}_1$ to Low-Z Output	5		5		5		10		10		ns	3
t_{LZCE2}	CE_2 to Low-Z Output	5		5		5		5		5		ns	3
t_{CHZ}	$\overline{CE}_1$/CE_2 to High-Z Output		12		15		15		20		20	ns	2, 3
t_{PU}	$\overline{CE}_1$ to Power Up	0		0		0		0		0		ns	
t_{PD}	$\overline{CE}_1$ to Power Down		20		20		20		25		25	ns	

Write Cycle (4)

At recommended operating conditions, unless otherwise specified.

Symbol	Parameter	25		30		35		45		55		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{WC}	Write Cycle Time	25		30		35		45		55		ns	
t_{CW1}	$\overline{CE}_1$ to End of Write	20		25		30		35		45		ns	
t_{CW2}	CE_2 to End of Write	20		22		25		30		40		ns	
t_{AW}	Address Setup to End of Write	20		25		30		35		45		ns	
t_{AH}	Address Hold from End of Write	0		0		0		0		0		ns	
t_{AS}	Address Setup to Start of Write	0		0		0		0		0		ns	
t_{WP}	Write Pulse Width	15		20		25		30		35		ns	5
t_{DS}	Data Setup to End of Write	12		15		20		25		30		ns	
t_{DH}	Data Hold from End of Write	0		0		0		0		0		ns	
t_{WHZ}	$\overline{WE}$ Low to High-Z Outputs		12		15		15		20		20	ns	2
t_{WLZ}	$\overline{WE}$ High to Low-Z Outputs	0		0		0		0		0		ns	

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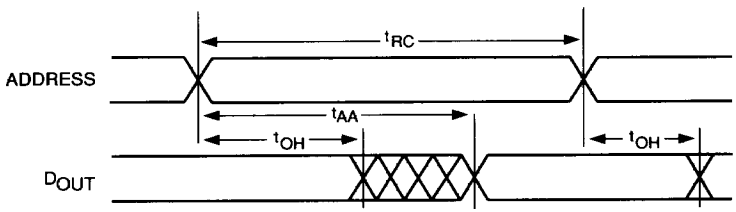
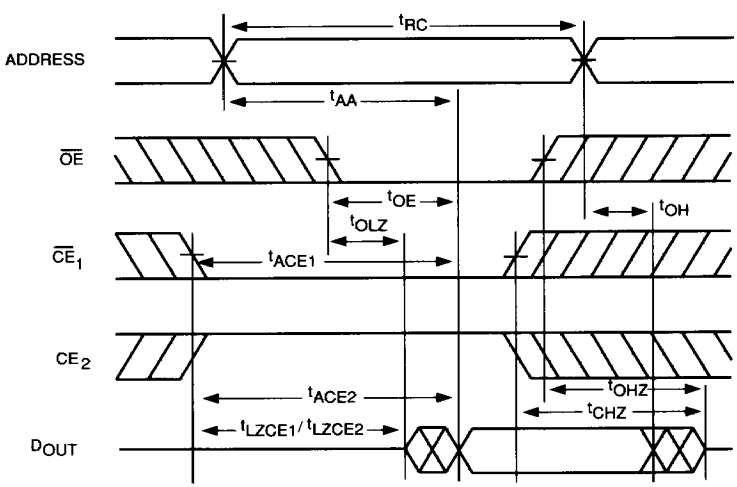
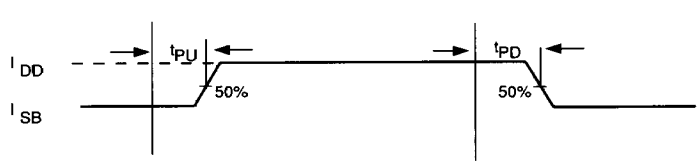
Read Cycle No.1 (Address Controlled) (5, 6)



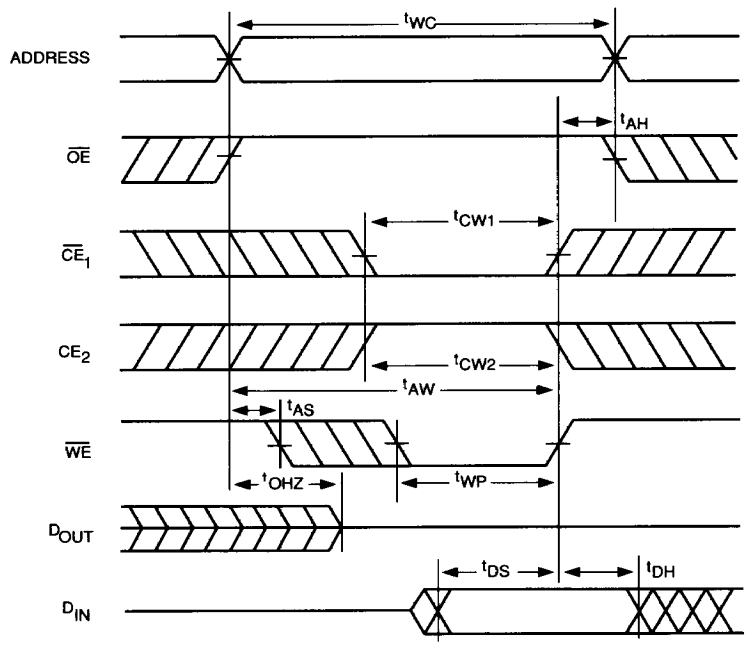
Read Cycle No. 2 (Chip Enable Controlled) (5,7)



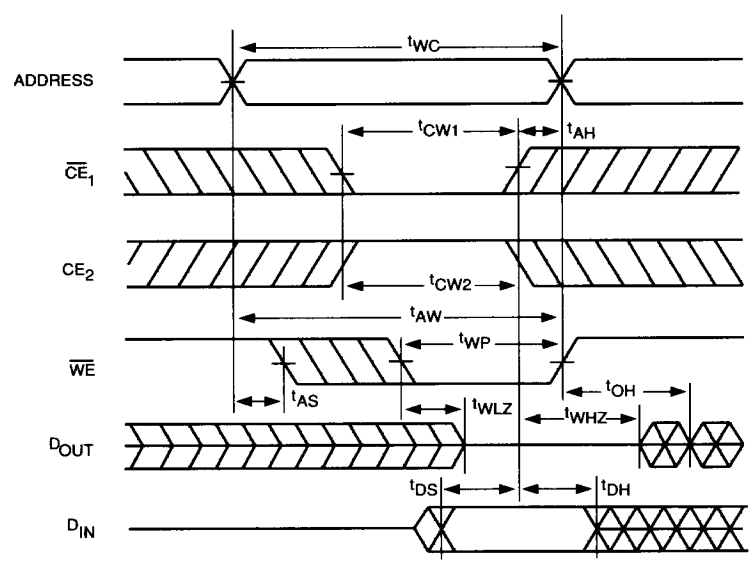
Standby Current (Chip Enable Controlled)



Write Cycle No. 1 (Write Enable Controlled) (4, 8)



Write Cycle No. 2 (Chip Enable Controlled) (4, 8)



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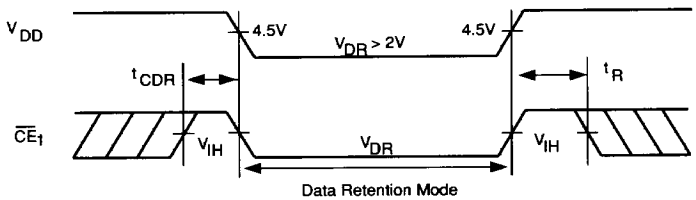
Data Retention



Data Retention Characteristics

V63C64L, T_A = 0°C to 70°C, V_{LC} = 0.2V, V_{HC} = V_{DD} -0.2V

Symbol	Parameter	Test Conditions	Min.	Typ. (1)		Max.		Unit
				V_{DD} @ 2.0V	V_{DD} @ 3.0V	V_{DD} @ 2.0V	V_{DD} @ 3.0V	
V_{DR}	V_{DD} for Data Retention	—	2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	1. $\overline{CE}_1 \geq V_{HC}$, $CE_2 \geq V_{HC}$ 2. $CE_2 \leq V_{LC}$	—	10	15	60	90	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(10)	—	—	—	—	ns
$\|I_{LI}\|$ (11)	Input Leakage Current		—	—	—	2	2	µA

NOTES:

(1) Test Conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, Input pulse levels of 0 to 3.0V and output loading specified in Figure 2.

(2) t_{OHZ}, t_{CHZ} and t_{WHZ} are tested with the load in Figure 3. Transition is measured ±500 mV from steady state voltage.

(3) At any given temperature and voltage conditions t_{CHZ} is less than t_{CLZ} for all devices. These parameters are sampled and not 100% tested.

(4) The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ low, CE_2 high and $\overline{WE}$ low. All signals must be in their valid state to initiate a Write and any of the three signals can terminate the Write by going false. The Data Input Setup and Hold timing are referenced to the rising edge of the signal that terminates the Write.

(5) $\overline{WE}$ is high for a Read cycle.

(6) The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.

(7) Address is valid prior to or coincident with $\overline{CE}_1$ low and CE_2 high transitions.

(8) I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

(9) $T_A = +25°C$.

(10) t_{RC} = Read Cycle Time.

(11) This parameter is guaranteed but not tested.