256Kx72 Synchronous Pipeline SRAM *Preliminary**

FEATURES

- Fast clock speed: 100, 133, 150, 166 and 200** MHz
- Fast access time: 5.0, 4.0, 3.8, 3.5, 3.1ns
- +3.3V power supply (VDD)
- +2.5V output buffer supply (VDDQ)
- Single-cycle deselect
- Common data inputs and data outputs
- Clock-controlled and registered addresses, data I/Os and control signals
- SNOOZE MODE for reduced-power standby
- Individual BYTE WRITE control and GLOBAL WRITE
- Six chip enables for simple depth expansion and address pipeline
- Internally self-timed WRITE cycle
- Burst control (interleaved or linear burst)
- Packaging:
- 159-bump PBGA package, 14mm x 22mm
- Commercial, industrial, and military temperature ranges
- User configurable as 512K x 36, or 1M x 18
- Upgradable to 512K x 72 SSRAM
  (contact factory for information)

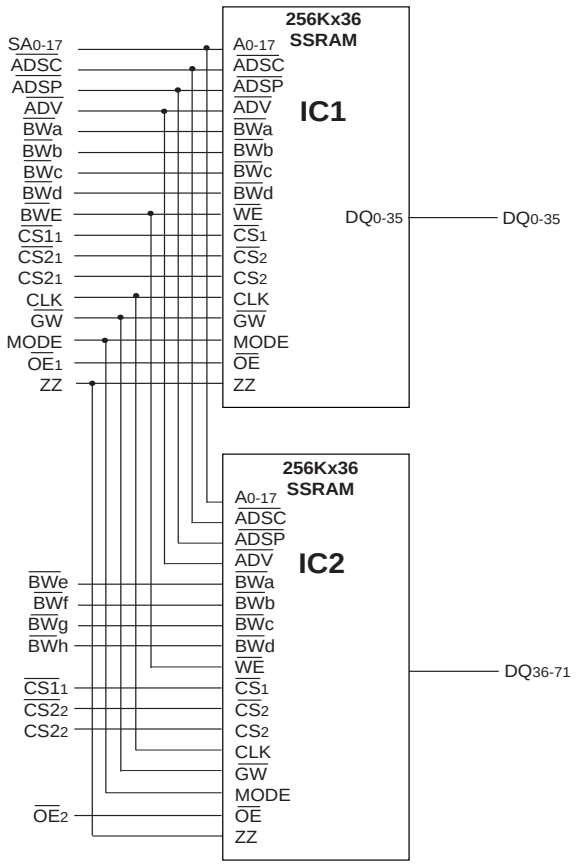
***200 MHz for commercial and industrial temperature only.*

DESCRIPTION

The WEDPY256K72V-XBX employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process. The 16Mb Synchronous SRAMs integrate two 256K x 36 SRAMs into a single PBGA package to provide 256K x 72 configuration. All synchronous inputs are controlled by a positive-edge-triggered single-clock input (CLK). The synchronous inputs include all addresses, all data inputs, and active LOW chip selects ($\overline{CS}$). Asynchronous inputs include the output enable ($\overline{OE1}$/$\overline{OE2}$), clock (CLK).

** This data sheet describes a product that is not fully qualified or characterized and is subject to change without notice.*

FIG. 1 BLOCK DIAGRAM



PIN CONFIGURATION
(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10
A	—	DQ16	DQ14	DQ12	DQ10	ZZ	DQ6	DQ4	DQØ	DQ8
B	$\overline{ADV}$	DQ17	DQ15	DQ11	DQ9	DQ7	DQ5	DQ3	DQ1	SA13
C	$\overline{OE1}$	$\overline{ADSP}$	$\overline{GW}$	DQ13	DNU	GND	DQ29	DQ2	SA12	SA10
D	$\overline{CS2_1}$	CLK	$\overline{BWa}$	GND	GND	VDD	VDDQ	SA11	SA9	SA6
E	$\overline{BW_c}$	$\overline{BWb}$	$\overline{BWd}$	GND	VDD	GND	GND	SA8	SA7	SAØ
F	$CS2_1$	DQ18	DQ22	VDD	VDDQ	GND	VDD	DQ30	DQ34	SA1
G	$\overline{CS1_1}$	DQ19	DQ23	GND	VDD	VDDQ	GND	DQ31	DQ33	SA5
H	DQ26	DQ20	DQ24	VDDQ	VDDQ	VDD	VDD	DQ28	DQ32	DQ35
J	SA17	DQ21	DQ25	VDD	VDD	VDDQ	VDDQ	DQ27	DQ39	DQ37
K	SA16	DQ52	DQ49	GND	VDDQ	VDD	GND	DQ40	DQ38	DQ36
L	SA14	DQ51	DQ50	VDD	GND	VDDQ	VDD	DQ42	DQ41	DQ44
M	SA15	DQ53	DQ48	GND	GND	VDD	GND	DQ43	SA3	DNU
N	$\overline{OE2}$	$\overline{ADSC}$	DQ47	VDDQ	VDD	GND	GND	MODE	SA2	SA4
P	$\overline{BWE}$	$\overline{CS2_2}$	DQ46	DQ45	GND	DNU	DQ59	DQ64	DQ66	DQ70
R	$\overline{BWh}$	$\overline{BWg}$	$\overline{BWf}$	$\overline{BWe}$	DQ56	DQ60	DQ61	DQ65	DQ69	DQ71
T	$\overline{CS1_2}$	$CS2_2$	DQ62	DQ54	DQ55	DQ57	DQ58	DQ63	DQ67	DQ68

DNU = DO NOT USE. Reserved for future upgrades.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x36)

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte "a"	H	L	L	H	H	H
WRITE All Bytes	H	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

NOTE:
1. Using $\overline{BWE}$ and $\overline{BWa}$ through $\overline{BWd}$, any one or more bytes may be written.
2. Insert $\overline{BWe}$ through $\overline{BWh}$ for DQ36-71 control.

TRUTH TABLE

Operation	Address Used	CS1	CS2	CS2	ZZ	ADSP	ADSC	ADV	WRITE	OE	CLK	DQ
Deselected Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	HIGH Z
Deselected Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	HIGH Z
Deselected Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	HIGH Z
Deselected Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	HIGH Z
Deselected Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	HIGH Z
SNOOZE MODE, Power-Down	None	X	X	X	H	X	X	X	X	X	X	HIGH Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	HIGH Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	HIGH Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	HIGH Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	HIGH Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	HIGH Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	HIGH Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. *X means "Don't Care." $\overline{}$ means active LOW. H means logic HIGH. L means logic LOW.*
2. *For $\overline{\text{WRITE}}$, L means any one or more byte write enable signals ($\overline{\text{BWa}}$, $\overline{\text{BWb}}$, $\overline{\text{BWc}}$, or $\overline{\text{WE}}$) are LOW or $\overline{\text{GW}}$ is LOW. $\overline{\text{WRITE}}$ = H for all $\overline{\text{BWx}}$, $\overline{\text{BWE}}$, $\overline{\text{GW}}$ High.*
3. *BWa enables WRITEs to DQ0-8. $\overline{\text{BWb}}$ enables WRITEs to DQ9-17. BWc enables WRITEs to DQ18-26. $\overline{\text{BWd}}$ enables WRITE to DQ27-35.*
4. *All inputs excepts $\overline{\text{OE}}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.*
5. *Wait states are inserted by suspending bursts.*
6. *For a WRITE operation following a READ operation, $\overline{\text{OE}}$ must be HIGH before the input data setup time and held HIGH throughout the input data hold time.*
7. *This device contains circuitry that will ensure the outputs will be held in High-Z during power-up.*
8. *$\overline{\text{ADSP}}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{\text{BWE}}$ LOW or $\overline{\text{GW}}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.*

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply relative to V_{SS}	-0.5V to +4.6V
Voltage on V_{DDQ} Supply relative to V_{SS}	-0.5V to +4.6V
VIN (DQx)	-0.5V to V_{DDQ} +0.5V
VIN (Inputs)	-0.5V to V_{DD} +0.5V
Storage Temperature (BGA)	-55°C to +150°C
Short Circuit Output Current	100 mA

**Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

-55°C ≤ TA ≤ +125°C

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V_{IH}	Inputs	1.7	V_{DD} +0.3	V	1
	V_{IHQ}	Data (DQ)	1.7	V_{DDQ} +0.3	V	1
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.7	V	1
Input Leakage Current	I_{LI}	$0V \leq V_{IN} \leq V_{DD}$	-2.0	2.0	µA	2
Ouptut Leakage Current	I_{LO}	Outputs disabled, $0V \leq V_{IN} \leq V_{DDQ}$ (DQx)	-1.0	1.0	µA	
Output High Voltage	V_{OH}	I_{OH} = -1.0mA	2.0	—	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1.0mA	—	0.4	V	1
Supply Voltage	V_{DD}		3.135	3.6	V	1
Output Buffer Supply	V_{DDQ}		2.375	2.9	V	1

NOTES:

1. All voltages referenced to Vss (GND).

DC CHARACTERISTICS

-55°C ≤ TA ≤ +125°C

Description		Conditions	100 MHz	133 MHz	150 MHz	160 MHz	200 MHz	Units	Notes
Power Supply Current: Operating	IDD	Device selected; All inputs ≤ VIL or ≥ VIH; Cycle time ≥ tKC MIN; VDD = MAX; Outputs open	600	750	950	950	1050	mA	1.2
CMOS Standby	ISB2	Device deselected; VDD = MAX; All inputs ≤ Vss + 0.2	20	20	20	20	20	mA	2
Clock Running	ISB4	Device deselected; VDD = MAX; All inputs ≤ Vss + 0.2 or ≥ VDD -0.2; Cycle time ≥ tKC MIN; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{GW}$, $\overline{BW}$x, $\overline{ADV}$, ≥ VIH	170	180	220	220	240	mA	2

NOTES:

1. IDD is specified with no output current and increases with faster cycle times. IDD increases with faster cycle times and greater output loading.

2. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).

BGA CAPACITANCE

(T_A = +25°C, F = 1MHz)

Description	Symbol	Max	Units	Notes
Control Input Capacitance	C_I	6	pF	1
Common Control Input Capacitance (2)	C_{IC}	15	pF	1
Input/Output Capacitance (DQ)	C_O	10	pF	1
Address Capacitance (SA)	C_{SA}	15	pF	1
Clock Capacitance (CLK)	C_{CK}	12	pF	1

NOTES:

1. This parameter is guaranteed by design but not tested.

2. Common Inputs = zz, $\overline{ADV}$, $\overline{ADSP}$, $\overline{GW}$, $\overline{ADSC}$, $\overline{MODE}$, $\overline{BWE}$

BGA THERMAL RESISTANCE

Description	Symbol	Max	Units	Notes
Junction to Ambient (No Airflow)	Theta JA	30.5	°C/W	1
Junction to Ball	Theta JB	17.3	°C/W	1
Junction to Case (Top)	Theta JC	9.8	°C/W	1

NOTE 1: Refer to BGA Thermal Resistance Correlation application note at www.whiteedc.com in the application notes section for modeling conditions.

AC CHARACTERISTICS
-55°C ≤ TA ≤ +125°C

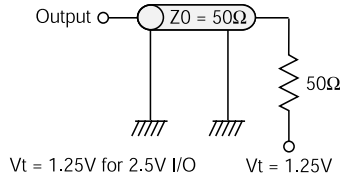
	Symbol	100MHz		133MHz		150MHz		166MHz		200MHz*		
Parameter		**Min.**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock												
Clock Cycle Time	tkc	10		7.5		7.0		6.0		5.0		ns
Clock Frequency	tkf		100		133		150		166		200	MHz
Clock HIGH Time (6)	tkh	3.0		2.5		2.5		2.3		2.0		ns
Clock LOW Time (6)	tkl	3.0		2.5		2.5		2.3		2.0		ns
Output Times												
Clock to output valid	tkq		5.0		4.0		3.8		3.5		3.1	ns
Clock to output invalid (2)	tkqx	1.5		1.5		1.5		15		1.0		ns
Clock to output on Low-Z (2,3,4)	tkqlz	1.5		0		0		0		0		ns
Clock to output in High-Z (2,3,4)	tkqhz		5.0		4.2		4.0		3.5		3.1	ns
$\overline{OE}$ to output valid (5)	toeq		5.0		4.2		4.0		3.5		3.1	ns
$\overline{OE}$ to output in Low-Z (2,3,4)	toelz	0		0		0		0		0		ns
$\overline{OE}$ to output in High Z (2,3,4)	toehz		4.5		4.2		4.0		3.5		3.0	ns
Setup Time												
Address (6,7)	tas	2.0		1.5		1.5		1.5		1.5		ns
Write Enable ($\overline{WE}$) (7)	tws	2.0		1.5		1.5		1.5		1.5		ns
Address status, ($\overline{ADSC}$, $\overline{ADSP}$) (7)	tadss	2.0		1.5		1.5		1.5		1.5		ns
Address advance ($\overline{ADV}$) (7)	taas	2.0		1.5		1.5		1.5		1.5		ns
Data-in (6,7)	tds	2.0		1.5		1.5		1.5		1.5		ns
Chip enable ($\overline{CE}$) (7)	tces	2.0		1.5		1.5		1.5		1.5		ns
Hold Times												
Address (7) (7)	tah	0.5		0.5		0.5		0.5		0.5		ns
Address status ($\overline{ADSC}$, $\overline{ADSP}$) (7)	tadsh	0.5		0.5		0.5		0.5		0.5		ns
Address advance ($\overline{ADV}$) (7)	taah	0.5		0.5		0.5		0.5		0.5		ns
Write Enable (WE) (7)	twh	0.5		0.5		0.5		0.5		0.5		ns
Data-in (6,7)	tdh	0.5		0.5		0.5		0.5		0.5		ns
Chip Enable (CS) (7)	tceh	0.5		0.5		0.5		0.5		0.5		ns

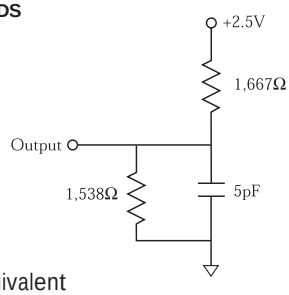
** Commercial and industrial temperatures only.*

NOTES:

1. Test conditions as specified with the output loading as shown in test conditions unless otherwise noted.
2. This parameter is measured with output load as shown in test conditions.
3. This parameter is not tested.
4. Transition is measured ±500mV from steady state voltage.
5. $\overline{OE}$ is a "Don't Care" when a byte write enable is sampled LOW.
6. Measured at HIGH above VIH and LOW below VIL
7. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK to remain enabled.

OUTPUT LOADS





AC Output Load Equivalent

AC TEST CONDITIONS

Parameter	2.5V I/O	Unit
Input Pulse Levels	Vss to 2.5	V
Input Rise and Fall Times	1	ns
Input Timing Reference Levels	1.25	V
Output Timing Reference Levels	1.25	V
Output Load	See figures, at left	

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to ISB2Z. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and a ignored.

ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, ISB2Z is guaranteed after the setup time tzz is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

Description	Conditions	Symbol	Min	Max	Units	Notes
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		20	mA	
ZZ active to input ignored		tZZ		2 (tKC)	ns	1
ZZ inactive to input sampled		tRZZ	2(tKC)		ns	1
ZZ active to snooze current		tZZI		2 (tKC)	ns	1
ZZ inactive to exit snooze current		tRZZI	0		ns	1

NOTES:

1. This parameter is sampled.

SNOOZE MODE WAVEFORM

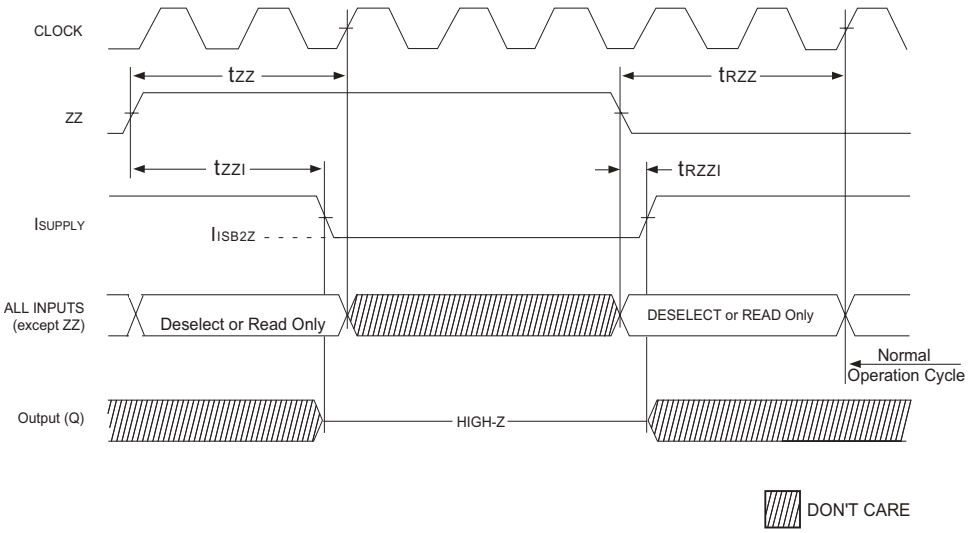
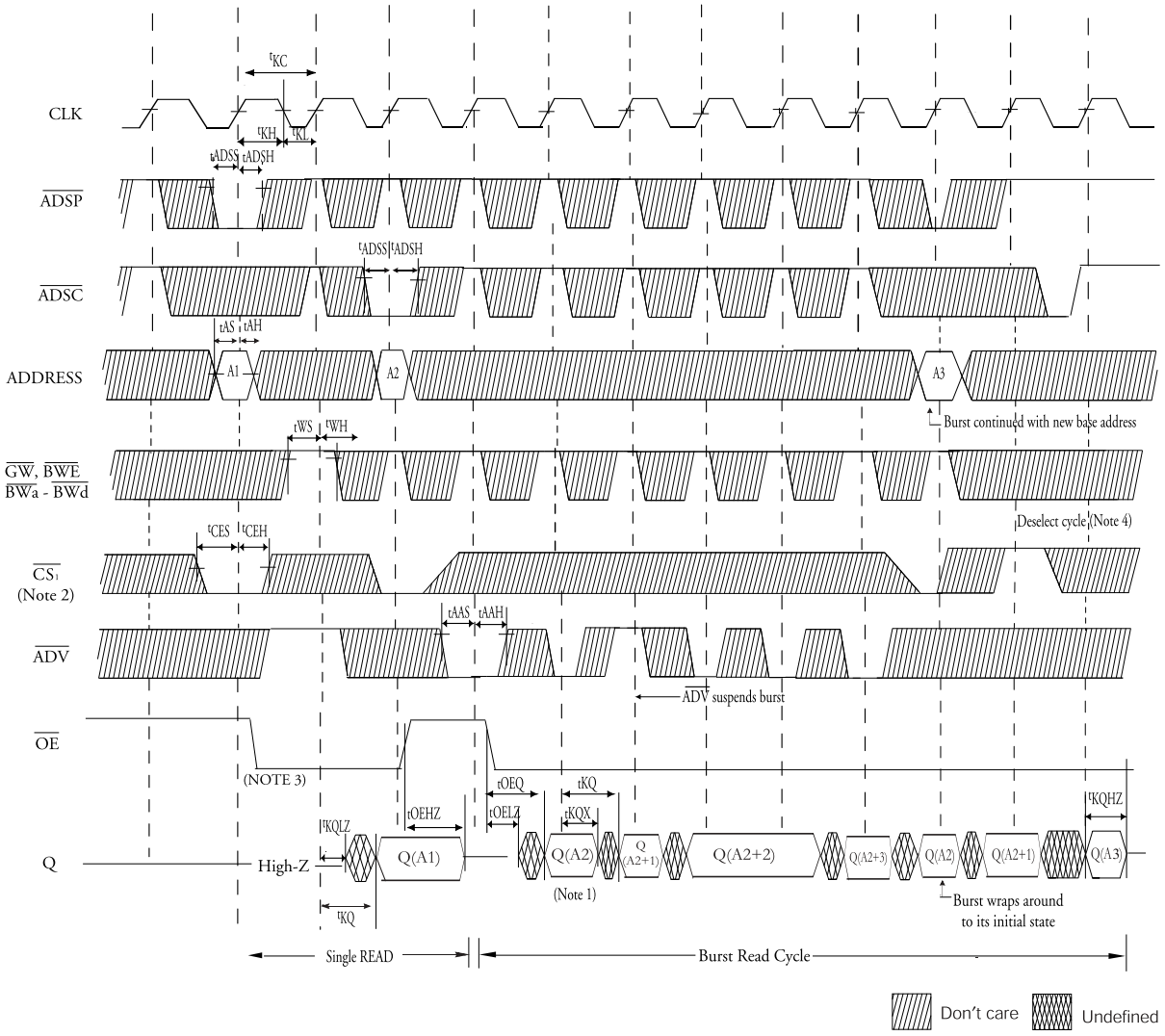


FIG. 2: READ TIMING[3]



NOTES:

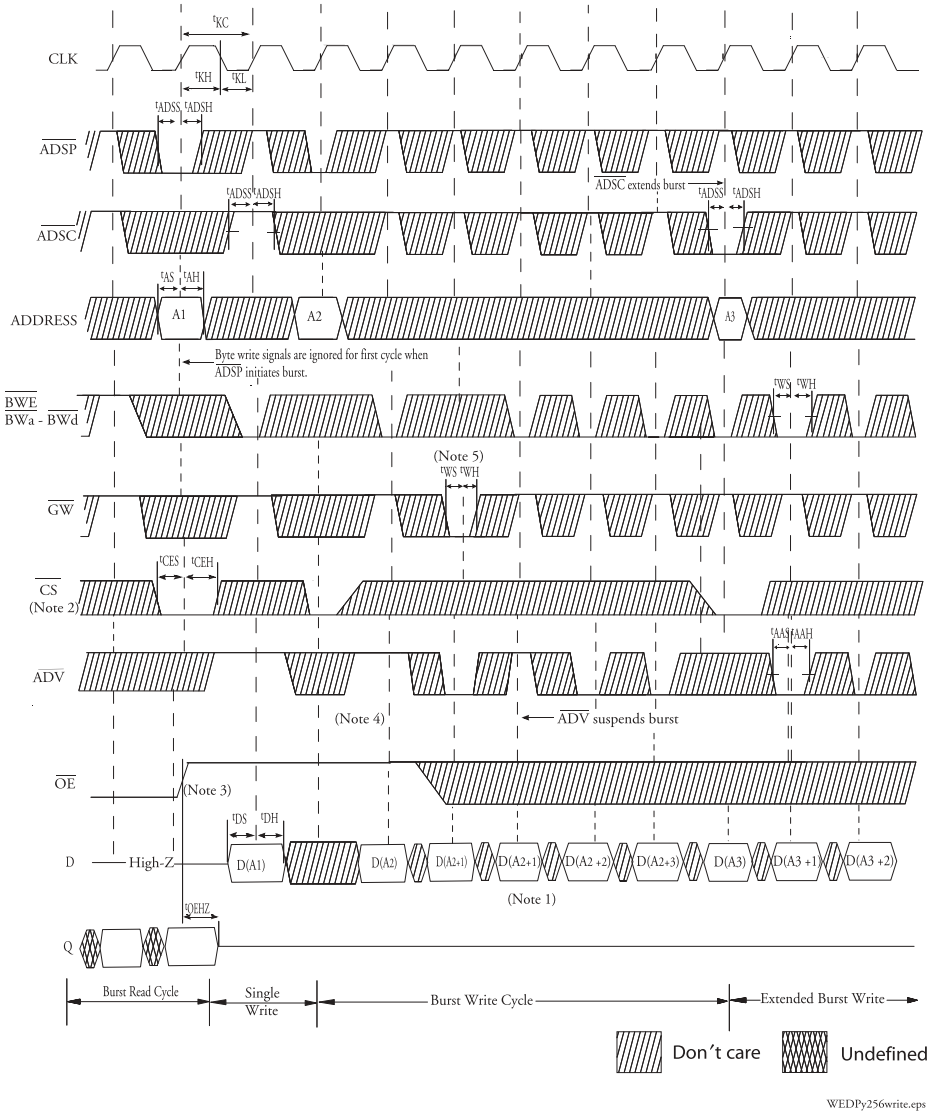
1. DQ (A2) refers to output from address A2. DQ (A2 + 1) refers to output from the next internal burst address following A2.

2. $\overline{CS2}$ and $\overline{CS2}$ have timing identical to $\overline{CS1}$. On this diagram. When CS1 is LOW, $\overline{CS2}$ is LOW and $\overline{CS2}$ is HIGH. When $\overline{CS1}$ is HIGH, $\overline{CS2}$ is HIGH and CS2 is LOW.

3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

4. Outputs are disabled within two clock cycles after deselect.

FIG. 3: WRITE TIMING



NOTES:

1. D(A2) refers to input for address A2. D(A2 +1) refers to input for the next internal burst address following A2.

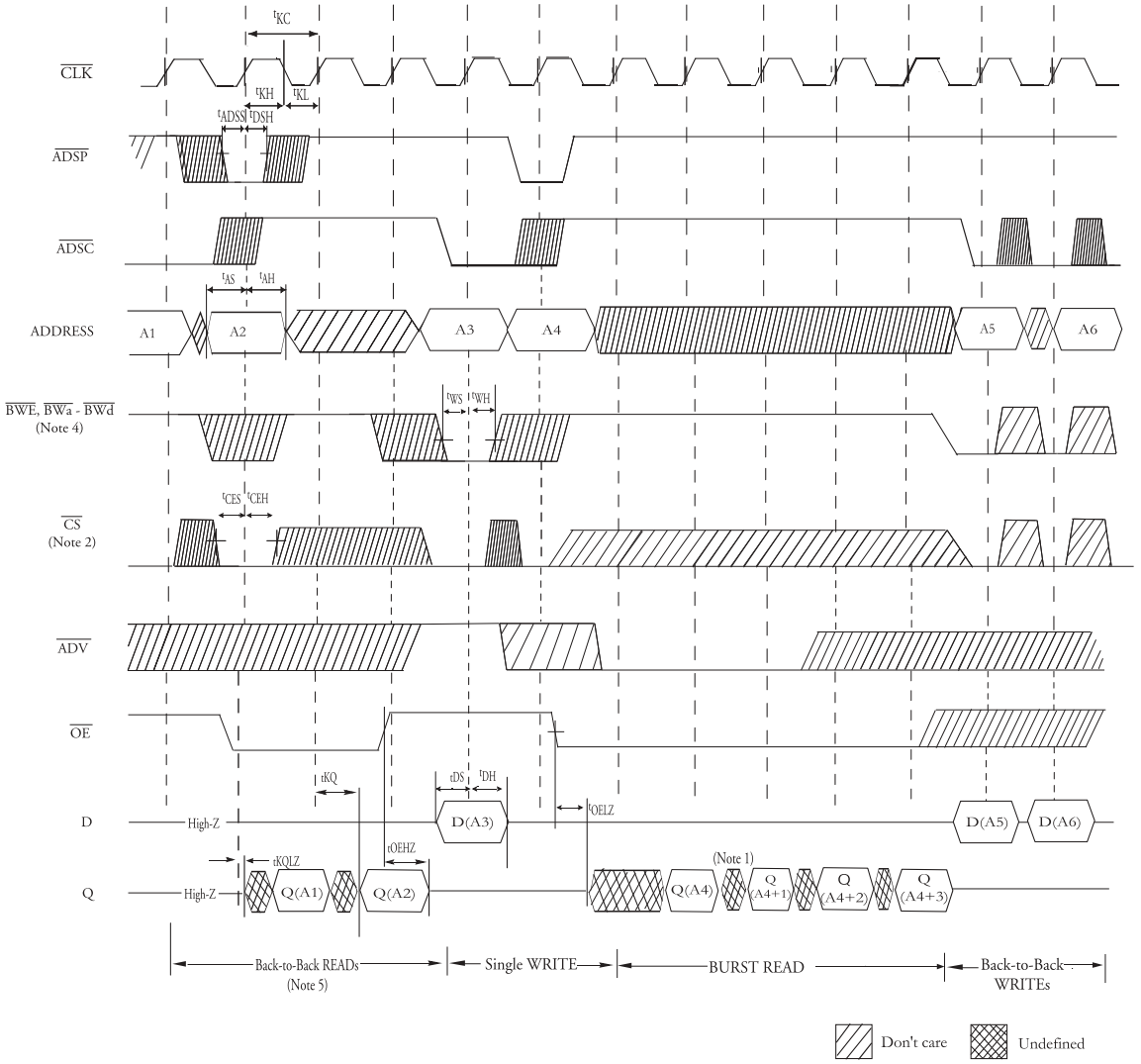
2. $\overline{CS2}$ and CS2 have timing identical to $\overline{CS1}$. On this diagram, when $\overline{CS1}$ is LOW, $\overline{CS2}$ is LOW and $\overline{CS2}$ is HIGH. When $\overline{CS1}$ is HIGH, CS2 is HIGH and CS2 is LOW.

3. $\overline{OE}$ msut be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contentinon for th etime period prior to the byte write enable inputs being sampled.

4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

5. Full-width WRITE can be initiated by $\overline{GW}$ LOW; or $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BWa}$-$\overline{BWd}$ LOW.

FIG. 5: READ/WRITE TIMING[3]



NOTES:

1. Q(A4) refers to output from addrss A4. Q(A4 + 1) refers to output from the next internal burst address to following A4.

2. $\overline{CS2}$ and CS2 have timing identical to $\overline{CS1}$. On this diagram, when $\overline{CS1}$ is LOW, $\overline{CS2}$ is LOW and $\overline{CS2}$ is HIGH. When $\overline{CS1}$ is HIGH, CS2 is HIGH and CS2 is LOW.

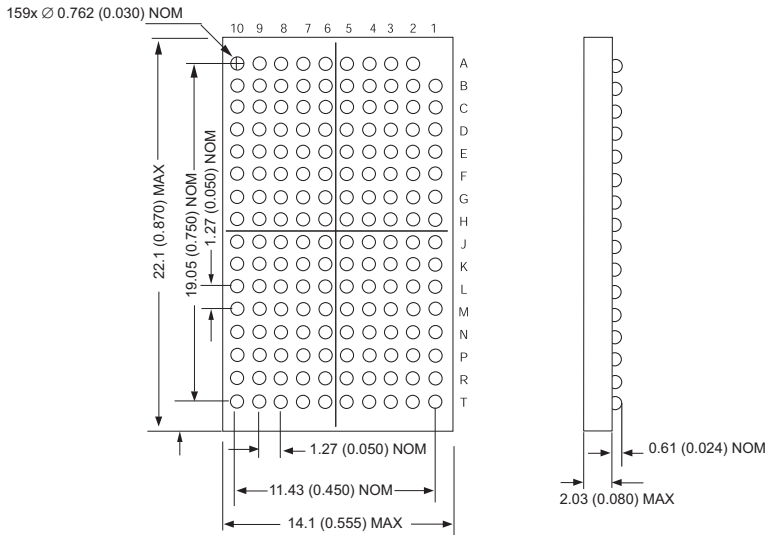
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$, or $\overline{ADV}$ cycle is performed.

4. $\overline{GW}$ is HIGH.

5. Back-to back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.

PACKAGE DIMENSION: 159 BUMP PBGA

BOTTOM VIEW



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WED P Y 256K72 V - X B X

DEVICE GRADE:

M	= Military	-55°C to +125°C
I	= Industrial	-40°C to +85°C
C	= Commercial	0°C to +70°C

PACKAGE:

B = 159 Plastic Ball Grid Array (PBGA)

FREQUENCY (MHz)

100 = 100MHz
133 = 133MHz
150 = 150MHz
166 = 166MHz
200 = 200MHZ

3.3V Power Supply

CONFIGURATION, 256k x 72

SSRAM, Pipeline Burst

PLASTIC

WHITE ELECTRONIC DESIGNS CORP.

Document Title

256K x 72 Synchronous SRAM

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	July 2001	Advanced
Rev 1	Changes (Pg. 1, 5) 1.1 Add speed grades (100MHz-200MHz) to DC Characteristics Table		
Rev 2	Change (Pg. 1) 1.1 Change product status from Advanced to Preliminary.	January 2002	Preliminary
Rev 3	Change (Pg. 1, 11) 1.1 Change Package Dimension title from Top View to Bottom View	September 2002	Preliminary
Rev 4	Changes (Pg. 1, 5) 1.1 BGA Capacitance: Change C_I from 10pF to 6pF 1.2 Change C_{IP} to C_{IC}, capacitance from 20pF to 15pF 1.3 Change C_{CK} from 20pF to 12pF 1.4 Change C_O from 12pF to 10pF 1.5 Change C_{SA} from 20pF to 15pF 1.6 Add Note 2: Control Inputs = zz, ADV#, ADSP#, GW#, ADSC#, MODE#, BWE#.	November 2002	Preliminary
Rev 5	Changes (Pg. 1, 5, 7, 12) 1.1 Add Thermal Resistance Table 1.2 Correct formatting on page 7	May 2003	Preliminary
Rev 6	Changes (Pg. 1, 11, 12) 1.1 Change mechanical drawing to new style	November 2003	Preliminary