



Description

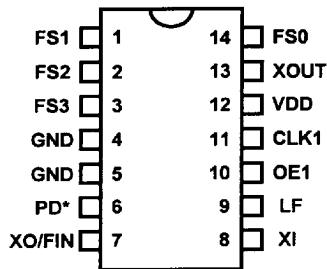


Figure 2: CH9008D

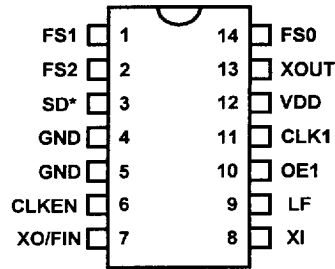


Figure 3: CH9008E

Table 1 • Pin Description CH9008D

Pin	Type	Symbol	Description
1, 2, 3, 14	In	FS1, FS2, FS3, FS0	Frequency select for CLK1 (internal pull-up)
4, 5	Power	GND	Ground
6	In	PD*	Power down input (active low, internal pull-up)
7	Out / In	XO / FIN	Crystal output or external FREF input
8	In	XI	Crystal input
9	In	LF	External loop filter
10	In	OE1	CLK1 output enable (active high, internal pull-up)
11	Out	CLK1	Clock1 output
12	Power	VDD	5V or 3.3V supply
13	Out	XOUT	Buffered reference (14.318 MHz) clock output

Table 2 • Pin Description CH9008E

Pin	Type	Symbol	Description
1, 2, 14	In	FS1, FS2, FS0	Frequency select for CLK1 (internal pull-up)
3	In	SD*	Slow down input (active low, internal pull-up)
4, 5	Power	GND	Ground
6	In	CLKEN	Clock enable input (active high, internal pull-up)
7	Out / In	XO / FIN	Crystal output or external FREF input
8	In	XI	Crystal input
9	In	LF	External loop filter
10	In	OE1	CLK1 output enable (active high, internal pull-up)
11	Out	CLK1	Clock1 output
12	Power	VDD	5V or 3.3V supply
13	Out	XOUT	Buffered reference (14.318 MHz) clock output

Table 3 • Frequencies for CH9008D and E (in MHz)

Frequency Select				Version D	Version E	
3	2	1	0	CLK1	CLK1	Slow Freq
0	0	0	0	16.0	25.0	8.0
0	0	0	1	40.0	33.33	8.0
0	0	1	0	50.0	40.0	8.0
0	0	1	1	80.0	50.0	16.0
0	1	0	0	66.6	66.6	16.0
0	1	0	1	100.0	60.0	16.0
0	1	1	0	8.0	80.0	16.0
0	1	1	1	4.0	50.0	8.0
1	0	0	0	8.0		
1	0	0	1	20.0		
1	0	1	0	25.0		
1	0	1	1	40.0		
1	1	0	0	33.3		
1	1	0	1	50.0		
1	1	1	0	4.0		
1	1	1	1	2.0		
Number of pins				14	14	
Power down option				Yes	No	
Clock enable				No	Yes	
Glitch-free transitions				Yes	Yes	
Slow down option				No	Yes	
Slow down frequency				N/A	See above	
Internal pull-up				Yes	Yes	

Note: Please consult Chronitel for custom frequency patterns

Table 4 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	-0.5 TO +7.0	V
VIN	Input voltage on any pin with respect to GND	-0.5 TO VDD+0.5	V
TSTOR	Storage temperature	-55 TO +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5 • DC Specifications (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 1mA	2.5			V
VOL	Output low voltage	VDD = 4.75V, IOL = 2mA			0.5	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			3	10	μA
ILK	Input leakage current		-10		10	μA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IPD	Power down supply current	PD* = Low		3		μA
ISD	Slow down supply current	SD* = Low, VDD = 5V, No load		3		mA
IDD	Operating current	VDD = 5V CLK1 = 40 MHz, No load CLK1 = 80 MHz, No load		10 20		mA

Table 6 • AC Specifications (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	20	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	15 pF load, VOUT = 0.8V to 2.0V			3	ns
TF	Output clock fall time	15 pF load, VOUT = 0.8V to 2.0V			3	ns
TDC	Duty cycle	15 pF load	45	48/52	55	%
TJCC	Jitter, cycle to cycle	CLK1 = 50 MHz		50	100	ps
TJLT	Jitter, long term (10,000 cycles)	CLK1 = 50 MHz		200	1000	ps
TFT	Frequency transition time	8 – 80 MHz without 1 nF LF cap		2		ms
		8 – 80 MHz with 1 nF LF cap		10		ms
TPU	Power up time	From OFF to 100 MHz without 1 nF LF cap		3		ms
		From OFF to 100 MHz with 1 nF LF cap		15		ms

Table 7 • DC Specifications (Operating Conditions: $T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Description	Test Condition @ $T_A = 25^{\circ}\text{C}$	Min	Typ	Max	Unit
V_{OH}	Output high voltage	$V_{DD} = 3.0\text{V}$, $I_{OH} = 1\text{mA}$	$V_{DD} - 0.5$			V
V_{OL}	Output low voltage	$V_{DD} = 3.0\text{V}$, $I_{OL} = 2\text{mA}$			0.5	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			3	10	μA
I_{LK}	Input leakage current		-10		10	μA
C_I	Input capacitance	Except XO / FIN, XI			10	pF
C_I	Input capacitance	Pins XO / FIN, XI		20		pF
I_{PD}	Power down supply current	$PD^* = \text{Low}$		3		μA
I_{SD}	Slow down supply current	$SD^* = \text{Low}$, $V_{DD} = 3.3\text{V}$, No load		3		mA
I_{DD}	Operating current	$V_{DD} = 3.3\text{V}$ CLK1 = 40 MHz, No load CLK1 = 80 MHz, No load		5 10		mA

Table 8 • AC Specifications (Operating Conditions: $T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Description	Test Condition @ $T_A = 25^{\circ}\text{C}$	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	20	MHz
T_{IR}	Input clock rise time				20	ns
T_{IF}	Input clock fall time				20	ns
T_R	Output clock rise time	15 pF load, $V_{OUT} = 0.8\text{V}$ to 2.0V			3	ns
T_F	Output clock fall time	15 pF load, $V_{OUT} = 0.8\text{V}$ to 2.0V			3	ns
TDC	Duty cycle	15 pF load	45	48/52	55	%
T_{JCC}	Jitter, cycle to cycle	CLK1 = 50 MHz		50	100	ps
T_{JLT}	Jitter, long term (10,000 cycles)	CLK1 = 50 MHz		200	1000	ps
T_{FT}	Frequency transition time	8 – 80 MHz without 1 nF LF cap		2		ms
		8 – 80 MHz with 1 nF LF cap		10		ms
TPU	Power up time	From OFF to 100 MHz without 1 nF LF cap		3		ms
		From OFF to 100 MHz with 1 nF LF cap		15		ms

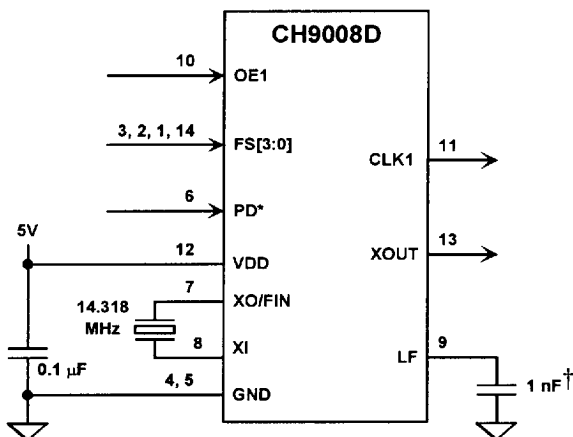


Figure 4: Application Schematic

Note: For other versions, please refer to pin descriptions for exact pin numbers and functions

† Typically a 1 nF capacitor, but may vary depending on application

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9008x-N	300 mil PDIP	14	5V
CH9008x-S	150 mil SOIC	14	5V
CH9008x-N-L	300 mil PDIP	14	3.3V
CH9008x-S-L	150 mil SOIC	14	3.3V
Note: x = frequency table version			