Data Sheet
June 1995

AT&T Microelectronics

DSP32C Digital Signal Processor with External Memory Interface

Introduction

AT&T is an industry leader in floating-point digital signal processing. AT&T's DSP32 architecture was introduced in 1985 and is now the accepted standard in the speech, signal processing, and telecommunications application areas.

The DSP32C device offers more than three times the throughput of the DSP32 while offering pin, source code, and object code upward compatibility. In addition to powerful DSP devices, AT&T offers application support to its customers. Application support is supplied by field engineers, application notes, application software, and a 24-hour bulletin board.

Software and hardware development tools are available from both AT&T and third parties to speed development schedules. These tools include a device software simulator, hardware development board, and in-circuit emulator. The DSP32C product family offers high processing power, ease of use, and excellent development support.

Description

The AT&T DSP32C Digital Signal Processor is a 32-bit, floating-point, programmable integrated circuit. As the second generation to the DSP32, it has access to a large base of both software and hardware support.

The DSP32C is fabricated in AT&T's high-speed, low-power CMOS technology. Packaging options for the DSP32C with External Memory Interface include a standard 133-pin, square ceramic pin-grid-array (CPGA) package and a 164-pin, JEDEC standard bumpered quad flat pack (BQFP) package.

Two execution units, the control arithmetic unit (CAU) and the data arithmetic unit (DAU), operate in parallel to achieve high throughput. The CAU performs 16- or 24-bit fixed-point arithmetic for logic and control functions. This unit, which includes 22 general-purpose registers, can execute 20 million instructions per second (MIPS). The DAU performs 32-bit floating-point arithmetic for signal processing functions. Four 40-bit accumulators are used as inputs/outputs to a floating-point multiplier and a floating-point adder that work in parallel to perform 40 million floating-point operations per second (MFLOPS).

Table 1. DSP32C Products

Device Code	RAM	Instruction Cycle Time	External Memory Interface	Package
DSP32C-R35	3 - 0.5K x 32	80 ns, 60 ns, or 50 ns	Yes	133 CPGA
DSP32C-F35	3 - 0.5K x 32	80 ns, 60 ns, or 50 ns	Yes	164 BQFP
DSP32C-M4*	4 - 0.5K x 32	80 ns, 70 ns	No	68 PLCC

* This version of the DSP32C is described in the *AT&T DSP32C Without External Memory Interface* Data Sheet.

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Description (continued)

Table 2. Features and Benefits of the DSP32C

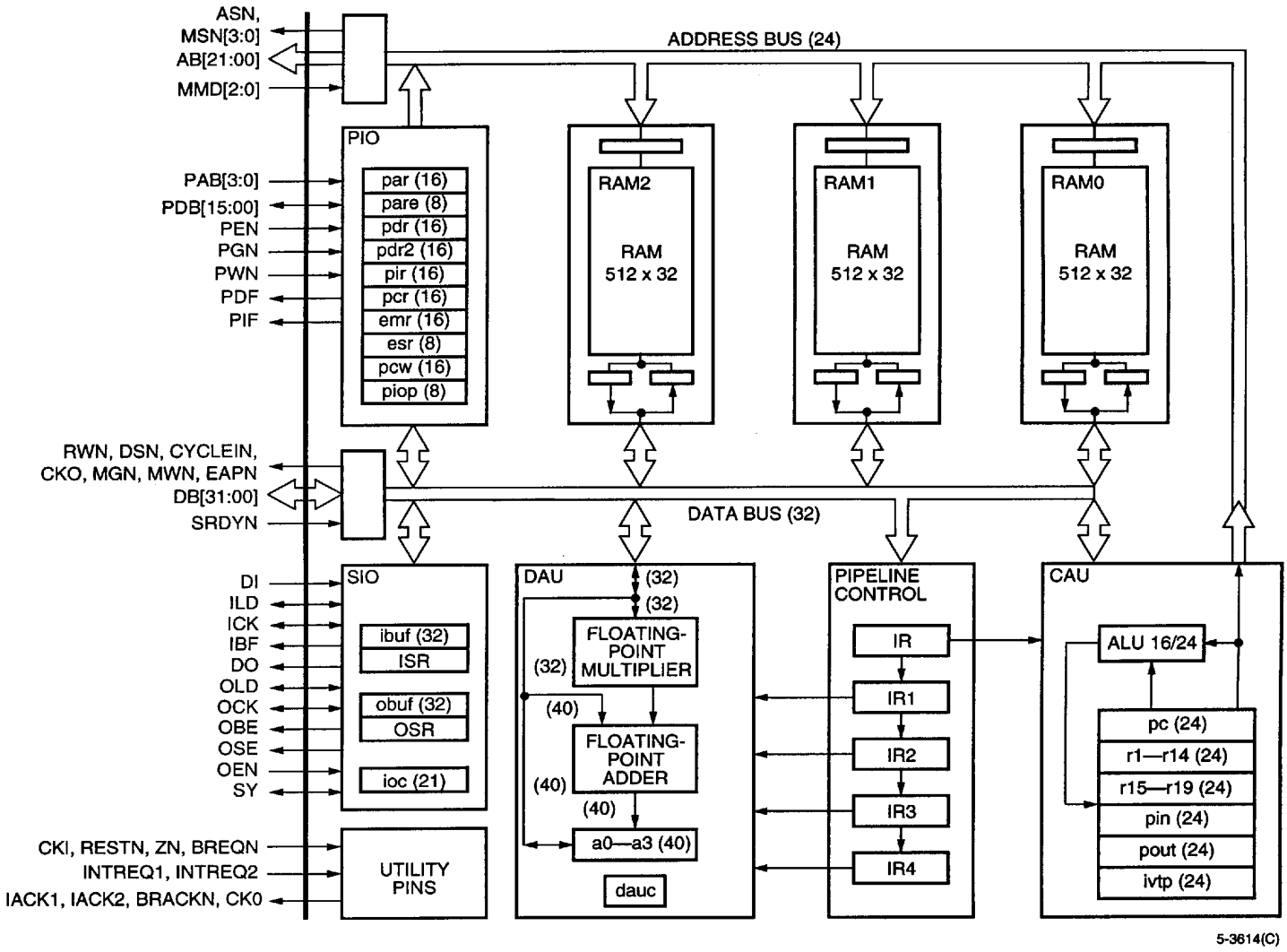
Features	Benefits
Full 32-bit floating-point architecture Increased precision & dynamic range	Simplifies program development to provide faster time to market Much easier algorithm development opens up new application possibilities
Instruction started every instruction cycle	Allows more complex functions or a greater number of simultaneous functions to be implemented
Four memory accesses per instruction cycle Exceptional memory bandwidth	Eliminates memory accessing bottlenecks
C-like assembly language	Easy to learn/excellent readability
Serial and parallel ports with DMA High bandwidth, nonintrusive I/O	Clean interface to external devices Lower system cost Easy interface to PC buses External control via parallel I/O (PIO)
Hardware data format conversions — *IEEE** P754 floating-point — Integer conversions: 8-bit unsigned 16-bit linear 24-bit linear — μ-law/A-law conversions	Eliminates lengthy software routines Permits shared data with host processor or other platforms Increased throughput in: — Graphics and image processing — Applications with 16-bit data — HQ digital audio and control applications — Telecom and speech applications
Fully vectored interrupt structure with hardware context save	Allows very fast interrupt processing (up to 2 million interrupts/s)
Byte-addressable address space	Efficient storage of 8- and 16-bit data Lower system cost
Flexible wait-state facility — Each wait-state is 1/4 instruction cycle — Two independent external memory speed partitions	Greater memory speed selection flexibility than conventional full-cycle wait-states Allows mixing of slow and fast memory Optimizes system speed/cost requirements

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 3. DSP32C with External Memory Interface Device Speed Options

Minimum Instruction Cycle Time (ns)	Maximum Clock Frequency (MHz)
50	80.000
60	66.666
80	50.000

Description (continued)



LEGEND:					
a0—a3	Accumulators 0—3	**IR1—IR4**	Instruction register pipeline	**pdr**	PIO data register
ALU	Arithmetic logic unit	**ISR**	Input shift register	**pdr2**	PIO data register 2
CAU	Control arithmetic unit	**ivtp**	Interrupt vector table pointer	**pin**	Serial DMA input pointer
DAU	Data arithmetic unit	**obuf**	Output buffer	**PIO**	Parallel I/O unit
dauc	DAU control register	**OSR**	Output shift register	**piop**	Parallel I/O port register
emr	Error mask register	**par**	PIO address register	**pir**	PIO interrupt register
esr	Error source register	**pare**	PIO address register extended	**pout**	Serial DMA output pointer
ibuf	Input buffer	**pc**	Program counter	**r1—r19**	Registers 1—19
ioc	Input/output control register	**pcr**	PIO control register	**RAM**	Read/write memory
IR	Instruction register	**pcw**	Processor control word	**SIO**	Serial I/O unit

Figure 1. Block Diagram of the DSP32C with External Memory Interface

Architecture

The DSP32C architecture is being used today to solve a wide variety of complex problems. A large set of general-purpose registers simplifies assembly-language programming and allows very efficient compiler implementations. Both internal and external memory are treated as a general resource allowing the programmer to freely mix both programs and/or data within the 16 Mbyte address space.

In addition to its powerful number-crunching capabilities and flexible memory organization, the DSP32C offers many features that allow it to be easily and quickly integrated into real world systems.

A block diagram of the DSP32C with External Memory Interface appears in Figure 1. The following subsections describe the components shown in this diagram.

Control Arithmetic Unit (CAU)

The CAU generates memory addresses and performs 16- or 24-bit integer arithmetic at the rate of 20 million instructions per second. The CAU consists of a 24-bit arithmetic logic unit (ALU) which performs the integer arithmetic and logical operations, a 24-bit program counter (**pc**) register, and 22 general-purpose 24-bit registers. All 22 registers can be used for operands in the execution of 16- or 24-bit integer operations; however, some of these registers also serve special purposes. When addressing 32-bit floating-point operands, registers **r1**—**r14** are used as memory pointers (**rP**), and **r15**—**r19** are used as increment registers (**rI**). Register **r20**, also called **pin**, is used as the serial DMA input pointer. Register **r21**, also called **pout**, is used as the serial DMA output pointer. Register **r22**, also called interrupt vector table pointer (**ivtp**), is used as the base address for the interrupt vector table.

Data Arithmetic Unit (DAU)

The DAU is configured for multiply/accumulate operations and is the primary execution unit for signal-processing algorithms. The DAU contains a floating-point multiplier and a floating-point adder, and four 40-bit accumulators (**a0**—**a3**). The multiplier and adder work in parallel to perform 20 million instructions per second of the form a = b + c * d. The DAU multiplier operands (c and d) are 32-bit floating-point numbers (an 8-bit exponent and a 24-bit mantissa) from memory or an accumulator. The multiplier always provides one 40-bit input to the adder. The other input can originate from memory, the I/O ports, or an accumulator. The operands for this second adder input can be 8-, 16-, 24-, 32-, or 40-bit numbers. The 40-bit operands (8-bit exponent, 24-bit mantissa, and eight mantissa guard bits) come from an accumulator (**a0**—**a3**). The 8-, 16-, and 24-bit operands are used in special function instructions whose purpose is data-type conversion. For either conversions or addition operations, 32-bit operands may come from memory or I/O registers. Available conversions are between the DSP32C floating-point format and the following: 8-, 16-, and 24-bit two's complement integer, μ-law, A-law, and single-precision *IEEE* floating-point format.

Internal and External Memory

The DSP32C provides on-chip RAM and an external memory interface for off-chip ROM and/or RAM expansion. All memory can be addressed as 8-, 16-, 24-, or 32-bit words, with 32-bit data accessed at the same speed as 8-bit data. Instructions, tables, and data can be arbitrarily located in on-chip RAM or external memory. The addresses of the various blocks of memory can be configured in eight different memory modes. Four of the memory modes provide a DSP32-compatible 16-bit address space. The other four memory modes provide a full 24-bit address space. See the Memory Configuration section for more information on configuring the address space. Regardless of the configuration, the first instruction executed after reset is at address 0x000000.

Internally, the DSP32C device has 1,536 words of RAM which are available in all memory configurations. The on-chip RAM is static and does not need to be refreshed.

The external memory interface can directly address up to 16 Mbytes of additional memory. The interface supports wait-states and bus arbitration. The external memory is divided into two sections: a low partition (A) and a high partition (B). The number of wait-states for each partition is independently configurable (see Register Operation, Table 25, **pcw** Register). Therefore, a mix of slow and fast memories can be used to provide the necessary throughput at a reasonable cost.

Architecture (continued)

Serial I/O Unit (SIO)

The serial I/O unit is used for serial-to-parallel conversion of input data and parallel-to-serial conversion of output data. SIO inputs are loaded into the input shift register (ISR) and then into the input buffer (**ibuf**). SIO outputs are loaded into the output buffer (**obuf**) and then into the output shift register (OSR). This double-buffering makes back-to-back transfers possible, allowing the DSP32C program to begin a second transfer before the first has been completed. Data widths can be 8, 16, 24, or 32 bits. The input/output control (**ioc**) register in the SIO is used to select various I/O configurations, bit lengths, internal or external clocks, and internal or external synchronization (see Register Operation, Table 19, **ioc** Register).

Parallel I/O Unit (PIO)

The parallel I/O unit is an on-chip register file and bi-directional data bus that can be used for communication between the DSP32C device and an external device. The external PIO data bus can be 8 or 16 bits wide. PIO data transfers are made under program or DMA control. Using PIO DMA, an external device can download a program or data without interrupting execution of the DSP32C program. The PIO has three 16-bit data registers (**pdr**, **pdr2**, and **pir**), a 24-bit address register (**par/pare**), a 16-bit processor control word (**pcw**), an 8-bit I/O port register (**piop**), a 16-bit control register (**pcr**), a 16-bit error mask register (**emr**), and an 8-bit error source register (**esr**). These registers are used to control PIO transfers and configure error control and interrupt features (see Register Operation).

Memory Configuration

The addresses of the various blocks of memory can be configured in eight different memory modes. Four of the memory modes (0—3) provide a DSP32-compatible, 16-bit address space. The other four memory modes (4—7) provide a full 24-bit address space. Pin MMD2 selects either the DSP32 compatible 16-bit address space or the expanded 24-bit address space. Pins MMD0 and MMD1 select memory modes that determine the location of on-chip memory resources in the memory address space. Figure 2 shows the location of memory resources.

Memory accesses can be made without regard to the type or location of the physical memory; however, to achieve maximum throughput, instruction/data memory accesses of floating-point operations must alternate between physical memories. There are four physical memories: (1) RAM0, (2) RAM1, (3) external memory A and B, and (4) RAM2.

The number of wait-states for the external memory partitions A and B are independently configurable via the MEMA and MEMB fields of the **pcw** register. The number of wait-states may be statically configured or externally controlled. Statically configured waits of 1, 2, or 3 states allow the DSP32C to access memory without delays for handshaking (a state is one period of CKI, or 12.5 ns at maximum clock frequency). When configured for two or more externally controlled wait-states, the DSP32C generates wait-states until the memory acknowledges the transaction via the synchronous ready (SRDYN) handshaking signal.

Architecture (continued)

Memory Configuration (continued)

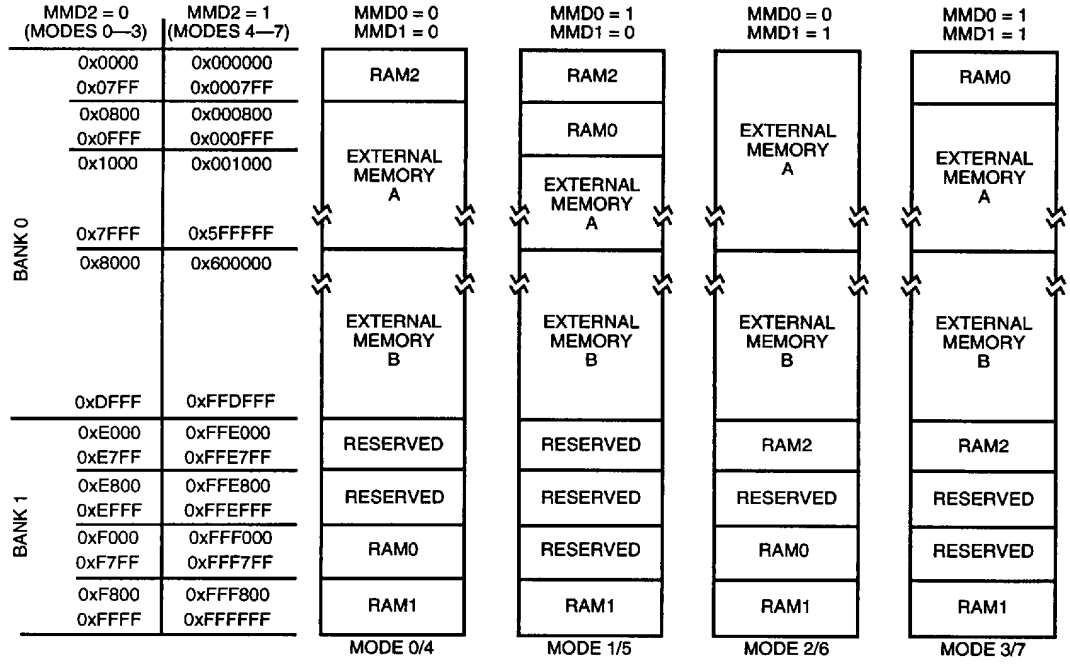


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Figure 2. DSP32C Memory Configurations

Architecture (continued)

Memory Addressing

Each 32-bit word is organized as 4 bytes, e.g., 3, 2, 1, 0, where byte 3 is the most significant byte (MSbyte) and byte 0 is the least significant byte (LSbyte) (see Table 4, Memory Addressing). A 16-bit integer is 2 bytes, either 1, 0 (with byte 1 the MSbyte and byte 0 the LSbyte) or 3, 2 (with byte 3 the MSbyte and byte 2 the LSbyte).

Integer operands of 24 bits are organized as 4 bytes. Byte 2 is the MSbyte, byte 0 is the LSbyte, and byte 3 is a sign extension of byte 2. Integer operands of 24 bits are addressed the same as 32-bit words. Memory address 0 can refer to an 8-bit byte (byte 0), a 16-bit integer (bytes 1, 0), a 24-bit integer (bytes 2, 1, 0), or a 32-bit word (bytes 3, 2, 1, 0).

Table 4. Memory Addressing

32-Bit Word				
	24-Bit Integer			
16-Bit Integer		16-Bit Integer		Memory Address
Byte	Byte	Byte	Byte	
3	2	1	0	0
7	6	5	4	4
11	10	9	8	8
etc.				

The external memory is accessed by a 22-bit external address bus (AB00—AB21) and four byte select lines (MSN0—MSN3) (see Table 5, Data Type Memory Select and Write Data). The bus obtains its data from the 22 most significant bits of the address bus and selects a 32-bit word in memory. The four byte select signals (active-low) select bytes within the 32-bit word (see Pin Information). The value of the byte select lines is determined by the two least significant bits of the address and the data type implied in the instruction. The address is specified either directly or via a register pointer (**pc, r1—r22**). With the maximum external memory attached, one can address a total of 16M bytes, 8M 16-bit integers, 4M 24-bit integers, or 4M 32-bit words.

Table 5. Data Type Memory Select and Write Data

Data Type Memory Select					DSP32C Write Data*			
Data Type	MSN3	MSN2	MSN1	MSN0	24—31	16—23	8—15	0—7
Byte 0	1	1	1	0	A	A	A	A
Byte 1	1	1	0	1	B	B	B	B
Byte 2	1	0	1	1	C	C	C	C
Byte 3	0	1	1	1	D	D	D	D
Low 16-bit	1	1	0	0	B	A	B	A
High 16-bit	0	0	1	1	D	C	D	C
32-bit/24-bit	0	0	0	0	D	C	B	A

* A = write data DB00—DB07; B = write data DB08—DB15; C = write data DB16—DB23; D = write data DB24—DB31.

Architecture (continued)

Interrupt Operation

The DSP32C provides a single-level interrupt facility with six sources (four internal and two external). The interrupts are prioritized and are individually maskable via the INTER field of the **pcw** register. The sources are described below in descending priority:

1. External Interrupt One (INTREQ1) — level sensitive.
2. Parallel Buffer Full (PDF) — generated when the **pdr** register is loaded.
3. Parallel Buffer Empty (PDE) — generated when the **pdr** register is read.
4. SIO Input Buffer Full (IBF) — generated when the IBF flag is set.
5. SIO Output Buffer Empty (OBE) — generated when the OBE flag is set.
6. External Interrupt Two (INTREQ2) — level sensitive.

Before servicing an interrupt, the DSP32C saves the state of the machine that is invisible to the programmer, as well as DAU accumulators **a0—a3** and the **dauc** register. Internal states that are visible to the programmer and need to be saved, except **a0—a3** and the **dauc**, must be saved and restored by the interrupt service routine. In response to a given interrupt, the DSP32C branches to the corresponding address in the interrupt vector table. The interrupt vector table contains six pairs of 32-bit words starting at the location specified in the interrupt vector table pointer register **ivtp** (r22). Each pair of words in the table should contain an unconditional branch to the appropriate interrupt routine. Note that even when masked, the interrupt conditions may be tested in conditional branch instructions (see Instruction Set). Figure 3 is a memory map of the interrupt vector table. To return to the interrupted program, the user should restore the user-visible state of the DSP32C (which was saved), and then execute the **ireturn** instruction. The latter operation restores **a0—a3** and the state of the machine that is not visible to the user.

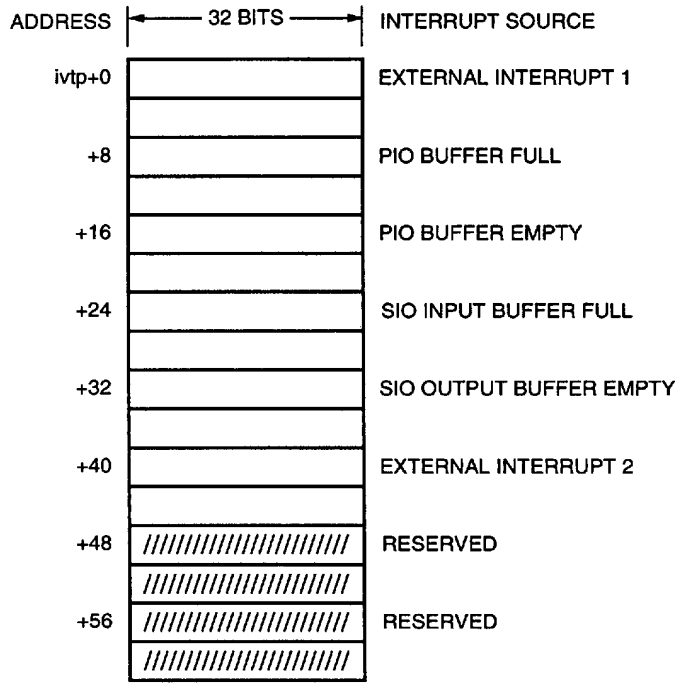


Figure 3. Interrupt Vector Table

Instruction Set

Table 6. Features and Benefits of the DSP32C Instruction Set

Features	Benefits
Instruction started every instruction cycle	Allows more complex or a greater number of applications to be implemented
Full set of microprocessor-like instructions	Expands the number of applications that can be efficiently handled
Conditional branches	Simplifies programming task*
Conditional ALU operations	Permits very fast, efficient coding* Eliminates unnecessary branch instructions
Single-cycle **pc**-relative addressing for position-independent code	Simplifies multitask applications*
Data stationary coding	Enables parallel operation of arithmetic and logical operations Allows efficient compiler implementations* Provides automatic pipeline control* Simplifies program development process*

* Provides faster time to market.

The DSP32C assembly language frees programmers from tedious memorization of assembly-language mnemonics. Instructions in the DSP32C are patterned after the C programming language and are entered in a natural equation syntax. In addition to being easier to learn, the resulting code is far more readable than mnemonic-based assembly languages, making code maintenance much easier.

C-like assembly language → Easy to learn/excellent readability

Assembly-language example (32-bit multiply/ accumulate with store to memory):

```
*r1++ = a0 = a1 + *r2++ * *r3++
```

The execution of this instruction simply follows the conventions of the high-level C programming language:

"Multiply the 32-bit floating-point values stored in the memory locations pointed to by registers **r2** and **r3**. Add the result to the contents of accumulator **a1**, store the result in accumulator **a0**, and write the result to the 32-bit memory location pointed to by register **r1**. Post-increment pointer registers **r1**, **r2**, and **r3**."

The DSP32C has two general types of instructions that correspond to the two execution units: data arithmetic (DA) instructions and control arithmetic (CA) instructions.

Primarily, DA instructions perform 32-bit floating-point multiply/accumulate operations for signal processing algorithms. Other DA instructions convert the DSP32C's internal floating-point data to and from each of the following types: 8-bit, 16-bit, or 24-bit 2's complement integer; μ-law; A-law; or single-precision *IEEE* floating-point.

The CA instructions perform microprocessor operations such as 16-bit and 24-bit integer arithmetic and logic functions, conditional branching, and moving data.

Instruction Set (continued)

Flags

The DSP32C has internal flags that are affected by the results of certain DA, CA, or I/O instructions and certain I/O events. These flags, although not directly visible to the user, may be tested by conditional instructions. Table 7 lists the flags and their meanings.

Table 7. DSP32C Flags

DAU Flags		
Flag	**Meaning (Flag = 1)**	**Description**
N	Result is negative	Sign bit = 1.
Z	Result is zero	All 40 bits of accumulator = 0.
V	Result overflowed*	| DAU result | > 3.40282 E 38.
U	Result underflowed*	| DAU result | < 5.87747 E –39.
CAU Flags		
n	Result is negative	(16-bit) n = b23 (bit 23 of ALU result). (24-bit) n = b23.
z	Result is zero	(16-bit) z = $\overline{b23+b22+\ldots b1+b0}$ (+ = OR). (24-bit) z = $\overline{b23+b22+\ldots b1+b0}$.
c	Carry or borrow out of MSB	(16-bit) c = b15c (carry out of ALU bit 15). (24-bit) c = b23c.
v	Result overflowed	(16-bit) v = b14c ^ b15c (^ = exclusive OR). (24-bit) v = b22c ^ b23c.
I/O Flags		
i	Serial input buffer full	Pin IBF = 1.
o	Serial output buffer full	Pin OBE = 0.
p	Parallel data register full	Pin PDF = 1.
P	Parallel interrupt register full	Pin PIF = 1.
s	SY (I/O sync) set (1)	Pin SY = 1.
b	Serial I/O frame boundary	fbs = 1.
r	Interrupt pin 1 high (1)	Pin INTREQ1 = 1.
R	Interrupt pin 2 high (1)	Pin INTREQ2 = 1.

* The *DSP3207 Digital Signal Processor Information Manual* dated July 1994, Section 3.3.3, contains a detailed description of the floating-point formats and exceptions. The DSP3207 floating-point format and arithmetic is identical to that of the DSP32C.

DSP32C instructions and the flags affected by each instruction are specified in the following tables. A zero (0) shown in place of a flag means that the flag is always made zero; a dash (—) in place of a flag means that the flag is unaffected by the instruction.

The complete DSP32C instruction set, grouped as DA and CA instructions, follows. Where braces, { }, are shown in an instruction, one of the enclosed items must be chosen. Items enclosed in brackets, [ ], are optional.

Note: { } and [ ] are not part of the instruction syntax. Parentheses, ( ), are part of the syntax and must appear where shown in an instruction. Lower-case letters are part of the syntax and upper-case letters are replaced by immediate data or by a register name (see tables following each instruction group).

Instruction Set (continued)

Data Arithmetic (DA) Instructions

The DA instructions are divided into two functional groups: multiply/accumulate and special functions.

Table 8. Data Multiply/Accumulate Instructions

Instruction	DAU Flags Affected	Description
[Z=] aN = [–]aM {+,–} Y*X	NZVU	The product of the **X** and **Y** fields is added to or subtracted from the accumulator **aM** (or its negative), and the result is stored in accumulator **aN**. The result can also be output according to the **Z** field.
aN = [–]aM {+,–} (Z=Y)*X	NZVU	The **Y** field operand is output according to the **Z** field. The product of the **X** and **Y** fields is added to or subtracted from the accumulator **aM** (or its negative), and the sum is stored in accumulator **aN**.
[Z=] aN = [–]Y {+,–} aM*X	NZVU	The product of the **X** field and the accumulator **aM** is added to or subtracted from the **Y** field (or its negative). The result is placed in accumulator **aN** and can also be output according to the **Z** field.
[Z=] aN = [–]Y*X	NZVU	The product of the **X** and **Y** fields is added to or subtracted from zero. The result is stored in accumulator **aN** and can also be output according to the **Z** field.
aN = [–](Z=Y)*X	NZVU	The value of the **Y** field is output according to the **Z** field. The product of the **Y** and **X** fields (or the negative of the product) is stored in accumulator **aN**.
[Z=] aN = [–]Y {+,–}X	NZVU	The sum or difference of the **Y** and **X** fields is stored in accumulator **aN**, and the result can also be output according to the **Z** field. Note that **X** is a multiplier input.
[Z=] aN = [–]Y	NZVU	The value of the **Y** field (or its negative) is placed in accumulator **aN** and can also be output according to the **Z** field.
aN = [–](Z=Y) {+,–} X	NZVU	The sum or difference of the **Y** and **X** fields is stored in accumulator **aN**, and **Y** can also be output according to the **Z** field.

Table 9. Replacement Table for DA Multiply/Accumulate Instructions

Replace	Value†	Description
aN, aM	a0—a3	One of the four DAU accumulators.
X, Y	*rP, *rP++, *rP– –, *rP++rI a0—a3 ibuf	32-bit memory location. One of the four DAU accumulators. SIO input buffer.
Z	*rP, *rP++, *rP– –, *rP++rI, *rP++rIr obuf pdr	32-bit memory location. **rIr** indicates carry reverse add. SIO output buffer. PIO data register (**pdr** concatenated with **pdr2**).

† **rP** refers to **r1—r14** and is used as a memory pointer. **rI** refers to **r15—r19** and is used as an increment pointer.

Instruction Set (continued)

Data Arithmetic (DA) Instructions (continued)

Table 10. DA Special Function Instructions

Instruction	DAU Flags Affected	Description
[Z=] aN = ic(Y)	NZ00	Input conversion, μ-law, A-law, 8-bit linear to float.
[Z=] aN = oc(Y)	—	Output conversion, float to μ-law, A-law, 8-bit linear (see Table 20).
[Z=] aN = float(Y)	NZ00	16-bit integer to float.
[Z=] aN = float24(Y)	NZ00	24-bit integer to float.
[Z=] aN = int(Y)	—	Float to 16-bit integer (round or truncate, **dauc[4]**).
[Z=] aN = int24(Y)	—	Float to 24-bit integer (round or truncate, **dauc[4]**).
[Z=] aN = round(Y)	NZVU*	Round float (40-bit) to float (32-bit).
[Z=] aN = ifalt(Y)	—	If (aN < 0) then [Z =] aN = Y else [Z =] aN.
[Z=] aN = ifaeq(Y)	—	If (aN = 0) then [Z =] aN = Y else [Z =] aN.
[Z=] aN = ifagt(Y)	—	If (aN > 0) then [Z =] aN = Y else [Z =] aN.
[Z=] aN = dsp(Y)	NZVU*	*IEEE*-to-DSP32 format conversion.
[Z=] aN = ieee(Y)	—	DSP32-to-*IEEE* format conversion.
[Z=] aN = seed(Y)	NZ0U*	32-bit to 32-bit reciprocal program seed.

* The *DSP3207 Digital Signal Processor Information Manual* dated July 1994 contains detailed descriptions of underflow and overflow for the **round**, **dsp**, and **seed** instructions. These descriptions can be found in the detailed descriptions of each instruction in Section 4.7 of the manual. The DSP3207 floating-point format, arithmetic, and the **round**, **dsp**, and **seed** instructions are identical to the DSP32C.

Table 11. Replacement Table for DA Special Function Instructions

Replace	Value†	Description
aN	a0—a3	One of the four DAU accumulators.
Y‡	*rP, *rP++, *rP– –, *rP++rI	32-bit memory location.
	a0—a3	One of the four DAU accumulators.
	ibuf	SIO input buffer.
	pdr	PIO data register (**pdr**).
Z	*rP, *rP++, *rP– –, *rP++rI	32-bit memory location.
	obuf	SIO output buffer.
	pdr	PIO data register (**pdr** concatenated with **pdr2**).

† **rP** refers to **r1**—**r14** and is used as a memory pointer. **rI** refers to **r15**—**r19** and is used as an increment pointer.
‡ **Y** may not be **a0**—**a3** for the **float** or **dsp** special functions.

Instruction Set (continued)

Control Arithmetic (CA) Instructions

Table 12. CA Control Instructions

Instruction	Flags Affected	Instruction Format	Description
if (CA COND) goto {rH, N, rH+N,}	None	0	Conditional branch.
if (rM– –>= 0) goto {rH, N, rH+N,}		3a	Conditional branch.
if (DA COND) goto {rH, N, rH+N,}		0	Conditional branch.
if (IO COND) goto {rH, N, rH+N,}		0	Conditional branch.
call {rH, N, M, rH+N,} (rM)		4	Call subroutine.
return (rM)		0	Return from subroutine.
ireturn		0	Return from interrupt.
do J,{K,rH}		3b, 3c	Do next J + 1 instructions. K + 1 (or rH + 1) times. J = 0, 1, 2 . . . 31. K = rH = 0, 1, 2 . . . 2047.
goto {rH, N, M, rH+N}		0	Unconditional branch.
nop		0	No operation.

Notes:
The **do** instruction and the instructions it encompasses are not interruptible, except for the last instruction during the last iteration. Further, the **do** instruction cannot be used in an interrupt routine.

A **do** loop should not contain any **goto** or **call** instructions. The assembler does not issue any warnings or errors if this is attempted.

Table 13. Replacement Table for CA Control Group Instructions, CA Conditions (CA COND)

Value	CAU Flags*	Description
pl	n = 0	Result is nonnegative (plus).
mi	n = 1	Result is negative (minus).
ne	z = 0	Result not equal to zero.
eq	z = 1	Result equal to zero.
vc	v = 0	Overflow clear, no overflow.
vs	v = 1	Overflow set, overflowed.
cc	c = 0	Carry clear, no carry.
cs	c = 1	Carry set, carry.
ge	n ^ v = 0	Greater than or equal to.
lt	n ^ v = 1	Less than.
gt	z | (n ^ v) = 0	Greater than.
le	z | (n ^ v) = 1	Less than or equal to.
hi	c | z = 0	Greater than (unsigned number).
ls	c | z = 1	Less than (unsigned number).

* Symbol interpretation: ^ = XOR; | = OR.

Instruction Set (continued)

Control Arithmetic (CA) Instructions (continued)

Table 14. Replacement Table for CA Control Group Instructions, DA Conditions (DA COND)

Value	DAU Flags	Description
ane	Z = 0	Not equal to zero.
aeq	Z = 1	Equal to zero.
age	N = 0	Greater than or equal to zero.
alt	N = 1	Less than zero.
avc	V = 0	Overflow clear, no overflow.
avs	V = 1	Overflow set, overflowed.
auc	U = 0	Underflow clear, no underflow.
aus	U = 1	Underflow set, underflowed.
agt	N I Z = 0	Greater than zero.
ale	N I Z = 1	Less than or equal to zero.

Table 15. Replacement Table for CA Control Group Instructions, I/O Conditions (IO COND)

Mnemonic	Condition	Description
ibe	ibf = 0	Input buffer empty.
ibf	ibf = 1	Input buffer full.
obe	obe = 1	Output buffer empty.
obf	obe = 0	Output buffer full.
pde	pdf = 0	Parallel data register empty.
pdf	pdf = 1	Parallel data register full.
pie	pif = 0	Parallel interrupt register empty.
pif	pif = 1	Parallel interrupt register full.
syc	sy = 0	Sync signal low.
sys	sy = 1	Sync signal high.
fbc	fb = 0	Serial frame boundary clear.
fbs	fb = 1	Serial frame boundary set.
ireq1_hi	ireq1 = 1	INTREQ1 pin is deasserted (1).
ireq1_lo	ireq1 = 0	INTREQ1 pin is asserted (0).
ireq2_hi	ireq2 = 1	INTREQ2 pin is deasserted (1).
ireq2_lo	ireq2 = 0	INTREQ2 pin is asserted (0).

Instruction Set (continued)

Control Arithmetic (CA) Instructions (continued)

Table 16. CA Arithmetic/Logic Instructions

Instruction	CAU Flags Affected	Instruction Format	Description
rD[e] = rH + N	nzvc	5a, 5b	Three operand add with 16-bit sign extended immediate.
rD[e] = rS1 + rS2	nzvc	6a, 6b	Triadic add.
rD[e] = rD + rS	nzvc	6a, 6b	Dyadic add.
rD[e] = rS1 – rS2	nzvc	6a, 6b	Triadic left subtract.
rD[e] = rS2 – rS1	nzvc	6a, 6b	Triadic right subtract.
rD[e] = rD – {N, rS}	nzvc	6a, 6b, 6c, 6d	Right subtract.
rD[e] – {N, rS}	nzvc	6a, 6b, 6c, 6d	Compare.
rD[e] = {N, rS} – rD	nzvc	6a, 6b, 6c, 6d	Left subtract.
rD[e] = rD & {N, rS}	nz00	6a, 6b, 6c, 6d	AND.
rD[e] = rS1 & rS2	nz00	6a, 6b	Triadic AND.
rD[e] & {N, rS}	nz00	6a, 6b, 6c, 6d	Bit test.
rD[e] = rD | {N, rS}	nz00	6a, 6b, 6c, 6d	OR.
rD[e] = rS1 | rS2	nz00	6a, 6b	Triadic OR.
rD[e] = rD ^ {N, rS}	nz00	6a, 6b, 6c, 6d	XOR.
rD[e] = rS1 ^ rS2	nz00	6a, 6b	Triadic XOR.
rD[e] = rS / 2	nz0c	6a, 6b	Arithmetic right shift.
rD[e] = rS >> 1	0z0c	6a, 6b	Logical right shift.
rD[e] = rS >>> 1	nz0c	6a, 6b	Rotate right through carry.
rD[e] = rS <<< 1	nzvc	6a, 6b	Rotate left through carry.
rD[e] = –rS	nzvc	6a, 6b	Negate.
rD[e] = rS * 2	nzvc	6a, 6b	Arithmetic left shift.
rD[e] = rD # {N, rS}	nz0c	6a, 6b, 6c, 6d	Dyadic carry reverse add.
rD[e] = rS1 # rS2	nz0c	6a, 6b	Triadic carry reverse add.
rD[e] = rD &~ {N, rS}	nzvc	6a, 6b, 6c, 6d	Dyadic AND with complement.
rD[e] = rS1 &~ rS2	nzvc	6a, 6b	Triadic AND with complement.
rD[e] = rS	nzvc	6a, 6b	Assignment.
rD[e] = rS {+,–} 1	nzvc	6a, 6b	Increment/decrement.

Except for instructions with immediate operands (**N**), all CA arithmetic/logic instructions above may also be conditionally executed on the basis of CA conditions. The syntax is as follows:

if (CA COND) *instruction*

The optional e suffix is for 24-bit (extended) operands. Flags are set according to the rules for 24-bit operands. **N** is always 16 bits, and bit 15 is extended to 24 bits, for 24-bit operations.

Instruction Set (continued)

Control Arithmetic (CA) Instructions (continued)

Table 17. CA Data Move Instructions

Instruction	CAU Flags Affected	Format	Description
rD = N	nz00	6c	16-bit immediate load.
rDe = M	—	8b	24-bit immediate load.
{ioc†, dauc} = VALUE	—	5a	5- or 21-bit immediate load.
{MEM, *N, obuf, piop} = {rSh, rSl}	—	7	MEM, *N, piop, and obuf are 8 bits.
{MEM, *N, obuf, pdr, pdr2, pir, pcw} = rS, pcsh	—	7	MEM, *N, and obuf are 16 bits.
{MEM, *N, obuf} = rSe, pcshe	—	7	MEM, *N, and obuf are 24 bits.
{rDh, rDl} = {MEM, *N, ibuf, piop}	nz00	7	MEM, *N, piop, and ibuf are 8 bits.
rD = {MEM, *N, ibuf, pdr, pdr2, pir, pcw}‡	nz00	7	MEM, *N, and ibuf are 16 bits.
rDe = {MEM, *N, ibuf}	nz00	7	MEM, *N, and ibuf are 24 bits.
MEM = {ibufl, piop}	—	7	8-bit transfer.
MEM = {ibuf, pdr, pdr2, pir, pcw}§	—	7	16-bit transfer.
MEM = {ibufe, pdre}§	—	7	32-bit transfer.
{obufl, piop} = MEM	—	7	8-bit transfer.
{obuf, pdr, pdr2, pir, pcw} = MEM	—	7	16-bit transfer.
{obufe, pdre} = MEM	—	7	32-bit transfer.

† **ioc = VALUE** may not be used in an interrupt routine.
‡ **rD = {pdr, pdr2, pir, pcw}** cannot be used in the presence of 32-bit PIO DMA.
§ **MEM = {pdr, pdr2, pir, pcw, pdre}** cannot be used in the presence of PIO DMA.

Table 18. Replacement Table for All CA Instructions

Replace	Value	Description
rH	pc, r1—r22	One of 22 general-purpose registers, or the program counter.
rM, rS, rD	r1—r22	One of 22 CAU registers.
rDh, rSh	r1—r22	High-order bits 8—15 are moved. The low-order bits 0—7 are cleared for **rD** and remain unchanged for **rS**.
rDl, rSl	r1—r22	Low-order bits 0—7 are moved. The high-order bits are cleared for **rD** and remain unchanged for **rS**.
MEM	*rP, *rP++, *rP– –, *rP++rI, (P, I = 1—22)	32-bit, 16-bit, or 8-bit memory location.
N	16-bit number	Two's complement integer.
M	24-bit number	Two's complement integer.
VALUE	21-bit number or 5-bit number	VALUE is a 21-bit value for the **ioc** word and a 5-bit value for the **dauc** word.

Instruction Encoding

The following sections specify the device level encoding of the DSP32C instruction set.

DA Instruction Formats

Format 1. [Z=] aN = {+,–} Y {+,–} aM * X

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	0	0	1	M			r	F	S	N		X	Y	Z

Format 2. aN = {+,–} aM {+,–} (Z=Y) * X

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	0	1	0	M			r	F	S	N		X	Y	Z

Format 3. [Z=] aN = {+,–} aM {+,–} Y * X

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	0	1	1	M			r	F	S	N		X	Y	Z

Format 4. aN = {+,–} (Z = Y) {+,–} X

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	0	0	1	1	1	0	r	F	S	N		X	Y	Z

Format 5. Special Function Instructions

Bit	31	30	29	28	27	26—23	22	21	20—14	13—7	6—0
Field	0	1	1	1	1	G	N		0000000	Y	z

Instruction Encoding (continued)

Encoding for DA Instruction Formats

G Field. Specifies a data-type conversion operation.

G	Operation
0000	ic (input conversion)
0001	oc (output conversion)
0010	float
0011	int
0100	round
0101	ifalt
0110	ifaeq
0111	ifagt
1000	Reserved
1001	Reserved
1010	float24
1011	int24
1100	ieee (convert DSP to *IEEE*)
1101	dsp (convert *IEEE* to DSP)
1110	seed
1111	Reserved

M Field. Specifies the accumulator used or a constant value.

M	Operation
000	a0
001	a1
010	a2
011	a3
100	0.0
101	1.0
110	Specifies Format 4 DAU instruction
111	Reserved

F Field. Specifies sign of operation (adder input).

F	Operation
0	+
1	–

S Field. Specifies sign of operation (product).

S	Operation
0	+
1	–

r Field. Specifies bit-reversed addressing mode (carry-reverse add with register).

r	Operation
0	Nonbit-reversed
1	Bit-reversed

X, Y, Z Fields. These fields indicate register direct or register indirect modes. The 7-bit fields are divided into two subfields, p and i (pppiii). Bits 0—2 of the 7-bit field are labeled i. The i subfield specifies an rI register in the CAU. Bits 3—6 are labeled p. The p field specifies an rP register in the CAU.

p Field. Specifies register indirect: *rP, *rP++, *rP– –, *rP++rI, *rP++rIr.

p	Operation
0000	Selects register direct†
0001	r1
0010	r2
0011	r3
0100	r4
0101	r5
0110	r6
0111	r7
1000	r8
1001	r9
1010	r10
1011	r11
1100	r12
1101	r13
1110	r14
1111	Not allowed

† See i field (p = 0000).

Instruction Encoding (continued)

Encoding for DA Instruction Formats (continued)

N Field. Specifies the accumulator used.

N	Operation
00	a0
01	a1
10	a2
11	a3

i Field (p ≠ 0000). Specifies register-indirect: rl, rP++rl.

i	Operation (p ≠ 0000)
000	0
001	r15
010	r16
011	r17
100	r18
101	r19
110	–4(f), –2(i), –1(b)
111	+4(f), +2(i), +1(b)

i Field (p = 0000). Specifies a register-direct operation: REG. This is a special case of the i field (when p field equals zero).

i	Operation (p = 0000)
000	a0 – X, Y fields only
001	a1 – X, Y fields only
010	a2 – X, Y fields only
011	a3 – X, Y fields only
100	ibuf – X, Y fields only
101	obuf – Z field only
110	pdr – Y, Z fields
111	No write, Z field only

CA Instruction Formats (Eight Format Groups)

Refer to CAU Encoding for CA Instruction Formats for an explanation of each field, except where actual bit values (0, 1) are given.

Formats 0 and 1. Conditional Branch: 24-Bit Register-Indirect with 16-Bit Sign-Extended Offset.

Bit	31	30	29	28	27	26—22	21	20—16	15—0
Field	0	0	0	0	0	C	G	H	N

For **ireturn** instruction, C = 00000, G = 1, H = pcsh = 11110, N = 0.
For **nop** instruction, C = 00000, G = 0, H = 00000, N = 0.

Format 2. Reserved

Bit	31	30	29	28	27	26	25—20	19—15	14—10	9—5	4—0
Field	0	0	0	0	1	0	—	—	—	—	—

Format 3a. Loop Counter

Bit	31	30	29	28	27	26	25—21	20—16	15—0
Field	0	0	0	0	1	1	M	H	N

Instruction Encoding (continued)

CA Instruction Formats (Eight Format Groups) (continued)

Format 3b. Do Instruction (Immediate)

Bit	31	30	29	28	27	26	25—21	20—16	15—11	10—0
Field	1	0	0	0	1	1	00000	J	00000	K

Format 3c. Do Instruction (Register)

Bit	31	30	29	28	27	26	25—21	20—16	15—5	4—0
Field	1	0	0	0	1	1	00001	J	00000000000	H

Format 4. Call: 24-Bit Register-Indirect with 16-Bit Immediate Offset

Bit	31	30	29	28	27	26	25—21	20—16	15—0
Field	0	0	0	1	0	0	M	H	N

Format 5a. 16-Bit Three Operand Add

Bit	31	30	29	28	27	26	25—21	20—16	15—0
Field	0	0	0	1	0	1	D	H	N

Format 5b. 24-Bit Three Operand Add with 16-Bit Sign-Extended Immediate

Bit	31	30	29	28	27	26	25—21	20—16	15—0
Field	1	0	0	1	0	1	D	H	N

Format 6a. 16-Bit Arithmetic/Logic Group — Register Source

Bit	31	30	29	28	27	26	25	24—21	20—16	15—13	12	11	10	9—5	4—0
Field	0	0	0	1	1	0	0	F	D	C*	G	E	K	S1	S2

* Three least significant bits of the C field (CA conditions only).

Format 6b. 24-Bit Arithmetic/Logic Group — Register Source

Bit	31	30	29	28	27	26	25	24—21	20—16	15—13	12	11	10	9—5	4—0
Field	1	0	0	1	1	0	0	F	D	C*	G	E	K	S1	S2

* Three least significant bits of the C field (CA conditions only).

Format 6c. 16-Bit Arithmetic/Logic Group — Immediate Operand

Bit	31	30	29	28	27	26	25	24—21	20—16	15—0
Field	0	0	0	1	1	0	1	F	D	N

Format 6d. 24-Bit Arithmetic/Logic Group — Immediate Operand

Bit	31	30	29	28	27	26	25	24—21	20—16	15—0
Field	1	0	0	1	1	0	1	F	D	N

Instruction Encoding (continued)

CA Instruction Formats (Eight Format Groups) (continued)

Format 7a. Data Move Group — Direct Memory Address

Bit	31	30	29	28	27	26	25	24	23	22	21	20—16	15—0
Field	0	0	0	1	1	1	0	T	W		0	H	N

Format 7b. Data Move Group — Pointer Increment, Memory Address

Bit	31	30	29	28	27	26	25	24	23	22	21	20—16	15—11	10	9—5	4—0
Field	0	0	0	1	1	1	1	T	W		1	H	—	r	P	I

Format 7c. Data Move Group — I/O

Bit	31	30	29	28	27	26	25	24	23	22	21	20—16	15—10	9—5	4—0
Field	0	0	0	1	1	1	1	T	W		0	H	—	00000	R

Format 7d. Data Move Group — Memory to I/O

Bit	31	30	29	28	27	26	25	24	23	22	21	20—16	15—11	10	9—5	4—0
Field	0	0	0	1	1	1	0	T	W		1	R	—	r	P	I

Format 8a. Unconditional Branch: 24-Bit Register-Indirect with 24-Bit Offset

Bit	31	30	29	28—21	20—16	15—0
Field	1	0	1	NE	H	N

Format 8b. 24-Bit Immediate Load

Bit	31	30	29	28—21	20—16	15—0
Field	1	1	0	NE	H	N

Format 8c. Call Subroutine: 24-Bit Direct Immediate Address

Bit	31	30	29	28—21	20—16	15—0
Field	1	1	1	NE	M	N

Instruction Encoding (continued)

CAU Encoding for CA Instruction Formats

C Field. Specifies a CA, DA, or I/O condition. For Format 6a and 6b instructions, only CA conditions are allowed, and are specified by the three least significant bits of the C field.

C	Operation
00xxx	**CA Condition**
00000	No condition
00001	n
00010	z
00011	v
00100	c
00101	n ^ v
00110	z | (n ^ v)
00111	c | z
01xxx	**DA Condition**
01000	U
01001	N
01010	Z
01011	V
01100	N | Z
01101	Reserved
01110	Reserved
01111	Reserved
10xxx	**I/O Condition**
10000	ibf
10001	obe
10010	pdf
10011	pif
10100	sy
10101	fb
10110	ireq1
10111	ireq2

T Field. Specifies the direction of a transfer to or from a register.

T	Operation
0	Data is moved to a register from memory
1	Data is moved to memory from a register

E Field. Specifies whether the instruction is a two- or three-operand instruction.

E	Operation
0	Two-operand instruction
1	Three-operand instruction (register source)

K Field. Specifies whether the instruction is to be executed based on the condition field.

K	Operation
0	Nonconditional execution
1	Conditional execution

W Field. Specifies the high or low byte or integer data.

W	Operation
00	High byte
01	Low byte
10	Integer
11	32 bits

G Field. Specifies whether to branch if the condition specified in the C field is true or false.

G	Operation
0	Branch if condition = 0
1	Branch if condition = 1

F Field. Specifies the arithmetic/logic group function encoding.

F	Operation
0000	+ addition
0001	*2 multiplication by 2
0010	– subtraction {N, rS} – rD
0011	# carry-reverse add
0100	– subtraction rD – {N, rS}
0101	– negation
0110	& ≈ and with complement
0111	– compare (no store)
1000	^ exclusive or
1001	>>>1 rotate right through carry
1010	| bitwise OR
1011	<<<1 rotate left through carry
1100	>>1 shift right by 1
1101	/2 divide by 2
1110	& bitwise AND
1111	& bitwise AND (no store)

Instruction Encoding (continued)

CAU Encoding for CA Instruction Formats (continued)

S, D, M, or H Fields. Used for register encoding.

S, D, M, or H	Operation
00000	0
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Program counter (pc)
10000	0
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	–4(f), –2(i), –1(b)
10111	+4(f), +2(i), +1(b)
11000	r20 (pin)
11001	r21 (pout)
11010	dauc
11011	ioc
11100	Reserved
11101	r22 (ivtp)
11110	pcsh (pc shadow)
11111	Reserved

P Field. Specifies a register-indirect data move: *rP, *rP++, *rP– –, *rP++rI.

P	Operation
00000	Selects Format 7C
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Reserved
10000	Reserved
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	Reserved
10111	Reserved
11000	r20 (pin)
11001	r21 (pout)
11010	Reserved
11011	Reserved
11100	Reserved
11101	r22 (ivtp)
11110	Reserved
11111	Reserved

Instruction Encoding (continued)

CAU Encoding for CA Instruction Formats (continued)

I Field. Specifies a register-indirect operation.

I	Operation
00000	Reserved
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Reserved
10000	0
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	–2(i), –1(b)
10111	+2(i), +1(b)
11000	r20 (pin)
11001	r21 (pout)
11010	Reserved
11011	Reserved
11100	Reserved
11101	r22 (ivtp)
11110	Reserved
11111	Reserved

r Field. Specifies bit-reversed addressing mode (carry-reverse add with register).

r	Operation
0	Nonbit-reversed
1	Bit-reversed

N Field. Specifies a 16-bit integer included as immediate data or as an address.

NE Field. Specifies most significant 8 bits of 24-bit integer included as an immediate. NE concatenated with N forms the 24-bit integer.

R Field (P = 00000). Specifies a register-direct operation. This field is valid when the P field is zero.

R	Operation (P = 00000)
00000	Reserved
00001	Reserved
00010	Reserved
00011	Reserved
00100	ibuf
00101	obuf
00110	pdr
00111	Reserved
01000	Reserved
01001	Reserved
01010	Reserved*
01011	Reserved
01100	Reserved
01101	Reserved
01110	piop
01111	Reserved
10000	Reserved
10001	Reserved
10010	Reserved
10011	Reserved
10100	pdr2
10101	Reserved
10110	pir
10111	Reserved
.	.
.	.
.	.
11101	Reserved
11110	pcw
11111	Reserved

* bkp access for development system use.

Register Operation

This section describes the register settings which control or display various operating conditions in the DSP32C digital signal processor. Table 19 and Table 20 show the settings for the **ioc** and **dauc** registers. In Table 19, **internal** refers to signals generated by the DSP32C; **external** refers to signals generated for the DSP32C by an external device. The **ioc** register is cleared on reset.

Input/Output Control (ioc) Register

Table 19. Input/Output Control (ioc) Register

Bit	20	19	18	17	16	15—13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	DSZ	O24	CKI	OUT	IN	DMA	SAN	OLEN		AOL	AOC	ILEN		AIL	AIC	SLEN		BC	ASY

Bit(s)	Field	Description
0	ASY	If 0, SY is external. If 1, SY is internal. When generated internally, SY = {ICK, OCK} ÷ 256, 512, or 1024, based on **ioc[1]** (BC) and **ioc[3—2]** (SLEN).
1	BC	If 0, ICK is used to derive the internal load and SY signals. If 1, OCK is used to derive the internal load and SY signals.
3, 2	SLEN	These bits select the frequency ratio of the on-chip load signal to the on-chip SY signal. The possible ratios are listed below: Bit 3 Bit 2 Ratio 0 0 32 0 1 8 1 0 16 1 1 32
4	AIC	If 0, ICK is external. If 1, ICK is generated internally with a frequency of CKI ÷ 8 or CKI ÷ 24, based on **ioc[18]** (CKI).
5	AIL	If 0, ILD is external. If 1, ILD is generated internally with a frequency of ICK ÷ 32 or OCK ÷ 32, based on **ioc[1]** (BC).
7, 6	ILEN	These bits specify the length of the serial input data. Bit 7 Bit 6 Input Length 0 0 32 bits (prior to ILD) 0 1 8 bits (after ILD) 1 0 16 bits (after ILD) 1 1 32 bits (after ILD)
8	AOC	If 0, OCK is external. If 1, OCK is internally generated with a frequency of CKI ÷ 8 or CKI ÷ 24, based on **ioc[18]** (CKI).
9	AOL	If 0, OLD is external. If 1, OLD is internally generated with a frequency of ICK ÷ 32 or OCK ÷ 32, based on **ioc[1]** (BC).

Register Operation (continued)

Input/Output Control (ioc) Register (continued)

Table 19. Input/Output Control (ioc) Register (continued)

Bit	20	19	18	17	16	15—13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	DSZ	O24	CKI	OUT	IN	DMA	SAN	OLEN		AOL	AOC	ILEN		AIL	AIC	SLEN		BC	ASY

Bit(s)	Field	Description
11, 10	OLEN	These bits, in conjunction with **ioc[19]** (O24), specify the length of the serial output data. Bit 19 / Bit 11 / Bit 10 / Output Length 0 / 0 / 0 / 32 bits (no OSE is generated) 0 / 0 / 1 / 8 bits 0 / 1 / 0 / 16 bits 0 / 1 / 1 / 32 bits 1 / 0 / 0 / 24 bits 1 / 0 / 1 / Reserved 1 / 1 / x / Reserved
12	SAN	If 0, clear sanity bit. If 1, set sanity bit.
15—13	DMA	These bits control serial direct memory accesses (DMA). Bit 15 / Bit 14 / Bit 13 0 / 0 / 0 / No DMA 0 / 0 / 1 / Input DMA when IBF is high 0 / 1 / 0 / Output DMA when OBE is high 0 / 1 / 1 / Input DMA when IBF is high and output DMA when OBE is high 1 / 0 / 0 / Input and output DMA when IBF and OBE are high 1 / 0 / 1 / Input and output DMA when IBF is high 1 / 1 / 0 / Input and output DMA when OBE is high 1 / 1 / 1 / Input and output DMA when either IBF or OBE is high
16	IN	If 0, the LSB is received first during serial inputs. If 1, the MSB is received first during serial inputs.
17	OUT	If 0, the LSB is transmitted first during serial outputs. If 1, the MSB is transmitted first during serial outputs (cannot be used with 24-bit output length).
18	CKI	If 0, the internal bit-clock frequency is CKI ÷ 8. If 1, the internal bit-clock frequency is CKI ÷ 24.
19	O24	See OLEN, bits 11 and 10, for the use of this bit.
20	DSZ	If 0, the data size of input and output DMA is 32 bits. If 1, the data size of input DMA is determined by the ILEN field and the data size of output DMA is determined by the OLEN and O24 fields. (24-bit is performed as 32-bit.)

Register Operation (continued)

DAU Control (dauc) Register

Table 20. DAU Control (dauc) Register

Bit	4	3	2	1	0
Field	DAUC				

Bit(s)	Field	Description
4—0	DAUC	This register controls the type conversions performed on input and output data. The permissible combinations are shown below: xx0x0 — μ-law input conversion xx0x1 — A-law input conversion x0x0x — μ-law output conversion x0x1x — A-law output conversion xx1xx — Linear byte input conversion x1xxx — Linear byte output conversion 1xxxx — Truncate on float-to-integer conversions 0xxxx — Round on float-to-integer conversions (default) Choosing the linear byte input and/or output mode will override the corresponding μ-law/A-law setting.

Note: x = don't care.

Register Operation (continued)

Parallel I/O Register Selection

The parallel I/O interface provides a processor address bus (PAB0—PAB3) to select access to the various PIO registers. Table 21 shows the register selections possible. Table 22 through Table 25 display the PIO registers. All PIO registers may be read or written by the external device, except **esr**, which is read-only, and the **pcw**, which is only accessible by the DSP32C. Bit 9 of the parallel I/O control register (**pcr[9]**) is used to configure an 8-bit or 16-bit parallel interface. **pcr[1]** provides a DSP32-compatible means of accessing the **pir** register. **pcr[9]** = 1 and **pcr[1]** = 0 should not be used together.

Table 21. PIO Register Selection

PAB3—PAB0	Register Selected		
	DSP32-Compatible Mode	DSP32C 8-Bit Mode	DSP32C 16-Bit Mode
	pcr[9] = 0, pcr[1] = 0	pcr[9] = 0, pcr[1] = 1	pcr[9] = 1, pcr[1] = 1
0000	par(l) — low byte	par(l) — low byte	par
0001	par(h) — high byte	par(h) — high byte	Reserved
0010	pdr(l) — low byte	pdr(l) — low byte	pdr
0011	pdr(h) — high byte	pdr(h) — high byte	Reserved
0100	emr(l) — low byte	emr(l) — low byte	emr
0101	emr(h) — high byte	emr(h) — high byte	Reserved
0110	esr	esr	esr
0111	pcr(l) — low byte	pcr(l) — low byte	pcr
1000	pir(h) — high byte	pir(l) — low byte	pir
1001	pir(h) — high byte	pir(h) — high byte	Reserved
1010	pir(h) — high byte	pcr(h) — high byte	Reserved*
1011	pir(h) — high byte	pare	pare
1100	pir(h) — high byte	pdr2(l) — low byte	pdr2
1101	pir(h) — high byte	pdr2(h) — high byte	Reserved
1110	pir(h) — high byte	Reserved	Reserved
1111	pir(h) — high byte	Reserved	Reserved

* **pcr**(h) accessible for development system use.

Register Operation (continued)

Parallel I/O Control Register (pcr)

The PIO control register (**pcr**) is a 16-bit register used by an external device to control transfer modes with the DSP32C device.

Table 22. Parallel I/O Control Register (pcr)

Bit	15—11	10	9	8	7	6	5	4	3	2	1	0
Field	RES	FLG	PIO16	DMA32	RES	PIFs	PDFs	AUTO	DMA	ENI	REGMAP	RESET

Bit(s)	Field	Description
0	RESET	If 0, halt. If 1, run. A zero-to-one transition initiates a reset sequence.
1	REGMAP	Selects between the possible PAB-to-register mappings. (See Table 21.)
2	ENI	If 0, disables setting (1) and clearing (0) of the PIF pin due to reading or writing of the **pir**. If 1, enables setting (1) and clearing (0) of the PIF pin due to reading or writing of the **pir**.
3	DMA	If 0, PIO DMA is disabled. If 1, PIO DMA is enabled.
4	AUTO	If 0, **par** is not autoincremented on DMA. If 1, **par** is autoincremented on DMA.
5	PDFs	**pdr** status (read only). Set (1) when **pdr** is written by the DSP32C or an external device. Cleared (0) when **pdr** is read by the DSP32C or an external device.
6	PIFs	**pir** status (read only). Set (1) when **pir** is written by the DSP32C or an external device. Cleared (0) when **pir** is read by the DSP32C or an external device.
7	RES	Reserved.
8	DMA32	If 0, DMA transfers are 16 bits (**pdr**). If 1, DMA transfers are 32 bits (**pdr** and **pdr2**).
9	PIO16	If 0, the PIO interface is 8 bits. If 1, the interface is 16 bits.
10	FLG	If 0, the PDF and PIF changes on the leading edge of reads. If 1, the PDF and PIF changes on the trailing edge of reads.
11—15	RES	Reserved.

Notes:
A reset sequence clears the contents of the **pcr**, except **pcr[0]** which is set. To achieve a setting other than the default, the **pcr** must be written again after the reset.

When configuring the DSP32C PIO for 16-bit transfers, since reset clears (0) **pcr[1]**, the PIO is initialized in the DSP32-compatible mode. **pcr**(h) is not accessible in this mode. To access **pcr**(h), an external device must first write a logic 1 to **pcr[1]** (REGMAP). This places the PIO in the DSP32C 8-bit mode. **pcr**(h) may now be written (PAB3—PAB0 = 1010) to change the DMA32, PIO16, and FLG bits.

Register Operation (continued)

Error Source Register (esr)

The 8-bit error source register (**esr**) is a read-only register which is readable only by the external system. The register, which is cleared after a read operation, stores the error condition status.

Table 23. Error Source Register (esr)

Bit	7	6	5	4	3	2	1	0
Field	LOSY	LOS	ADER	OUE	RES	WPIR	NAN	RES

Bit	Field	Description
0	RES	Reserved.
1	NAN	If set (1), *IEEE*-to-DSP32 conversion detected a NaN.
2	WPIR	If set (1), the **pir** was written.
3	RES	Reserved.
4	OUE	If set (1), DAU overflow or underflow occurred.
5	ADER	Addressing error. If set (1), an attempt was made to access a float variable or an integer variable with an address that was not a multiple of four or two, respectively.
6	LOS	Loss of sanity. If set (1), sanity bit in the **ioc** register is set (1), and SY changes state from high to low.
7	LOSY	Loss of sync. If set (1), loss of external synchronization.

Register Operation (continued)

Error Mask Register (emr)

The 16-bit error mask register (**emr**) can be read or written by the external device and is divided into two halves. Bits 0, 2, and 3 and bits 8, 10, and 11 are reserved. When the **emr** is read, these bits are all read as logic one. **emr[1]** and **emr[4—7]**, when set (1), mask the corresponding error condition in the **esr** for signaling an external device. Similarly, **emr[9]** and **emr[12—15]**, when set (1), mask the corresponding error condition in the **esr** (i.e., bit 9 of the **emr** corresponds to bit 1 of the **esr**) for halting the DSP32C. When the DSP32C is reset, all **emr** bits are set (1).

Table 24. Error Mask Register (emr)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Halt Mask								PIF Notification Mask							

Bits	Field	Description
0—7	PIF Notification Mask	Each bit in the field is set (1) to mask each corresponding **esr** bit from signaling the external device (via the PIF pin) when an error source is detected. If a bit in this field is cleared (0), the corresponding **esr** bit is unmasked to allow the external device to be signaled if the error is detected. emr esr Error Source 0 0 Reserved 1 1 NaN — Not a Number (*IEEE*-to-DSP32C) 2 2 Reserved 3 3 Reserved 4 4 OUE — DAU Overflow/Underflow Occurred 5 5 ADER — Addressing Error 6 6 LOS — Loss of Sanity 7 7 LOSY — Loss of External Sync
8—15	Halt Mask	Each bit in the field is set (1) to mask each corresponding **esr** bit from halting the DSP32C when an error source is detected. If a bit in this field is cleared (0), the corresponding **esr** bit is unmasked to allow the DSP32C to be halted if the error was detected. emr esr Error Source 8 0 Reserved 9 1 NaN — Not a Number (*IEEE*-to-DSP32C) 10 2 Reserved 11 3 Reserved 12 4 OUE — DAU Overflow/Underflow Occurred 13 5 ADER — Addressing Error 14 6 LOS — Loss of Sanity 15 7 LOSY — Loss of External Sync

Register Operation (continued)

Processor Control Word (pcw) Register

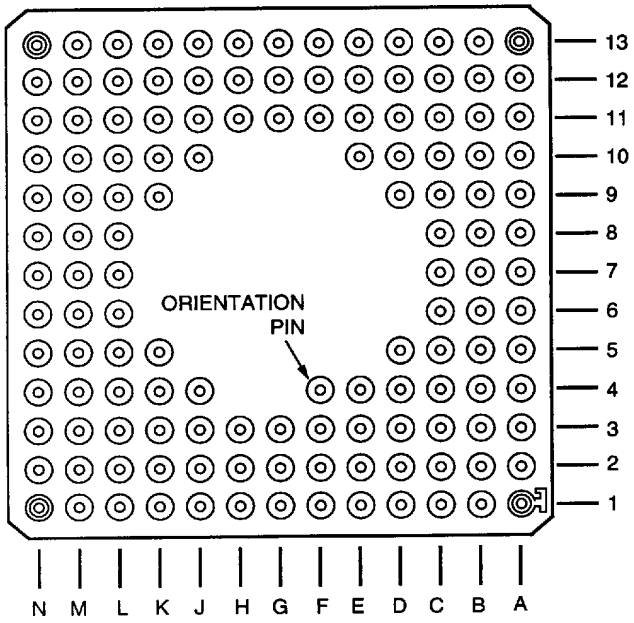
Table 25. Processor Control Word (pcw) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	INTER						PEND	MGN	PIOPH	PIOPL	MEMA		MEMB		WA	WB

Bit(s)	Field	Description
0	WB	If 0, disable wait-state generator for external memory partition B. If 1, enable wait-state generator for external memory partition B.
1	WA	If 0, disable wait-state generator for external memory partition A. If 1, enable wait-state generator for external memory partition A.
3, 2	MEMB	These bits select the number of wait-states that will be generated for the external memory in partition B. 00 — 1 wait-state* 01 — 2 wait-states 10 — 3 wait-states 11 — 2 or more wait-states (controlled by SRDYN signal)
5, 4	MEMA	These bits select the number of wait-states that will be generated for the external memory in partition A. 00 — 1 wait-state* 01 — 2 wait-states 10 — 3 wait-states 11 — 2 or more wait-states (controlled by SRDYN signal)
6	PIOPL	If 0, PIOP3—PIOP0 are inputs. If 1, PIOP3—PIOP0 are outputs when **pcr[9]**(PIO16) = 0.
7	PIOPH	If 0, PIOP7—PIOP4 are inputs. If 1, PIOP7—PIOP4 are outputs when **pcr[9]**(PIO16) = 0.
8	MGN	If 0, the MGN pin acts as a memory output enable signal. If 1, the MGN pin is used by the bus arbitration protocol to indicate that an external memory access is pending.
9	PEND	If **pcw[8]**(MGN) = 0, this bit is not used. If **pcw[8]** = 1, the logical value of this bit is ORed with an internal signal that indicates an external access is pending. It is then inverted to produce the signal at the MGN pin (i.e., if **pcw[8]**(MGN) = 1 and **pcw[9]**(PEND) = 1, then the pin MGN = 0).
15—10	INTER	Each bit in this field corresponds to one of the six sources for an interrupt. A value of 1 in a position enables the corresponding interrupt source; a value of 0 disables the source. Bit — Interrupt — Source 10 — INTREQ2 — Interrupt 2 pin 11 — OBE — Serial output buffer empty 12 — IBF — Serial input buffer full 13 — PDE — Parallel data empty (output) 14 — PDF — Parallel data full (input) 15 — INTREQ1 — Interrupt 1 pin

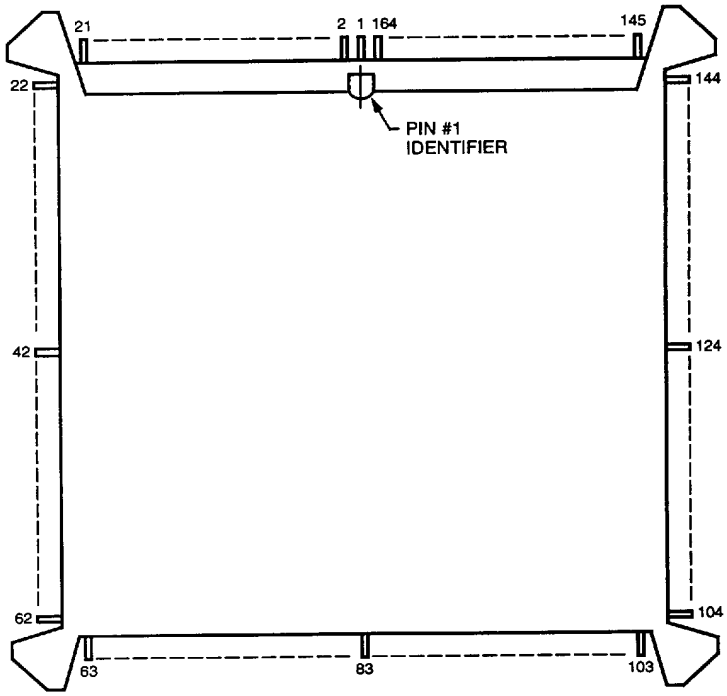
* 1 wait-state = one period of CKI = 12.5 ns at maximum clock frequency.

Pin Information



5-3616(C)

Figure 4. 133-Pin Square CPGA (DSP32C-R3) Diagram (Bottom View)



5-3617(C)

Figure 5. 164-Pin BQFP Package (DSP32C-F3) Diagram (Top View)

Pin Information (continued)

Pins by Functional Group Order

Table 26. DSP32C Pin Descriptions

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin (BQFP)	Pin (CPGA)	Symbol	Type*	Name/Description
108	D13	AB00	O(3)	**External Memory Address Bus — Bit 0.**
110	D12	AB01		**External Memory Address Bus — Bit 1.**
111	C13	AB02		**External Memory Address Bus — Bit 2.**
112	C12	AB03		**External Memory Address Bus — Bit 3.**
114	B13	AB04		**External Memory Address Bus — Bit 4.**
115	B12	AB05		**External Memory Address Bus — Bit 5.**
118	A13	AB06		**External Memory Address Bus — Bit 6.**
120	A12	AB07		**External Memory Address Bus — Bit 7.**
123	B11	AB08		**External Memory Address Bus — Bit 8.**
122	A11	AB09		**External Memory Address Bus — Bit 9.**
124	B10	AB10		**External Memory Address Bus — Bit 10.**
127	A10	AB11		**External Memory Address Bus — Bit 11.**
128	A9	AB12		**External Memory Address Bus — Bit 12.**
130	A8	AB13		**External Memory Address Bus — Bit 13.**
131	B6	AB14		**External Memory Address Bus — Bit 14.**
132	C7	AB15		**External Memory Address Bus — Bit 15.**
126	B8	AB16		**External Memory Address Bus — Bit 16.**
119	C8	AB17		**External Memory Address Bus — Bit 17.**
116	C9	AB18		**External Memory Address Bus — Bit 18.**
107	C10	AB19		**External Memory Address Bus — Bit 19.**
100	D10	AB20		**External Memory Address Bus — Bit 20.**
106	E10	AB21		**External Memory Address Bus — Bit 21.**
152	A2	DB00	I/O(3)	**External Memory Data Bus — Bit 0.**
153	A1	DB01		**External Memory Data Bus — Bit 1.**
154	B3	DB02		**External Memory Data Bus — Bit 2.**
156	B2	DB03		**External Memory Data Bus — Bit 3.**
157	B1	DB04		**External Memory Data Bus — Bit 4.**
158	C2	DB05		**External Memory Data Bus — Bit 5.**
160	C1	DB06		**External Memory Data Bus — Bit 6.**
161	D3	DB07		**External Memory Data Bus — Bit 7.**
162	D2	DB08		**External Memory Data Bus — Bit 8.**
164	D1	DB09		**External Memory Data Bus — Bit 9.**
2	E2	DB10		**External Memory Data Bus — Bit 10.**
5	E1	DB11		**External Memory Data Bus — Bit 11.**

* I = input; O = output; (3) = 3-state, P = power.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Functional Group Order (continued)

Table 26. DSP32C Pin Descriptions (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin (BQFP)	Pin (CPGA)	Symbol	Type*	Name/Description
3	F3	DB12	I/O(3)	**External Memory Data Bus — Bit 12.**
6	F2	DB13		**External Memory Data Bus — Bit 13.**
7	F1	DB14		**External Memory Data Bus — Bit 14.**
9	G2	DB15		**External Memory Data Bus — Bit 15.**
10	G1	DB16		**External Memory Data Bus — Bit 16.**
11	H3	DB17		**External Memory Data Bus — Bit 17.**
13	H2	DB18		**External Memory Data Bus — Bit 18.**
14	H1	DB19		**External Memory Data Bus — Bit 19.**
15	J2	DB20		**External Memory Data Bus — Bit 20.**
27	J1	DB21		**External Memory Data Bus — Bit 21.**
25	K3	DB22		**External Memory Data Bus — Bit 22.**
29	K2	DB23		**External Memory Data Bus — Bit 23.**
31	K1	DB24		**External Memory Data Bus — Bit 24.**
32	L2	DB25		**External Memory Data Bus — Bit 25.**
33	L1	DB26		**External Memory Data Bus — Bit 26.**
37	M3	DB27		**External Memory Data Bus — Bit 27.**
36	M2	DB28		**External Memory Data Bus — Bit 28.**
35	M1	DB29		**External Memory Data Bus — Bit 29.**
39	N2	DB30		**External Memory Data Bus — Bit 30.**
40	N1	DB31		**External Memory Data Bus — Bit 31.**
104	—	EAPN	O(3)	**External Access Pending (Active-Low).** Indicates that the DSP32C has an external access pending but does not have ownership of its bus.
101 99 148	E12 E13 E4	MMD0 MMD1 MMD2	I	**Memory Mode — Bit 0.** **Memory Mode — Bit 1.** **Memory Mode — Bit 2.** MMD0 and MMD1 select the address location of memory resources (see Memory Configuration).
134 135 138 140	A7 A6 A5 A4	MSN0 MSN1 MSN2 MSN3	O(3)	**Memory Select — Bit 0 (Active-Low).** **Memory Select — Bit 1 (Active-Low).** **Memory Select — Bit 2 (Active-Low).** **Memory Select — Bit 3 (Active-Low).** MSN0—MSN3 (Active-low) select individual bytes 0, 1, 2, or 3 of memory addressed by the external memory address bus.

* I = input; O = output; (3) = 3-state, P = power.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Functional Group Order (continued)

Table 26. DSP32C Pin Descriptions (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin (BQFP)	Pin (CPGA)	Symbol	Type*	Name/Description
142	A3	MGN/ EAPN	O(3)	**Memory Output Enable/External Access Pending (Active-Low).** When **pcw[8]** = 0, MGN indicates that memory output should be placed on the external memory data bus. When **pcw[8]** = 1, EAPN indicates that the DSP32C has an external access pending but does not have ownership of its bus.
139	B4	MWN	O(3)	**Memory Write (Active-Low).** Controls data writes to memory.
136	C6	ASN	O(3)	**Address Strobe (Active-Low).** Indicates a valid address on the address bus.
143	C5	DSN	O(3)	**Data Strobe (Active-Low).** During a read transaction, DSN indicates that data may be placed on the data bus. During a write transaction, DSN indicates that valid data is present on the data bus.
144	C4	CYCLEIN	O(3)	**Cycle Initiate (Active-Low).** Indicates the beginning of a valid external memory transaction.
150	D4	RWN	O(3)	**Read/Write.** If HIGH, memory transaction is a read operation, and, if LOW, memory transaction is a write operation.
149	F4	SRDYN	I	**Synchronous Ready (Active-Low).** Indicates to the DSP32C that the memory transaction may be completed.
28	L6	BREQN	I	**Bus Request (Active-Low).** When asserted, the DSP32C places data, address, and control signals in the high-impedance state.
19	K5	BRACKN	O(3)	**Bus Request Acknowledge (Active-Low).** Indicates that the DSP32C has relinquished its address, data, and control lines, and that the external processor may access the external memory of the DSP32C.
24	L5	INTREQ1	I	**Interrupt Request 1 (Active-Low).** Higher-priority external interrupt. Maskable in the **pcw** register.
23	L4	INTREQ2	I	**Interrupt Request 2 (Active-Low).** Lower-priority external interrupt. Maskable in the **pcw** register.
18	K4	IACK1	O(3)	**Interrupt Acknowledge 1.** Indicates the servicing of interrupt request 1.
17	J4	IACK2	O(3)	**Interrupt Acknowledge 2.** Indicates the servicing of interrupt request 2.
82	K13	PDB00	I/O(3)	**Parallel Data Bus — Bit 0.**
80	K12	PDB01		**Parallel Data Bus — Bit 1.**
79	K11	PDB02		**Parallel Data Bus — Bit 2.**
78	L13	PDB03		**Parallel Data Bus — Bit 3.**
76	L12	PDB04		**Parallel Data Bus — Bit 4.**

* I = input; O = output; (3) = 3-state, P = power.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Functional Group Order (continued)

Table 26. DSP32C Pin Descriptions (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin (BQFP)	Pin (CPGA)	Symbol	Type*	Name/Description
75	M13	PDB05	I/O(3)	**Parallel Data Bus — Bit 5.**
74	M12	PDB06		**Parallel Data Bus — Bit 6.**
72	M11	PDB07		**Parallel Data Bus — Bit 7.**
66	J10	PDB08/ PIOP0	I/O(3)	**Parallel Data Bus — Bit 8/PIO Port — Bit 0.**
67	K10	PDB09/ PIOP1		**Parallel Data Bus — Bit 9/PIO Port — Bit 1.**
68	L10	PDB10/ PIOP2		**Parallel Data Bus — Bit 10/PIO Port — Bit 2.**
61	N11	PDB11/ PIOP3		**Parallel Data Bus — Bit 11/PIO Port — Bit 3.**
60	M10	PDB12/ PIOP4		**Parallel Data Bus — Bit 12/PIO Port — Bit 4.**
59	L9	PDB13/ PIOP5		**Parallel Data Bus — Bit 13/PIO Port — Bit 5.**
53	L8	PDB14/ PIOP6		**Parallel Data Bus — Bit 14/PIO Port — Bit 6.**
52	L7	PDB15/ PIOP7		**Parallel Data Bus — Bit 15/PIO Port — Bit 7.**
89	H13	PAB0	I	**Processor Address Bus — Bit 0.**
91	G12	PAB1		**Processor Address Bus — Bit 1.**
92	G13	PAB2		**Processor Address Bus — Bit 2.**
84	J12	PAB3 (PACK)†		**Processor Address Bus — Bit 3.** PAB0—PAB3 are decoded to select the appropriate PIO register.
85	J13	PEN	I	**Processor Interface Enable (Active-Low).** When active, PEN allows a read or a write of the PIO data bus (PDB).
87	H12	PGN	I	**Processor Read Enable (Active-Low).** Allows an external microprocessor to read data from the selected PIO register.
88	H11	PWN	I	**Processor Write Enable (Active-Low).** When active, enables on-chip registers to be written by an external microprocessor.
70	N12	PIF (PINT)‡	O(3)	**Parallel Interrupt Full.** Interrupt to µP. PIF is set when a non-masked error occurs, or when the DSP32C or an external microprocessor writes to **pir**, and **pcr[2]** is set; PIF is cleared when **esr** or **pir** is read by the µP, or **pir** is read by the DSP32C.
71	N13	PDF	O(3)	**Parallel Data Full.** Set when **pdr** is written by the DSP32C or an external microprocessor; cleared when **pdr** is read by the DSP32C or an external microprocessor.

* I = input; O = output; (3) = 3-state, P = power.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Functional Group Order (continued)

Table 26. DSP32C Pin Descriptions (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin (BQFP)	Pin (CPGA)	Symbol	Type*	Name/Description
57	N10	DI	I	**Data Input.** Serial input PCM data.
47	N6	IBF	O(3)	**Input Buffer Full.** Indicates state of input buffer (**ibuf**). IBF is cleared when **ibuf** is loaded onto the data bus by the DSP32C.
56	N9	ICK	I/O(3)	**Input Clock.** Clock for serial PCM input data. In internal mode, ICK is an output; in external mode, ICK is an input, depending on the **ioc** register.
55	N8	ILD	I/O(3)	**Input Load.** Clock for loading input buffer from serial-to-parallel converter. In internal mode, ILD is an output; in external mode, ILD is an input, depending on the **ioc** register.
43	M4	DO	O(3)	**Data Output.** Serial output PCM data. 3-stated when OEN is set.
45	N5	OBE	O(3)	**Output Buffer Empty.** Indicates the state of serial PCM output buffer (**obuf**). OBE is cleared when **obuf** is written by the DSP32C.
51	M8	OCK	I/O(3)	**Output Clock.** Clock for serial PCM output data. In internal mode, OCK is an output; in external mode, OCK is an input, depending on the **ioc** register.
49	N7	OLD	I/O(3)	**Output Load.** Clock for loading parallel-to-serial converter from **obuf**. In internal mode, OLD is an output; in external mode, OLD is an input, depending on the **ioc** register.
44	N4	OSE	O(3)	**Output Shift Register Empty.** Indicates end of serial output transmission. OSE is the complement of OLD delayed by the number of bits in the transmission, as set by the **ioc** register.
41	N3	OEN	I	**Output Enable (Active-Low).** Enables DO for output. When high, DO is 3-stated.
48	M6	SY	I/O(3)	**Synchronization.** Internal mode (Output)—DSP32C provides frame sync. External mode (Input)—frame sync is provided to the DSP32C. (May also be used as a general-purpose status pin when configured in external mode.)

* I = input; O = output; (3) = 3-state, P = power.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Functional Group Order (continued)

Table 26. DSP32C Pin Descriptions (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin (BQFP)	Pin (CPGA)	Symbol	Type*	Name/Description
96	D11	CKI	I	**Clock In.** System clock.
93	F11	CKO	O(3)	**Clock Out.** Buffered clock at the same frequency as CKI. Synchronizes external devices to the DSP32C.
95	F12	RESTN	I	**Reset (Active-Low).** Controls the DSP32C run/halt state. A low level causes entry into the halt state. The low-to-high transition causes the reset sequence. Reset sequence stores **pc** in **r14**; clears **pc**, **ioc**, **esr**; and sets **emr** to mask all errors. The **pcr** register bits, except **pcr[0]**, are cleared; **pcr[0]** is set. CAU and DAU condition flags and the **dauc** register are not affected by reset. The **pcw** register is set to generate two or more wait-states (depending on SRDYN signal) for external memory.
97	F13	ZN	I(R)	**3-State (Active-Low).** When active, all DSP32C output pins are 3-stated. When not connected, ZN is inactive. Used for power-on reset.
8, 16, 26, 34, 42, 50, 58, 69, 77, 86, 94, 105, 113, 121, 129, 137, 147, 155, 163	B7, E3, E11, J3, J11, M7	V_{DD}	P	**+5 V.**
4, 12, 22, 30, 38, 46, 54, 65, 73, 81, 90, 98, 109, 117, 125, 133, 141, 151, 159	B5, B9, C3, C11, D5, D9, G3, G11, K9, L3, L11, M5, M9	V_{SS}	P	**Ground.**

* I = input; O = output; (3) = 3-state, P = power.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Numerical Order

Table 27. DSP32C Pin Descriptions—CPGA Package

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
A1	DB01	I/O(3)	**External Memory Data Bus — Bit 1.**
A2	DB00	I/O(3)	**External Memory Data Bus — Bit 0.**
A3	MGN/ EAPN	O(3)	**Memory Output Enable/External Access Pending.**
A4	MSN3	O(3)	**Memory Select — Bit 3.**
A5	MSN2	O(3)	**Memory Select — Bit 2.**
A6	MSN1	O(3)	**Memory Select — Bit 1.**
A7	MSN0	O(3)	**Memory Select — Bit 0.**
A8	AB13	O(3)	**External Memory Address Bus — Bit 13.**
A9	AB12	O(3)	**External Memory Address Bus — Bit 12.**
A10	AB11	O(3)	**External Memory Address Bus — Bit 11.**
A11	AB09	O(3)	**External Memory Address Bus — Bit 9.**
A12	AB07	O(3)	**External Memory Address Bus — Bit 7.**
A13	AB06	O(3)	**External Memory Address Bus — Bit 6.**
B1	DB04	I/O(3)	**External Memory Data Bus — Bit 4.**
B2	DB03	I/O(3)	**External Memory Data Bus — Bit 3.**
B3	DB02	I/O(3)	**External Memory Data Bus — Bit 2.**
B4	MWN	O(3)	**Memory Write.**
B5	V_{SS}	P	**Ground.**
B6	AB14	O(3)	**External Memory Address Bus — Bit 14.**
B7	V_{DD}	P	**+5 V.**
B8	AB16	O(3)	**External Memory Address Bus — Bit 16.**
B9	V_{SS}	P	**Ground.**
B10	AB10	O(3)	**External Memory Address Bus — Bit 10.**
B11	AB08	O(3)	**External Memory Address Bus — Bit 8.**
B12	AB05	O(3)	**External Memory Address Bus — Bit 5.**
B13	AB04	O(3)	**External Memory Address Bus — Bit 4.**
C1	DB06	I/O(3)	**External Memory Data Bus — Bit 6.**
C2	DB05	I/O(3)	**External Memory Data Bus — Bit 5.**
C3	V_{SS}	P	**Ground.**
C4	CYCLEIN	O(3)	**Cycle Initiate.**
C5	DSN	O(3)	**Data Strobe.**
C6	ASN	O(3)	**Address Strobe.**

* I = input; O = output; P = power; (3) = 3-state; (R) = on-chip pull-up.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 27. DSP32C Pin Descriptions—CPGA Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
C7	AB15	O(3)	**External Memory Address Bus — Bit 15.**
C8	AB17	O(3)	**External Memory Address Bus — Bit 17.**
C9	AB18	O(3)	**External Memory Address Bus — Bit 18.**
C10	AB19	O(3)	**External Memory Address Bus — Bit 19.**
C11	Vss	P	**Ground.**
C12	AB03	O(3)	**External Memory Address Bus — Bit 3.**
C13	AB02	O(3)	**External Memory Address Bus — Bit 2.**
D1	DB09	I/O(3)	**External Memory Data Bus — Bit 9.**
D2	DB08	I/O(3)	**External Memory Data Bus — Bit 8.**
D3	DB07	I/O(3)	**External Memory Data Bus — Bit 7.**
D4	RWN	O(3)	**Read/Write.**
D5	Vss	P	**Ground.**
D9	Vss	P	**Ground.**
D10	AB20	O(3)	**External Memory Address Bus — Bit 20.**
D11	CKI	I	**Clock In.**
D12	AB01	O(3)	**External Memory Address Bus — Bit 1.**
D13	AB00	O(3)	**External Memory Address Bus — Bit 0.**
E1	DB11	I/O(3)	**External Memory Data Bus — Bit 11.**
E2	DB10	I/O(3)	**External Memory Data Bus — Bit 10.**
E3	VDD	P	**+5 V.**
E4	MMD2	I	**Memory Mode — Bit 2.**
E10	AB21	O(3)	**External Memory Address Bus — Bit 21.**
E11	VDD	P	**+5 V.**
E12	MMD0	I	**Memory Mode — Bit 0.**
E13	MMD1	I	**Memory Mode — Bit 1.**
F1	DB14	I/O(3)	**External Memory Data Bus — Bit 14.**
F2	DB13	I/O(3)	**External Memory Data Bus — Bit 13.**
F3	DB12	I/O(3)	**External Memory Data Bus — Bit 12.**
F4	SRDYN	I	**Synchronous Ready.**
F11	CKO	O(3)	**Clock Out.**
F12	RESTN	I	**Reset.**
F13	ZN	I(R)	**3-state.**
G1	DB16	I/O(3)	**External Memory Data Bus — Bit 16.**
G2	DB15	I/O(3)	**External Memory Data Bus — Bit 15.**

* I = input; O = output; P = power; (3) = 3-state; (R) = on-chip pull-up.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 27. DSP32C Pin Descriptions—CPGA Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
G3	Vss	P	**Ground.**
G11	Vss	P	**Ground.**
G12	PAB1	I	**Processor Address Bus — Bit 1.**
G13	PAB2	I	**Processor Address Bus — Bit 2.**
H1	DB19	I/O(3)	**External Memory Data Bus — Bit 19.**
H2	DB18	I/O(3)	**External Memory Data Bus — Bit 18.**
H3	DB17	I/O(3)	**External Memory Data Bus — Bit 17.**
H11	PWN	I	**Processor Write Enable.**
H12	PGN	I	**Processor Read Enable.**
H13	PAB0	I	**Processor Address Bus — Bit 0.**
J1	DB21	I/O(3)	**External Memory Data Bus — Bit 21.**
J2	DB20	I/O(3)	**External Memory Data Bus — Bit 20.**
J3	VDD	P	**+5 V.**
J4	IACK2	O(3)	**Interrupt Acknowledge 2.**
J10	PDB08/ PIOP0	I/O(3)	**Parallel Data Bus — Bit 8/PIO Port — Bit 0.**
J11	VDD	P	**+5 V.**
J12	PAB3 (PACK)†	I	**Processor Address Bus — Bit 3.**
J13	PEN	I	**Processor Interface Enable.**
K1	DB24	I/O(3)	**External Memory Data Bus — Bit 24.**
K2	DB23	I/O(3)	**External Memory Data Bus — Bit 23.**
K3	DB22	I/O(3)	**External Memory Data Bus — Bit 22.**
K4	IACK1	O(3)	**Interrupt Acknowledge 1.**
K5	BRACKN	O(3)	**Bus Request Acknowledge.**
K9	Vss	P	**Ground.**
K10	PDB09/ PIOP1	I/O(3)	**Parallel Data Bus — Bit 9/PIO Port — Bit 1.**
K11	PDB02	I/O(3)	**Parallel Data Bus — Bit 2.**
K12	PDB01	I/O(3)	**Parallel Data Bus — Bit 1.**
K13	PDB00	I/O(3)	**Parallel Data Bus — Bit 0.**
L1	DB26	I/O(3)	**External Memory Data Bus — Bit 26.**
L2	DB25	I/O(3)	**External Memory Data Bus — Bit 25.**
L3	Vss	P	**Ground.**
L4	INTREQ2	I	**Interrupt Request 2.**

* I = input; O = output; P = power; (3) = 3-state; (R) = on-chip pull-up.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 27. DSP32C Pin Descriptions—CPGA Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
L5	INTREQ1	I	**Interrupt Request 1.**
L6	BREQN	I	**Bus Request.**
L7	PDB15/ PIOP7	I/O(3)	**Parallel Data Bus — Bit 15/PIO Port — Bit 7.**
L8	PDB14/ PIOP6	I/O(3)	**Parallel Data Bus — Bit 14/PIO Port — Bit 6.**
L9	PDB13/ PIOP5	I/O(3)	**Parallel Data Bus — Bit 13/PIO Port — Bit 5.**
L10	PDB10/ PIOP2	I/O(3)	**Parallel Data Bus — Bit 10/PIO Port — Bit 2.**
L11	Vss	P	**Ground.**
L12	PDB04	I/O(3)	**Parallel Data Bus — Bit 4.**
L13	PDB03	I/O(3)	**Parallel Data Bus — Bit 3.**
M1	DB29	I/O(3)	**External Memory Data Bus — Bit 29.**
M2	DB28	I/O(3)	**External Memory Data Bus — Bit 28.**
M3	DB27	I/O(3)	**External Memory Data Bus — Bit 27.**
M4	DO	O(3)	**Data Output.**
M5	Vss	P	**Ground.**
M6	SY	I/O(3)	**Synchronization.**
M7	VDD	P	**+5 V.**
M8	OCK	I/O(3)	**Output Clock.**
M9	Vss	P	**Ground.**
M10	PDB12/ PIOP4	I/O(3)	**Parallel Data Bus — Bit 12/PIO Port — Bit 4.**
M11	PDB07	I/O(3)	**Parallel Data Bus — Bit 7.**
M12	PDB06	I/O(3)	**Parallel Data Bus — Bit 6.**
M13	PDB05	I/O(3)	**Parallel Data Bus — Bit 5.**
N1	DB31	I/O(3)	**External Memory Data Bus — Bit 31.**
N2	DB30	I/O(3)	**External Memory Data Bus — Bit 30.**
N3	OEN	I	**Output Enable.**
N4	OSE	O(3)	**Output Shift Register Empty.**
N5	OBE	O(3)	**Output Buffer Empty.**
N6	IBF	O(3)	**Input Buffer Full.**
N7	OLD	I/O(3)	**Output Load.**
N8	ILD	I/O(3)	**Input Load.**

* I = input; O = output; P = power; (3) = 3-state; (R) = on-chip pull-up.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 27. DSP32C Pin Descriptions—CPGA Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
N9	ICK	I/O(3)	**Input Clock.**
N10	DI	I	**Data Input.**
N11	PDB11/ PIOP3	I/O(3)	**Parallel Data Bus — Bit 11/PIO Port — Bit 3.**
N12	PIF (PINT)‡	O(3)	**Parallel Input Full.**
N13	PDF	O(3)	**Parallel Data Full.**

* I = input; O = output; P = power; (3) = 3-state; (R) = on-chip pull-up.
† PAB3 is labeled PACK in the DSP32.
‡ PIF is labeled PINT in the DSP32.

Table 28. DSP32C Pin Descriptions—BQFP Package

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
1	—	NC	—
2	DB10	I/O(3)	**External Memory Data Bus — Bit 10.**
3	DB12	I/O(3)	**External Memory Data Bus — Bit 12.**
4	V_{SS}	P	**Ground.**
5	DB11	I/O(3)	**External Memory Data Bus — Bit 11.**
6	DB13	I/O(3)	**External Memory Data Bus — Bit 13.**
7	DB14	I/O(3)	**External Memory Data Bus — Bit 14.**
8	V_{DD}	P	**+5 V.**
9	DB15	I/O(3)	**External Memory Data Bus — Bit 15.**
10	DB16	I/O(3)	**External Memory Data Bus — Bit 16.**
11	DB17	I/O(3)	**External Memory Data Bus — Bit 17.**
12	V_{SS}	P	**Ground.**
13	DB18	I/O(3)	**External Memory Data Bus — Bit 18.**
14	DB19	I/O(3)	**External Memory Data Bus — Bit 19.**
15	DB20	I/O(3)	**External Memory Data Bus — Bit 20.**
16	V_{DD}	P	**+5 V.**
17	IACK2	O(3)	**Interrupt Acknowledge 2.**
18	IACK1	O(3)	**Interrupt Acknowledge 1.**
19	BRACKN	O(3)	**Bus Request Acknowledge.**
20	—	NC	—
21	—	NC	—

* I = input; O = output; P = power; NC = no connection; (3) = 3-state; (R) = on-chip pull-up.
† PIF is labeled PINT in the DSP32.
‡ PAB3 is labeled PACK in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 28. DSP32C Pin Descriptions—BQFP Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
22	VSS	P	**Ground.**
23	INTREQ2	I	**Interrupt Request 2.**
24	INTREQ1	I	**Interrupt Request 1.**
25	DB22	I/O(3)	**External Memory Data Bus — Bit 22.**
26	VDD	P	**+5 V.**
27	DB21	I/O(3)	**External Memory Data Bus — Bit 21.**
28	BREQN	I	**Bus Request.**
29	DB23	I/O(3)	**External Memory Data Bus — Bit 23.**
30	VSS	P	**Ground.**
31	DB24	I/O(3)	**External Memory Data Bus — Bit 24.**
32	DB25	I/O(3)	**External Memory Data Bus — Bit 25.**
33	DB26	I/O(3)	**External Memory Data Bus — Bit 26.**
34	VDD	P	**+5 V.**
35	DB29	I/O(3)	**External Memory Data Bus — Bit 29.**
36	DB28	I/O(3)	**External Memory Data Bus — Bit 28.**
37	DB27	I/O(3)	**External Memory Data Bus — Bit 27.**
38	VSS	P	**Ground.**
39	DB30	I/O(3)	**External Memory Data Bus — Bit 30.**
40	DB31	I/O(3)	**External Memory Data Bus — Bit 31.**
41	OEN	I	**Output Enable.**
42	VDD	P	**+5 V.**
43	DO	O(3)	**Data Output.**
44	OSE	O(3)	**Output Shift Register Empty.**
45	OBE	O(3)	**Output Buffer Empty.**
46	VSS	P	**Ground.**
47	IBF	O(3)	**Input Buffer Full.**
48	SY	I/O(3)	**Synchronization.**
49	OLD	I/O(3)	**Output Load.**
50	VDD	P	**+5 V.**
51	OCK	I/O(3)	**Output Clock.**
52	PDB15/ PIOP7	I/O(3)	**Parallel Data Bus — Bit 15/PIO Port — Bit 7.**
53	PDB14/ PIOP6	I/O(3)	**Parallel Data Bus — Bit 14/PIO Port — Bit 6.**

* I = input; O = output; P = power; NC = no connection; (3) = 3-state; (R) = on-chip pull-up.
† PIF is labeled PINT in the DSP32.
‡ PAB3 is labeled PACK in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 28. DSP32C Pin Descriptions—BQFP Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
54	Vss	P	**Ground.**
55	ILD	I/O(3)	**Input Load.**
56	ICK	I/O(3)	**Input Clock.**
57	DI	I	**Data Input.**
58	VDD	P	**+5 V.**
59	PDB13/ PIOP5	I/O(3)	**Parallel Data Bus — Bit 13/PIO Port — Bit 5.**
60	PDB12/ PIOP4	I/O(3)	**Parallel Data Bus — Bit 12/PIO Port — Bit 4.**
61	PDB11/ PIOP3	I/O(3)	**Parallel Data Bus — Bit 11/PIO Port — Bit 3.**
62	—	NC	—
63	—	NC	—
64	—	NC	—
65	Vss	P	**Ground.**
66	PDB08/ PIOP0	I/O(3)	**Parallel Data Bus — Bit 8/PIO Port — Bit 0.**
67	PDB09/ PIOP1	I/O(3)	**Parallel Data Bus — Bit 9/PIO Port — Bit 1.**
68	PDB10/ PIOP2	I/O(3)	**Parallel Data Bus — Bit 10/PIO Port — Bit 2.**
69	VDD	P	**+5 V.**
70	PIF (PINT)†	O(3)	**Parallel Interrupt Full.**
71	PDF	O(3)	**Parallel Data Full.**
72	PDB07	I/O(3)	**Parallel Data Bus — Bit 7.**
73	Vss	P	**Ground.**
74	PDB06	I/O(3)	**Parallel Data Bus — Bit 6.**
75	PDB05	I/O(3)	**Parallel Data Bus — Bit 5.**
76	PDB04	I/O(3)	**Parallel Data Bus — Bit 4.**
77	VDD	P	**+5 V.**
78	PDB03	I/O(3)	**Parallel Data Bus — Bit 3.**
79	PDB02	I/O(3)	**Parallel Data Bus — Bit 2.**
80	PDB01	I/O(3)	**Parallel Data Bus — Bit 1.**
81	Vss	P	**Ground.**

* I = input; O = output; P = power; NC = no connection; (3) = 3-state; (R) = on-chip pull-up.
† PIF is labeled PINT in the DSP32.
‡ PAB3 is labeled PACK in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 28. DSP32C Pin Descriptions—BQFP Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
82	PDB00	I/O(3)	**Parallel Data Bus — Bit 0.**
83	—	NC	—
84	PAB3 (PACK)‡	I	**Processor Address Bus — Bit 3.**
85	PEN	I	**Processor Interface Enable.**
86	VDD	P	**+5 V.**
87	PGN	I	**Processor Read Enable.**
88	PWN	I	**Processor Write Enable.**
89	PAB0	I	**Processor Address Bus — Bit 0.**
90	VSS	P	**Ground.**
91	PAB1	I	**Processor Address Bus — Bit 1.**
92	PAB2	I	**Processor Address Bus — Bit 2.**
93	CKO	O(3)	**Clock Out.**
94	VDD	P	**+5 V.**
95	RESTN	I	**Reset.**
96	CKI	I	**Clock In.**
97	ZN	I(R)	**3-State.**
98	VSS	P	**Ground.**
99	MMD1	I	**Memory Mode — Bit 1.**
100	AB20	O(3)	**External Memory Address Bus — Bit 20.**
101	MMD0	I	**Memory Mode — Bit 0.**
102	—	NC	—
103	—	NC	—
104	EAPN	O(3)	**External Access Pending.**
105	VDD	P	**+5 V.**
106	AB21	O(3)	**External Memory Address Bus — Bit 21.**
107	AB19	O(3)	**External Memory Address Bus — Bit 19.**
108	AB00	O(3)	**External Memory Address Bus — Bit 0.**
109	VSS	P	**Ground.**
110	AB01	O(3)	**External Memory Address Bus — Bit 1.**
111	AB02	O(3)	**External Memory Address Bus — Bit 2.**
112	AB03	O(3)	**External Memory Address Bus — Bit 3.**
113	VDD	P	**+5 V.**
114	AB04	O(3)	**External Memory Address Bus — Bit 4.**

* I = input; O = output; P = power; NC = no connection; (3) = 3-state; (R) = on-chip pull-up.
† PIF is labeled PINT in the DSP32.
‡ PAB3 is labeled PACK in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 28. DSP32C Pin Descriptions—BQFP Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
115	AB05	O(3)	**External Memory Address Bus — Bit 5.**
116	AB18	O(3)	**External Memory Address Bus — Bit 18.**
117	Vss	P	**Ground.**
118	AB06	O(3)	**External Memory Address Bus — Bit 6.**
119	AB17	O(3)	**External Memory Address Bus — Bit 17.**
120	AB07	O(3)	**External Memory Address Bus — Bit 7.**
121	VDD	P	**+5 V.**
122	AB09	O(3)	**External Memory Address Bus — Bit 9.**
123	AB08	O(3)	**External Memory Address Bus — Bit 8.**
124	AB10	O(3)	**External Memory Address Bus — Bit 10.**
125	Vss	P	**Ground.**
126	AB16	O(3)	**External Memory Address Bus — Bit 16.**
127	AB11	O(3)	**External Memory Address Bus — Bit 11.**
128	AB12	O(3)	**External Memory Address Bus — Bit 12.**
129	VDD	P	**+5 V.**
130	AB13	O(3)	**External Memory Address Bus — Bit 13.**
131	AB14	O(3)	**External Memory Address Bus — Bit 14.**
132	AB15	O(3)	**External Memory Address Bus — Bit 15.**
133	Vss	P	**Ground.**
134	MSN0	O(3)	**Memory Select — Bit 0.**
135	MSN1	O(3)	**Memory Select — Bit 1.**
136	ASN	O(3)	**Address Strobe.**
137	VDD	P	**+5 V.**
138	MSN2	O(3)	**Memory Select — Bit 2.**
139	MWN	O(3)	**Memory Write.**
140	MSN3	O(3)	**Memory Select — Bit 3.**
141	Vss	P	**Ground.**
142	MGN	O(3)	**Memory Output Enable/External Access Pending.**
143	DSN	O(3)	**Data Strobe.**
144	CYCLEIN	O(3)	**Cycle Initiate.**
145	—	NC	—
146	—	NC	—
147	VDD	P	**+5 V.**
148	MMD2	I	**Memory Mode — Bit 2.**

* I = input; O = output; P = power; NC = no connection; (3) = 3-state; (R) = on-chip pull-up.
† PIF is labeled PINT in the DSP32.
‡ PAB3 is labeled PACK in the DSP32.

Pin Information (continued)

Pins by Numerical Order (continued)

Table 28. DSP32C Pin Descriptions—BQFP Package (continued)

Please refer to the *AT&T DSP32C Information Manual* for a complete description of each pin.

Pin	Symbol	Type*	Name
149	SRDYN	I	**Synchronous Ready.**
150	RWN	O(3)	**Read/Write.**
151	Vss	P	**Ground.**
152	DB00	I/O(3)	**External Memory Data Bus — Bit 0.**
153	DB01	I/O(3)	**External Memory Data Bus — Bit 1.**
154	DB02	I/O(3)	**External Memory Data Bus — Bit 2.**
155	VDD	P	**+5 V.**
156	DB03	I/O(3)	**External Memory Data Bus — Bit 3.**
157	DB04	I/O(3)	**External Memory Data Bus — Bit 4.**
158	DB05	I/O(3)	**External Memory Data Bus — Bit 5.**
159	Vss	P	**Ground.**
160	DB06	I/O(3)	**External Memory Data Bus — Bit 6.**
161	DB07	I/O(3)	**External Memory Data Bus — Bit 7.**
162	DB08	I/O(3)	**External Memory Data Bus — Bit 8.**
163	VDD	P	**+5 V.**
164	DB09	I/O(3)	**External Memory Data Bus — Bit 9.**

* I = input; O = output; P = power; NC = no connection; (3) = 3-state; (R) = on-chip pull-up.
† PIF is labeled PINT in the DSP32.
‡ PAB3 is labeled PACK in the DSP32.

Device Requirements and Characteristics

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Table 29. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Voltage Range on Any Pin with Respect to Ground	–0.5	6.0	V
Power Dissipation	—	1.7	W
Storage Temperature	–65	150	°C
External Lead Bonding and Soldering Temperature	—	300	°C

Warning: All CMOS devices are prone to latch-up if excessive current is injected to/from the substrate. To prevent latch-up at powerup, no input pin should be subjected to input voltages greater than V_{IL}, or less than $V_{SS} - 0.5$ V before V_{DD} is applied. After powerup, input should not be greater than $V_{DD} + 0.5$ V or less than $V_{SS} - 0.5$ V.

Handling Precautions

All MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. **Although input protection circuitry has been incorporated into the devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting.** AT&T employs a human-body model for ESD susceptibility testing. Since the failure voltage of electronic devices is dependent on the current and voltage and, hence, the resistance and capacitance, it is important that standard values be employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the AT&T human-body model test circuit. The breakdown voltage for the DSP32C is greater than 2000 V*, according to the human-body model. ESD data for the charged-device model is available on request.

* The value of 2000 V for the breakdown voltage is subject to change.

Device Requirements and Characteristics (continued)

Temperature Class Definitions

Table 30. Temperature Class Definitions

Temperature Class	Ambient Temperature T_A (°C)	
	Min	Max
Commercial	0	70
Industrial	–40	85

Recommended Operating Conditions

Table 31. Recommended Operating Conditions

Device Speed	Package	Temperature Class	Device Code	Supply Voltage V_{DD} (V)	
				Min	Max
50 ns	133-Pin CPGA	Commercial	DSP32C-R35---050	4.75	5.25
	164-Pin BQFP	Commercial	DSP32C-F35---050	4.75	5.25
	133-Pin CPGA	Industrial	DSP32C-R35---050-I	4.75	5.25
60 ns	133-Pin CPGA	Commercial	DSP32C-R35---060	4.75	5.25
	164-Pin BQFP	Commercial	DSP32C-F35---060	4.75	5.25
	133-Pin CPGA	Industrial	DSP32C-R35---060-I	4.75	5.25
80 ns	133-Pin CPGA	Commercial	DSP32C-R35---080	4.5	5.5
	164-Pin BQFP	Commercial	DSP32C-F35---080	4.5	5.5
	133-Pin CPGA	Industrial	DSP32C-R35---080-I	4.75	5.25
	164-Pin BQFP	Industrial	DSP32C-F35---080-I	4.75	5.25

Package Thermal Considerations

The recommended operating temperature specified above is based on the maximum power, package type, and maximum junction temperature. The following equation describes the relationship between these parameters. For certain applications, the maximum power may be less than the worst-case value and the following relationship can be used to determine the maximum ambient temperature allowed.

$$T_A = T_J - P \times \Theta_{JA}$$

Maximum Junction Temperature (T_J) in 133-Pin CPGA ..... +125 °C
133-Pin CPGA Maximum Thermal Resistance in Still-Air-Ambient (Θ_{JA}) ..... 25 °C/W

Maximum Junction Temperature (T_J) in 164-Pin BQFP ..... +125 °C
164-Pin BQFP Maximum Thermal Resistance in Still-Air-Ambient (Θ_{JA}) ..... 37 °C/W

Electrical Characteristics

The parameters below are valid for the following conditions:
Commercial temperature class device: T_A = 0 °C to 70 °C; V_{SS} = 0 V; C_{LOAD} = 50 pF.
Industrial temperature class device: T_A = –40 °C to +85 °C; V_{SS} = 0 V; C_{LOAD} = 50 pF.

Parameter	Sym	Min	Max	Unit
Input Voltage: All Pins Except PAB3—PAB0, PEN, PGN, PWN, OCK, ICK, SY*				
Low	V_{IL}	—	0.8	V
High (commercial temperature class device)	V_{IH}	2.0	—	V
High (industrial temperature class device)	V_{IH}	2.2	—	V
Input Voltage: Pins PAB3—PAB0, PEN, PGN, PWN, OCK, ICK, SY*				
Low	V_{IL}	—	0.8	V
High (commercial temperature class device)	V_{IH}	2.4	—	V
High (industrial temperature class device)	V_{IH}	2.7	—	V
Output Low Voltage				
Low (I_{OL} = 2 mA)	V_{OL}	—	0.4	V
Low (I_{OL} = 5 µA)	V_{OL}	—	0.2	V
Output High Voltage				
High (I_{OH} = –2 mA)	V_{OH}	V_{DD} – 0.7	—	V
High (I_{OH} = –5 µA)	V_{OH}	V_{DD} – 0.2	—	V
Input Leakage: All Inputs Except ZN				
Low (V_{IL} = 0 V) Low	I_{IL}	–5	—	µA
High (V_{IH} = 5.5 V) High	I_{IH}	—	5	µA
Input Leakage: ZN† Pin				
Low (V_{IL} = 0 V) Low	I_{IL}	–500	—	µA
High (V_{IH} = 5.5 V) High	I_{IH}	—	5	µA
Output Offset Current				
Low (V_{OL} = 0 V)	I_{OZL}	–10	—	µA
High (V_{OH} = 5.5 V)	I_{OZH}	—	10	µA
Input, Output, I/O Capacitance	CI	—	10	pF
Power Supply Current‡				
Instruction Cycle Time = 50 ns; tCKILCKIL = 12.5 ns	I_{DD}	—	306	mA
Instruction Cycle Time = 60 ns; tCKILCKIL = 15 ns	I_{DD}	—	255	mA
Instruction Cycle Time = 80 ns; tCKILCKIL = 20 ns	I_{DD}	—	225	mA
Power Dissipation§				
Instruction Cycle Time = 50 ns; tCKILCKIL = 12.5 ns	PD	—	1.7	W
Instruction Cycle Time = 60 ns; tCKILCKIL = 15 ns	PD	—	1.4	W
Instruction Cycle Time = 80 ns; tCKILCKIL = 20 ns	PD	—	1.25	W

* The ICK, OCK, and SY pins have Schmitt triggers with hysteresis in the range of 0.5 V to 0.8 V.
† This pin has a pull-up device.
‡ Current in the input buffers is highly dependent on the input voltage level. At full CMOS levels, essentially no dc current is drawn, but for levels near the threshold of 1.4 V, high and unstable levels of current may flow. There are 72 inputs to the chip (19 input-only and 53 input/output pins). If all inputs are connected to a dc voltage around 1.4 V, an additional current in the range of 150 mA can be drawn. This current can be almost totally eliminated by setting the input pins to CMOS voltage levels (V_{DD} or V_{SS}). Therefore, all unused inputs should be tied inactive to V_{DD} or V_{SS} and all unused I/O pins should be tied inactive through a 10 kΩ resistor to V_{DD} or V_{SS}.
§ The power dissipation listed is for output loads = 70 pF. Total power dissipation can be calculated on the basis of the application by adding $C \times V_{DD}^2 \times f$ for each output, where C is the load capacitance and f is the output frequency.

Timing Requirements and Characteristics

The characteristics listed are valid under the following conditions:

Commercial temperature class device: T_A = 0 °C to 70 °C; V_{SS} = 0 V; C_{LOAD} = 50 pF.

Industrial temperature class device: T_A = –40 °C to +85 °C; V_{SS} = 0 V; C_{LOAD} = 50 pF.

Output characteristics can be derated as a function of load capacitance (C_L).

All outputs except PDBs: $dT/dC_L \leq 0.04$ ns/pF for $0 \leq C_L \leq 100$ pF
PDB outputs: $dT/dC_L \leq 0.11$ ns/pF for $0 \leq C_L \leq 200$ pF

Test conditions for inputs:

- Rise and fall times of 4 ns or less
- Timing reference level for setup times is V_{IM} = 1.5 V
- Timing reference levels for hold times: V_{IH} = 2.0 V, V_{IL} = 0.8 V

Test conditions for outputs:

- C_{LOAD} = 50 pF
- Timing reference level for delay times is V_{OM} = 1.5 V
- Timing reference levels for hold times: V_{OH} = 2.4 V, V_{OL} = 0.4 V

CKI and CKO Timing

Table 32. CKI and CKO Timing (See Figure 6.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min	Max	Min	Max	Min	Max	
t1	tCKILCKIL	Clock In Period	12.5	500*	15	500*	20	500*	ns
t2	tCKILCKIH	Clock In Low	5.7	—	6.8	—	9	—	ns
t3	tCKIHCKIL	Clock In High	5.7	—	6.8	—	9	—	ns
t4	tCKIRISE	Clock In Rise Time	—	3	—	3.5	—	4	ns
t5	tCKIFALL	Clock In Fall Time	—	3	—	3.5	—	4	ns
t6	tCKILCKOL	CKI Low to CKO Low	—	5	—	6	—	8	ns
t6a	tCKOFALL	Clock Out Fall Time	—	3	—	3.5	—	4	ns
t6b	tCKORISE	Clock Out Rise Time	—	3	—	3.5	—	4	ns
t7	tCKIHCKOH	CKI High to CKO High	—	5	—	6	—	8	ns

* The internal RAM contents are retained if CKI drops to DC, but the device is not guaranteed to function properly with CKI below 500 ns.

Timing Requirements and Characteristics (continued)

External Memory Interface (EMI) Timing

Table 33. Definition of Timing Characteristics for External Memory Interface (See Figures 7 and 8.)

Abbreviated Reference	*IEEE* Symbol	Parameter
t8	tCKOLABV	CKO Low to Address Valid*
t8a	tCKOLABX	Address Hold After CKO Low*
t10	tCKOLRWNV	CKO Low to Read-Write Valid
t10a	tCKOLRWNX	Read-Write Hold After CKO Low
t11	tCKOLCYCNL	CKO Low to Cycle Initiate Low
t12	tCKOLCYCNH	CKO Low to Cycle Initiate High
t13	tABVASNL	Address Valid to Address Strobe Low*
t13a	tCKOHASNL	CKO High to Address Strobe Low
t14	tASNLASNH	Address Strobe Width
t14a	tCKOLASNH	CKO Low to Address Strobe High
t14b	tASNHABX	Address Hold After Address Strobe High*
t15	tABVDSNH	Data Strobe High After Address Valid*
t15a	tCKOLDSNL	CKO Low to Data Strobe Low
t15b	tCKOLDSNH	CKO Low to Data Strobe High
t16	tDSNLDSNH	Data Strobe Width
t17	tMGNLMGNH	Read Data Strobe Width
t17b	tMGNHMGNL	Read Strobe High to Read Strobe Low
t17c	tCKOHMGNL	CKO High to Read Strobe Low
t17d	tCKOLMGNH	CKO Low to Read Strobe High
t18	tDSNHABX	Address Hold After Data Strobe High*
t20	tDSNHRWNX	Read-Write Hold After Data Strobe High
t20a	tDSNHDBE	Data Strobe High to Data Bus Low-Z
t20b	tMGNHDBE	Read Strobe High to Data Bus Low-Z
t20c	tRWNLDBE	Read-Write Low to Data Bus Low-Z
t21	tDBVDSNH	Data Bus Valid to Data Strobe High
t21a	tDSNHDBZ	Data Strobe High to Data Bus Hi-Z
t21c	tCKOLDBZ	Data Bus Hi-Z After CKO Low
t21e	tCKOLDBV	CKO Low to Data Bus Valid
t21f	tCKOLDBE	Data Bus Low-Z After CKO Low
t22	tDBVMWNH	Data Bus Valid to Write Strobe High
t22a	tMWNLMWNH	Write Strobe Width
t22b	tCKOHMWNL	CKO High to Write Strobe Low
t22c	tMWNHABX	Address Hold After Write Strobe High*
t22d	tCKOHMWNH	CKO High to Write Strobe High
t23	tABVMGNL	Read Strobe Low After Address Valid*
t23a	tABVMWNL	Write Strobe Low After Address Valid*

* Timing of MSN0—MSN3 is the same as the address bus.

Timing Requirements and Characteristics (continued)

External Memory Interface (EMI) Timing (continued)

Table 33. Definition of Timing Characteristics for External Memory Interface (continued)
(see Figures 7 and 8.)

Abbreviated Reference	*IEEE* Symbol	Parameter
t24	tABVDSNL	Data Strobe Low After Address Valid*
t24a	tMWNHDBZ	Data Bus Hi-Z After Write Strobe High
t24b	tASNHDBZ	Data Bus Hi-Z After Address Strobe High

* Timing of MSN0—MSN3 is the same as the address bus.

Table 34. Timing Characteristics for External Memory Interface (See Figures 7 and 8.)

Abbreviated Reference	*IEEE* Symbol	50 ns*		60 ns*		80 ns*		Unit
		Min	Max	Min	Max	Min	Max	
t8†	tCKOLABV	0	5	0	6	0	8	ns
t8a†	tCKOLABX	0	—	0	—	0	—	ns
t10	tCKOLRWNV	0	5	0	6	0	8	ns
t10a	tCKOLRWNX	0	—	0	—	0	—	ns
t11	tCKOLCYCNL	0	4	0	5	0	6	ns
t12	tCKOLCYCNH	0	4	0	5	0	6	ns
t13†	tABVASNL	0.5T – 1	0.5T + 3	0.5T – 1	0.5T + 3	0.5T – 3	0.5T + 3	ns
t13a	tCKOHASNL	0	4	0	4	0	5	ns
t14	tASNLASNH	1.5T – 2 + NT	—	1.5T – 2 + NT	—	1.5T – 2 + NT	—	ns
t14a	tCKOLASNH	0	3	0	4	0	5	ns
t14b†	tASNHABX	0	—	0	—	0	—	ns
t15†	tABVDSNH	2T – 3 + NT	—	2T – 3 + NT	—	2T – 5 + NT	—	ns
t15a	tCKOLDSNL	0	3	0	4	0	5	ns
t15b	tCKOLDSNH	0	3	0	4	0	5	ns
t16	tDSNLDSNH	T – 1 + NT	—	T – 1 + NT	—	T – 2 + NT	—	ns
t17	tMGNLMGNH	1.5T – 2 + NT	—	1.5T – 2 + NT	—	1.5T – 4 + NT	—	ns
t17b	tMGNHMGNL	0.5T – 1	—	0.5T – 1	—	0.5T – 2	—	ns
t17c	tCKOHMGNL	0	5	0	5	0	6	ns
t17d	tCKOLMGNH	0	5	0	5	0	6	ns
t18†	tDSNHABX	0	—	0	—	0	—	ns
t20	tDSNHRWNX	0	—	0	—	0	—	ns
t20a	tDSNHDBE	T	—	T	—	T – 1	—	ns
t20b	tMGNHDBE	T – 2	—	T – 2	—	T – 4	—	ns

* T = tCKILCKIL; N = number of wait-states; NT is the product of N and T.
† Timing of MSN0—MSN3 is the same as the address bus.

Timing Requirements and Characteristics (continued)

External Memory Interface (EMI) Timing (continued)

Table 34. Timing Characteristics for External Memory Interface (continued) (See Figures 7 and 8.)

Abbreviated Reference	*IEEE* Symbol	50 ns*		60 ns*		80 ns*		Unit
		Min	Max	Min	Max	Min	Max	
t20c	tRWNLDBE	T – 1	—	T – 1	—	T – 2	—	ns
t21	tDBVDSNH	T – 3 + NT	—	T – 3 + NT	—	T – 5 + NT	—	ns
t21a	tDSNHDBZ	—	2	—	2	—	2	ns
t21c	tCKOLDBZ	0	—	0	—	0	—	ns
t21e	tCKOLDBV	0	4	0	5	0	8	ns
t21f	tCKOLDBE	0	—	0	—	0	—	ns
t22	tDBVMWNH	0.5T – 2 + NT	—	0.5T – 2 + NT	—	0.5T – 2 + NT	—	ns
t22a	tMWNLMWNH	T + NT	—	T + NT	—	T + NT	—	ns
t22b	tCKOHMWNL	0	4	0	5	0	7	ns
t22c	tMWNHABX	0.5T – 2	—	0.5T – 3	—	0.5T – 4	—	ns
t22d	tCKOHMWNH	0	3	0	4	0	6	ns
t23	tABVMGNL	0.5T – 2	—	0.5T – 3	—	0.5T – 4	—	ns
t23a	tABVMWNL	0.5T – 2	—	0.5T – 3	—	0.5T – 4	—	ns
t24	tABVDSNL	T – 2	—	T – 3	—	T – 4	—	ns
t24a	tMWNHDBZ	0.5T – 2	0.5T + 2	0.5T – 2	0.5T + 3	0.5T – 2	0.5T + 4	ns
t24b	tASNHDBZ	–1	2	–1	2	–1	2	ns

* T = tCKILCKIL; N = number of wait-states; NT is the product of N and T.
† Timing of MSN0—MSN3 is the same as the address bus.

Timing Requirements and Characteristics (continued)

External Memory Interface (EMI) Timing (continued)

Table 35. Definition of Timing Requirements for External Memory Interface (See Figures 7 and 8.)

Abbreviated Reference	*IEEE* Symbol	Parameter
t25	tSRDYNLCKOH	SRDYN Setup to CKO High
t26	tCKOHSRDYNH	SRDYN Hold After CKO High
t27a	tDBINASNH	DATA in Setup to Address Strobe High
t27c	tDBINVCKOL	DATA in Setup to CKO Low
t27d	tDBINVDSNH	DATA in Setup to Data Strobe High
t27m	tDBINVMGNH	DATA in Setup to Read Strobe High
t28a	tASNHDBX	DATA in Hold After Address Strobe High
t28c	tCKOLDBX	DATA in Hold After CKO Low
t28d	tDSNHDBX	DATA in Hold After Data Strobe High
t28m	tMGNHDBX	DATA in Hold After Read Strobe High
t29	tABVDBINV	Address Valid to DATA in Valid*
t29a	tASNLDBINV	Address Strobe Low to DATA in Valid
t29d	tDSNLDBINV	Data Strobe Low to DATA in Valid
t29m	tMGNLDBINV	Read Strobe Low to DATA in Valid

* Timing of MSN0—MSN3 is the same as the address bus.

Table 36. Timing Requirements for External Memory Interface (See Figures 7 and 8.)

Abbreviated	50 ns		60 ns		80 ns		Unit
Reference	Min	Max*	Min	Max*	Min	Max*	
t25	4	—	5	—	6	—	ns
t26	0	—	0	—	0	—	ns
t27a	6	—	7	—	8	—	ns
t27c	3	—	4	—	5	—	ns
t27d	6	—	7	—	8	—	ns
t27m	8	—	9	—	10	—	ns
t28a	0	—	0	—	0	—	ns
t28c	0	—	0	—	0	—	ns
t28d	0	—	0	—	0	—	ns
t28m	0	—	0	—	0	—	ns
t29†	—	2T – 7 + NT	—	2T – 8 + NT	—	2T – 10 + NT	ns
t29a	—	0.5T – 5 + NT	—	0.5T – 6 + NT	—	1.5T – 8 + NT	ns
t29d	—	T – 5 + NT	—	T – 6 + NT	—	T – 8 + NT	ns
t29m	—	1.5T – 7 + NT	—	1.5T – 8 + NT	—	1.5T – 10 + NT	ns

* T = tCKILCKIL; N = number of wait-states; NT is the product of N and T.
† Timing of MSN0—MSN3 is the same as the address bus.

Timing Requirements and Characteristics (continued)

Serial I/O (SIO) Timing

Note: Serial I/O is fully static; however, the maximum clock period (input and output) is tested only to the values stated in Table 37 and Table 38.

Table 37. Timing Requirements and Characteristics for Serial Input (See Figure 9.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min	Max	Min	Max	Min	Max	
t31	tICKLICKL	Clock Period	25	1000	30	1000	40	1000	ns
t32	tICKLICKH	Clock Low Time	11	—	13	—	18	—	ns
t33	tICKHICKL	Clock High Time	11	—	13	—	18	—	ns
t34	tILDHICKH	Load High Setup	5	—	6	—	8	—	ns
t35	tICKHILDX	Load High Hold	0	—	0	—	0	—	ns
t36	tILDLICKH	Load Low Setup	5	—	6	—	8	—	ns
t37	tICKHILDX	Load Low Hold	0	—	0	—	0	—	ns
t38	tDIVICKH	Data Setup	5	—	6	—	8	—	ns
t39	tICKHDIX	Data Hold	0	—	0	—	0	—	ns
t40	tICKHIBFH	Input Buffer Delay	—	12	—	14	—	23	ns

Table 38. Timing Requirements for Serial Output (See Figure 10.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min	Max	Min	Max	Min	Max	
t41	tOCKLOCKL	Clock Period	25	1000	30	1000	40	1000	ns
t42	tOCKLOCKH	Clock Low Time	11	—	13	—	18	—	ns
t43	tOCKHOCKL	Clock High Time	11	—	13	—	18	—	ns
t44	tOLDHOCKH	Load High Setup	5	—	6	—	8	—	ns
t45	tOCKHOLDX	Load High Hold	0	—	0	—	0	—	ns
t46	tOLDLOCKH	Load Low Setup	5	—	6	—	8	—	ns
t47	tOCKHOLDX	Load Low Hold	0	—	0	—	0	—	ns

Table 39. Timing Characteristics for Serial Output (See Figure 10.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min	Max	Min	Max	Min	Max	
t48	tOCKHDOV	Data Delay	—	12	—	14	—	23	ns
t49	tOCKHDOX	Data Hold	2	—	2	—	2	—	ns
t50	tOCKHOBEH	Output Buffer Empty Delay	—	12	—	14	—	23	ns
t51	tOCKHOSEH	Output Shift Register Delay	—	12	—	14	—	23	ns
t52	tOENLDOE	Enable Delay	—	12	—	14	—	23	ns
t53	tOENHDOZ	Disable Delay	—	12	—	14	—	23	ns

Timing Requirements and Characteristics (continued)

Serial I/O (SIO) Timing (continued)

Note: Serial I/O is fully static; however, the maximum clock period (input and output) is tested only to the values stated in Table 37 and Table 38.

Table 40. Timing Requirements for Serial Clock Generation (See Figure 11.)

Abbreviated Reference	*IEEE* Symbol	Parameter*	50 ns		60 ns		80 ns		Unit
			Min	Max	Min	Max	Min	Max	
t54	tSYHICKH tSYHOCKH	SY High Setup	8	—	8	—	8	—	ns
t55	tICKHSYX tOCKHSYX	SY High Hold	0	—	0	—	0	—	ns
t56	tSYLICKH tSYLOCKH	SY Low Setup	8	—	8	—	8	—	ns
t57	tICKHSYX tOCKHSYX	SY Low Hold	0	—	0	—	0	—	ns

* ICK or OCK is selected by **ioc[1]** (BC).

Table 41. Timing Characteristics for Serial Clock Generation (See Figure 11.)

Abbreviated Reference	*IEEE* Symbol	Parameter*	50 ns		60 ns		80 ns		Unit
			Min	Max	Min	Max	Min	Max	
t58	tICKHSYL tOCKHSYL	Internal SY Delay	—	12	—	14	—	23	ns
t59	tICKHILDL tOCKHOLDL	Internal Load Delay	—	12	—	14	—	23	ns
t60	tSYLILDL tSYLOLDL	Internal Load/SY Delay	—	12	—	14	—	23	ns
t61†	tICKHICKH tOCKHOCKH	Clock Period	300/ 100	—	360/ 120	—	480/ 160	—	ns
t62†	tICKLICKH tOCKLOCKH	Clock Low Time	135/ 35	—	165/ 45	—	220/ 60	—	ns
t63†	tICKHICKL tOCKHOCKL	Clock High Time	135/ 35	—	165/ 45	—	220/ 60	—	ns

* ICK or OCK is selected by **ioc[1]** (BC).
† Depends on the value of the internal clock, determined by **ioc[18]** (CKI). Either CKI ÷ 8 or CKI ÷ 24.

Timing Requirements and Characteristics (continued)

Parallel I/O (PIO) Timing

Table 42. Timing Requirements for PIO Read Cycle (See Figure 12.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min*	Max	Min*	Max	Min*	Max	
t64	tPAVPRL	Address Setup	5	—	6	—	8	—	ns
t65	tPRHPAX	Address Hold	0	—	0	—	0	—	ns
t70a	tPRLPRH	Read Pulse	2T	—	2T	—	2T	—	ns
t76g	tPRWHPRWL	PIO Idle†	2T	—	2T	—	2T	—	ns

* T = tCKILCKIL.
† A minimum 2T interval is required for the start of the read or write cycle following the end of the previous read or write cycle.

Table 43. Timing Characteristics for PIO Read Cycle (See Figure 12.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min*	Max	Min*	Max	Min*	Max	
t66	tPRLPDV	Access from Read	—	17	—	20	—	30	ns
t67	tPRHPDZ	Data Hold from Read	2	7	2	8	2	10	ns

Table 44. Timing Requirements for PIO Write Cycle (See Figure 13.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min*	Max	Min*	Max	Min*	Max	
t68	tPAVPWL	Address Setup	5	—	6	—	8	—	ns
t69	tPWHPAX	Address Hold	0	—	0	—	0	—	ns
t70	tPWLPWH	Write Pulse	2T	—	2T	—	2T	—	ns
t71	tPDVPWH	Data Setup	10	—	15	—	20	—	ns
t72	tPWHPDX	Data Hold	0	—	0	—	0	—	ns
t76g	tPRWHPRWL	PIO Idle†	2T	—	2T	—	2T	—	ns

* T = tCKILCKIL.
† A minimum 2T interval is required for the start of the read or write cycle following the end of the previous read or write cycle.

Table 45. Timing Characteristics for PDF and PIF (See Figure 12 and Figure 13.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min	Max*	Min	Max*	Min	Max*	
t73	tPWHPDFH	PDF Write Delay	—	T + 15	—	T + 18	—	T + 25	ns
t73a	tPWHPIFH	PIF Write Delay	—	T + 15	—	T + 18	—	T + 25	ns
t74	tPRLPDFL	PDF Read Delay	—	15	—	18	—	28	ns
t75	tPRLPIFL	PIF Read Delay	—	15	—	18	—	28	ns
t76a	tPRHPDFL	PDF Read Delay	—	T + 15	—	T + 18	—	T + 25	ns
t76	tPRHPIFL	PIF Read Delay	—	T + 15	—	T + 18	—	T + 25	ns

* T = tCKILCKIL.

Timing Requirements and Characteristics (continued)

Parallel I/O (PIO) Timing (continued)

Table 46. Timing Requirements and Characteristics for PIOP (See Figure 14.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min*	Max	Min*	Max	Min*	Max	
t76b	tPIOPVCKOL	PIOP Setup	7	—	8	—	10	—	ns
t76c	tCKOLPIOPX	PIOP Hold	0	—	0	—	0	—	ns

Table 47. Timing Requirements and Characteristics for PIOP (See Figure 14.)

Abbreviated Reference	*IEEE* Symbol	Parameter	50 ns		60 ns		80 ns		Unit
			Min*	Max	Min*	Max	Min*	Max	
t76d	tCKOHPIOPX	PIOP Output Hold	4	—	4	—	5	—	ns
t76e	tCKOHPIOPV	PIOP Output Delay	—	15	—	20	—	35	ns

Reset and Interrupt Timing

The following terms describe reset:

Reset state — The DSP32C is in the reset state when the internal reset signal is asserted, initializing the internal states of the chip. This state is entered when:

- Power-on reset is detected, or
- ZN and RESTN pins are low, or
- A 0-to-1 transition is detected on RESTN, or
- A 0-to-1 transition is detected on **pcr[0]** (only if RESTN = 1).

Powerup reset — Powerup reset occurs during the first eight clock cycles after power has been applied ($V_{DD} \geq 3$ V). On-chip circuitry detects powerup and puts the chip in the reset state.

Reset sequence — The reset sequence is the execution of the internally generated instructions **call 0 (r14)** followed by **nop**. The reset sequence always follows the reset state.

Halt mode — The DSP32C is executing internally generated nops during the halt mode. PIO DMA remains active.

Run mode — The DSP32C is fetching and executing instructions.

Powerup reset sequences. On powerup of the DSP32C, on-chip circuitry puts the device in the reset state for the first eight clock cycles.

At this time, the logic levels of RESTN and ZN (both are active-low) control the DSP32C's operation:

ZN	RESTN	Description
0	0	Remain in the reset state.
x*	1	Perform reset sequence then run.
1	0	Perform reset sequence then halt.

* x denotes don't care.

Reset and halt operation. While in the run mode, the DSP32C can be placed in other modes by asserting the RESTN and ZN pins or by using the **pcr** register. To enter the halt mode, assert RESTN or write **pcr[0]** = 0. Note that RESTN has priority over **pcr[0]**. To bring the chip out of the halt mode, deassert RESTN or write **pcr[0]** = 1. This initiates a reset state followed by the reset sequence followed by the run mode.

To enter the reset state immediately, assert ZN and RESTN. Subsequent operations are the same as on powerup.

To enter the halt mode using only the RESTN signal (see Figure 18):

1. Assert RESTN.
2. Deassert RESTN. The reset state is performed, followed by the reset sequence.
3. Assert RESTN, again, within 10 clock cycles. The DSP32C enters the halt mode without executing any instructions.

Timing Requirements and Characteristics (continued)

Reset and Interrupt Timing (continued)

Table 48. Definition of Timing Requirements and Characteristics for Interrupts and Reset
(see Figure 15, Figure 18, and Figure 19)

Abbreviated Reference	*IEEE* Symbol	Parameter
t77	tINTREQLINTREQH	INTREQ Assertion to Guarantee Interrupt Is Recognized
t78	tIACKHINTREQH	Interrupt Acknowledge to Request Deassertion
t79	tRESTNLRESTNH	RESTN Assertion to Guarantee Reset
t79a	tPUSV	Powerup to RESTN and ZN Valid
t79b	tRESTNHZNH	RESTN High to ZN High
t79c	tHALT	RESTN High to RESTN Low (enter halt after reset)
t80	tCKOLIACKH	Interrupt Acknowledge Asserted with Respect to CKO

Table 49. Timing Requirements and Characteristics for Interrupts and Reset
(see Figure 15, Figure 18, and Figure 19)

Abbreviated Reference	50 ns*		60 ns*		80 ns*		Unit
	Min	Max	Min	Max	Min	Max	
t77	4T + 6	—	4T + 8	—	4T + 10	—	ns
t78	—	2T	—	2T	—	2T	ns
t79	4T – 6	—	4T – 8	—	4T – 10	—	ns
t79a	0	4T – 10	0	4T – 10	0	4T – 10	ns
t79b	—	8T†	—	8T†	—	8T†	ns
t79c	—	10T	—	10T	—	10T	ns
t80	—	7	—	8	—	10	ns

* T = tCKILCKIL.
† ZN may be asserted at any time. This maximum specification permits correct DSP32C operation. Assertion of ZN for longer than 8T keeps all DSP32C outputs in a high-impedance state.

Timing Requirements and Characteristics (continued)

Bus Request Timing

Table 50. Definition of Timing Requirements and Characteristics for Bus Request
(See Figure 16 and Figure 17.)

Abbreviated Reference	*IEEE* Symbol	Parameter
t81	tBREQNLCKOL	BREQN Setup Time to CKO Low
t82	tCKOLCKOH	Synchronous Bus Request Interval
t83	tCKOHBRACKNL	BRACKN Delay After CKO High
t84	tBRACKNLABZ	BRACKN Asserted to EMI High Impedance
t85	tBREQNHCKOL	BREQN Setup Time to CKO Low
t86	tCKOLCKOH	Synchronous Bus Request Deassertion Interval
t87	tCKOHBRACKNH	BRACKN Delay After CKO High
t88	tBRACKNHABV	BRACKN Deasserted to EMI Signals Active
t89	tCKOLMGNL	MGN/EAPN Asserted After CKO Low
t90	tCKOLMGNH	MGN/EAPN Deasserted After CKO Low

Table 51. Timing Requirements and Characteristics for Bus Request
(See Figure 16 and Figure 17.)

Abbreviated	50 ns*		60 ns*		80 ns*		Unit
Reference	Min	Max	Min	Max	Min	Max	
t81	6	—	7	—	8	—	ns
t82	2.5T	3.5T + NT	2.5T	3.5T + NT	2.5T	3.5T + NT	ns
t83	—	6	—	7	—	8	ns
t84	—	0	—	0	—	0	ns
t85	6	—	7	—	8	—	ns
t86	1.5T	—	1.5T	—	1.5T	—	ns
t87	—	6	—	7	—	8	ns
t88	0	—	0	—	0	—	ns
t89	—	6	—	7	—	8	ns
t90	—	6	—	7	—	8	ns

* T = tCKILCKIL; N = number of wait-states in external memory transaction; NT is the product of N and T.

Timing Diagrams

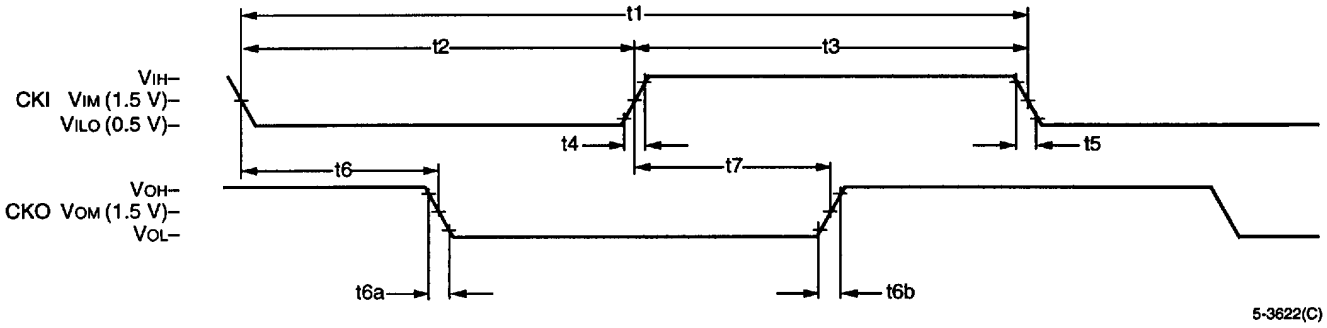
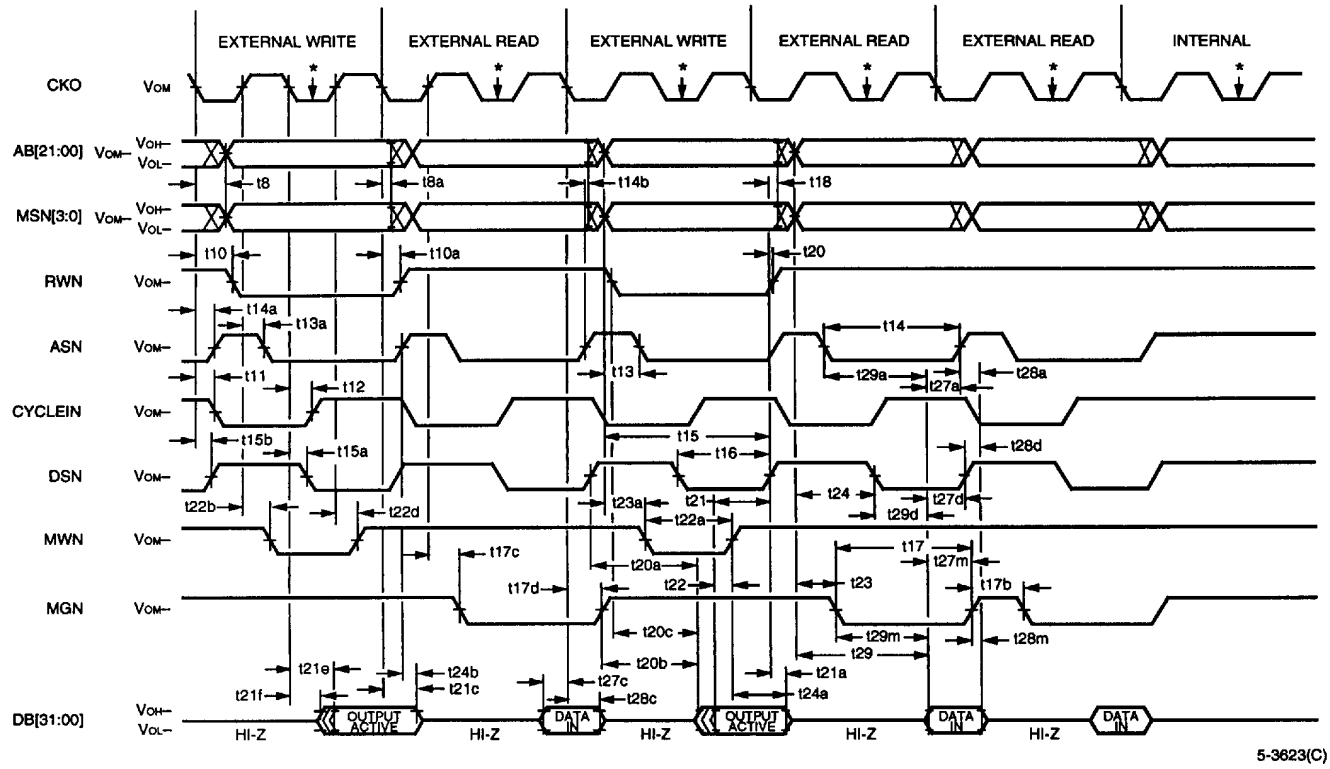


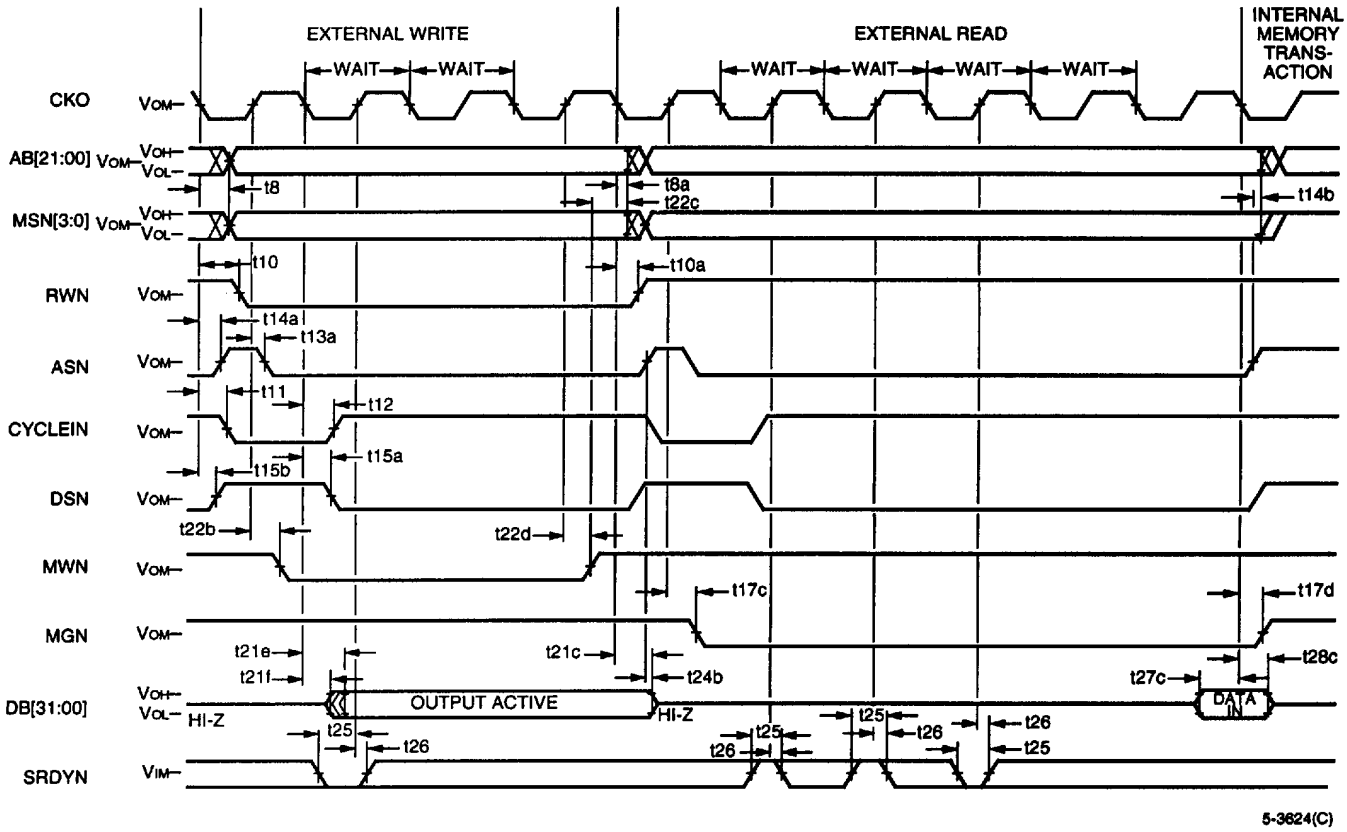
Figure 6. Clock In and Clock Out



* Additional clock periods are added here for memory waits.

Figure 7. External Memory Transactions (No Wait-States from External Memory)

Timing Diagrams (continued)



Note: SRDYN assertion is not necessary for wait-states programmed with **pcw**[MEMA]/**pcw**[MEMB] = 00, 01, or 10 and **pcw**[WA]/**pcw**[WB] = 1.

Figure 8. External Memory Transactions (Wait-States from External Memory)

Timing Diagrams (continued)

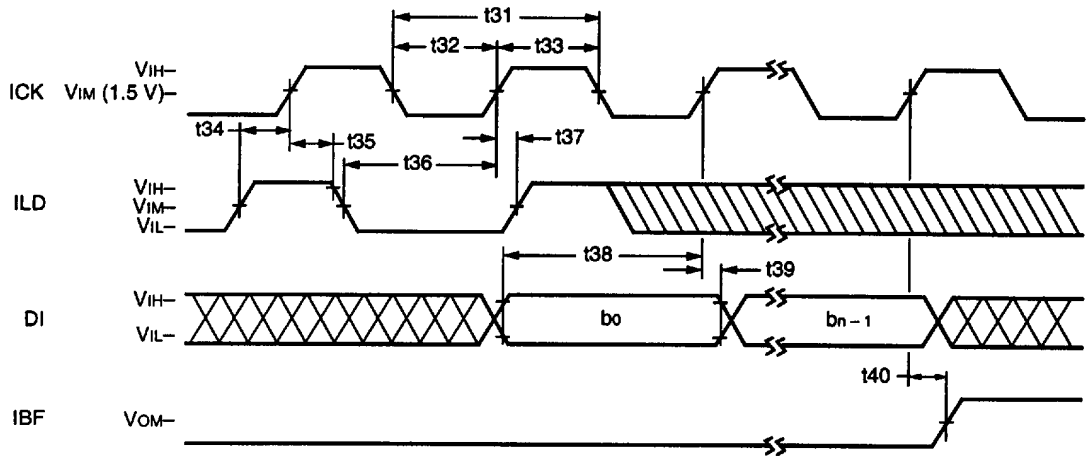


Figure 9. Serial Input Timing

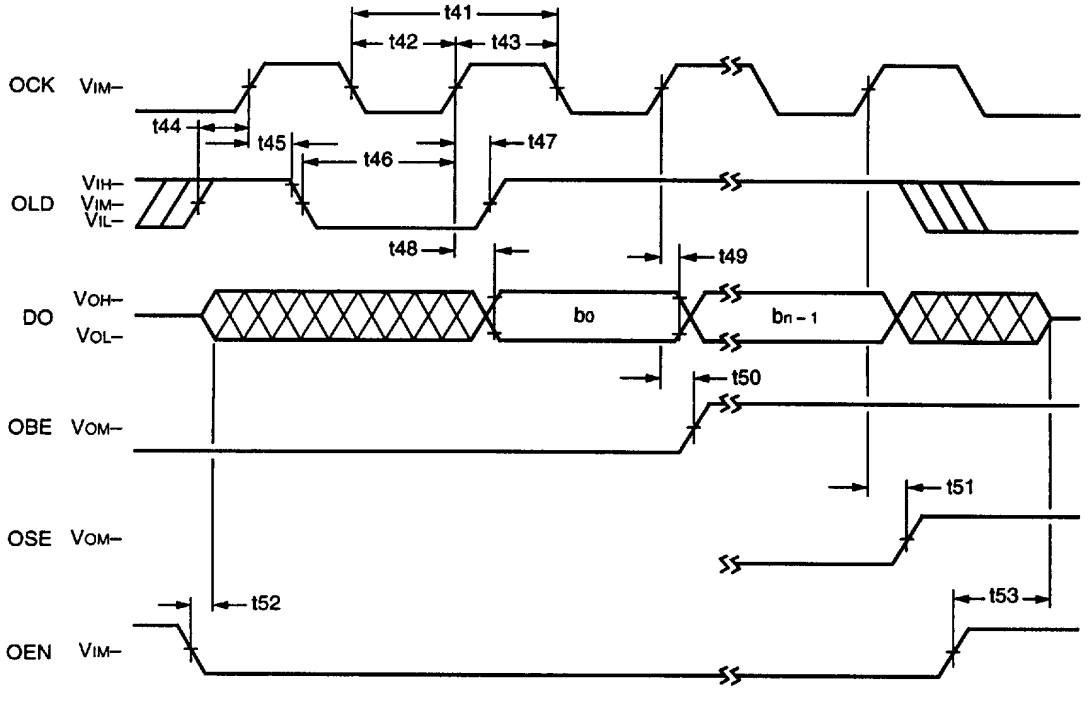
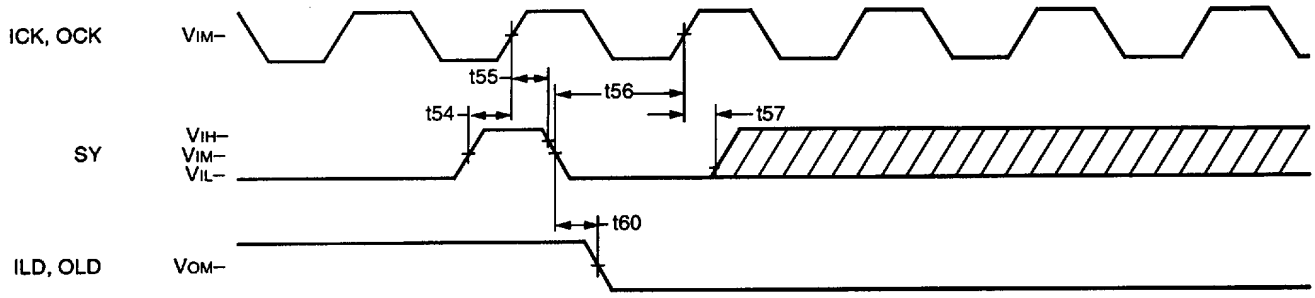
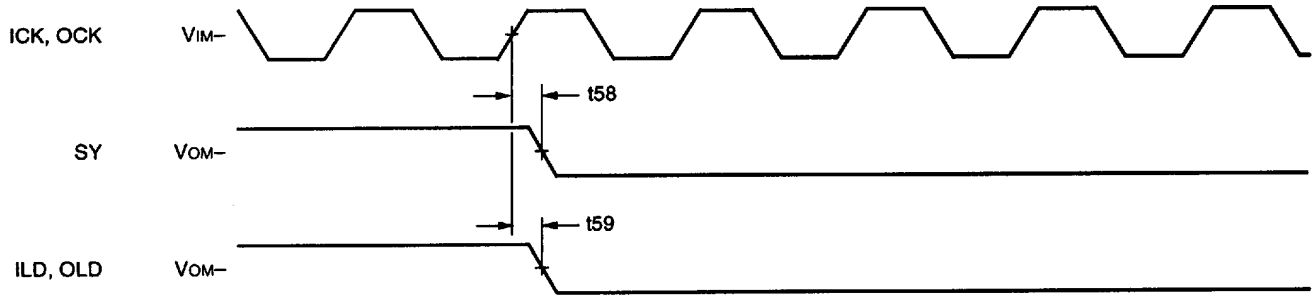


Figure 10. Serial Output Timing

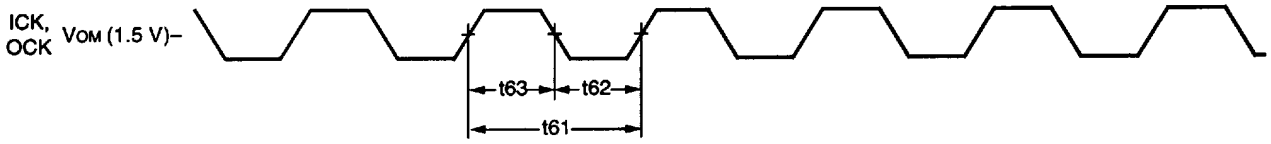
Timing Diagrams (continued)



A. External SY, ICK/OCK, Internal ILD/OLD



B. Internal SY, ILD/OLD, External ICK/OCK



C. Internal ICK/OCK

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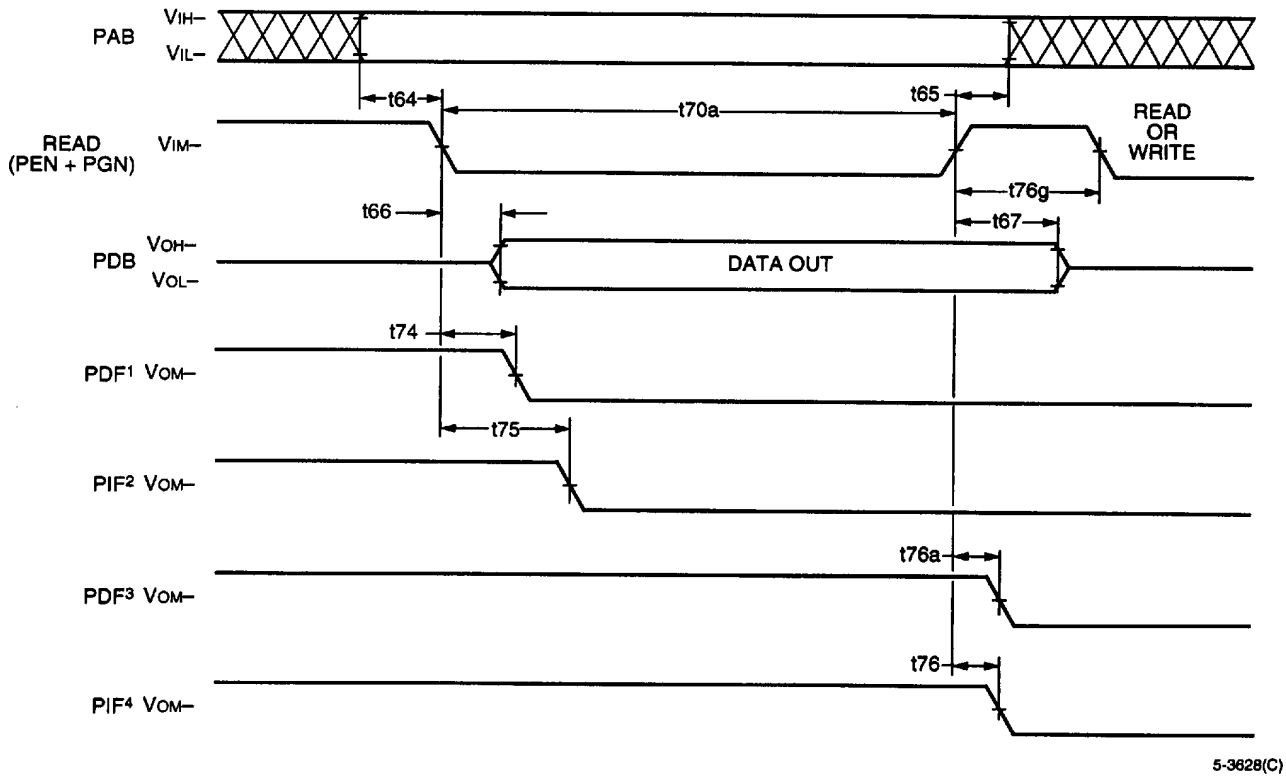
Figure 11. I/O Clock Generation Timing

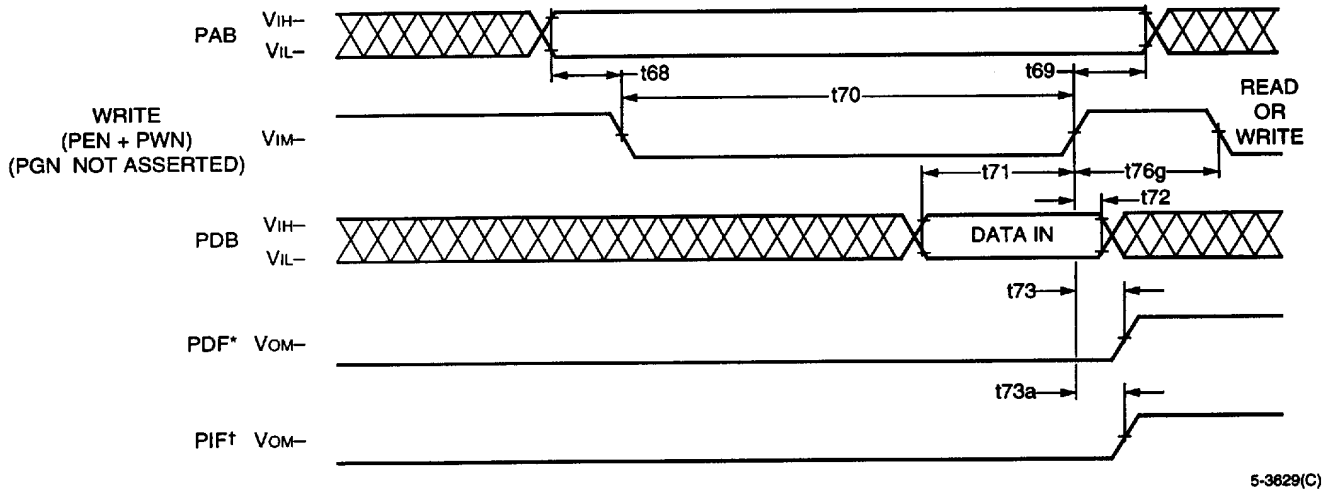
Timing Diagrams (continued)



1. PDF changes at the beginning of a read transaction when **pcr[10]** = 0. PDF changes only when **pdr**(h) (8-bit mode) or **pdr** (16-bit mode) is read. Reading **pdr**(l), **pdr2**(l), or **pdr2**(h) (8-bit mode), or reading **pdr2** (16-bit mode) does not affect the PDF flag.
2. PIF changes at the beginning of a read transaction if **pcr[10]** = 0. If PIF high was caused by the loading of the **pir** register, PIF changes when **pir**(h) (8-bit mode) is read, or **pir**(w) (16-bit mode) is read and **pcr[2]** (ENI) is set (1).
3. PDF changes at the end of a read transaction if **pcr[10]** = 1. (See Note 1 for a description of PDF logic.)
4. PIF changes at the end of a read transaction if **pcr[10]** = 1. (See Note 2 for a description of PIF logic.) PIF also changes when the **esr** register is read (if PIF high was caused by an unmasked error).

Figure 12. PIO Timing — Read Cycle

Timing Diagrams (continued)

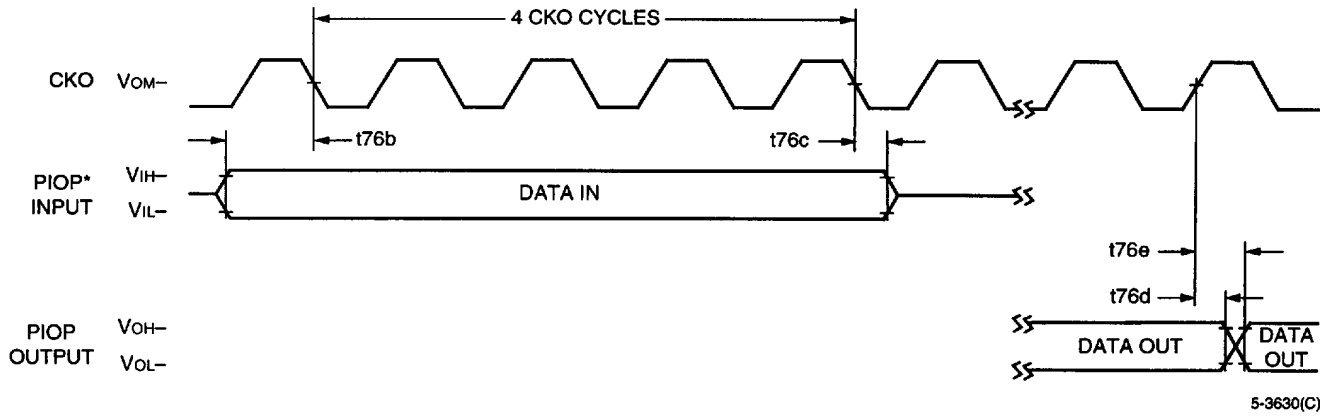


* PDF changes only when **pdr**(h) (8-bit mode) or **pdr** (16-bit mode) is written. Writing **pdr**(l), **pdr2**(l), **pdr2**(h) (8-bit mode), or writing **pdr2** (16-bit mode) does not affect the PDF flag.

† If **pcr[2]** (ENI) is set (1), PIF changes when **pir**(h) (8-bit mode) or **pir** (16-bit mode) is written.

Figure 13. PIO Timing — Write Cycle (PGN High)

Timing Diagrams (continued)



Note: The PIOP inputs are intended to sense slowly changing events. The DSP32C samples PIOP inputs once every four cycles of CKO; the value of PIOP read reflects the PIOP when sampled by a DSP32C instruction that reads the PIOP register.

Figure 14. PIOP Timing

8-Bit PIO

When the DSP32C PIO is configured as an 8-bit port, the upper 8 bits of PDB can be configured by **pcw[7—6]** to be two 4-bit input or output registers. The upper 8 bits of PDB are referred to as PIOP0—PIOP7.

When either PIOP0—PIOP3 or PIOP4—PIOP7 is configured as an input, the PIOP register can be read by the DSP32C, at most, once every four cycles of CKO.

When either PIOP0—PIOP3 or PIOP4—PIOP7 is configured as an output, the corresponding bits of PDB change only when the DSP32C program writes a different value to the corresponding bit in PIOP, or if **pcw[6]** (PIOPL) or **pcw[7]** (PIOPH) is cleared. This may occur, at most, once every four cycles of CKO. (When **pcw[6]** or **pcw[7]** is cleared, the corresponding bits of PDB become inputs, but the contents of the PIOP registers remain unchanged.)

Timing Diagrams (continued)

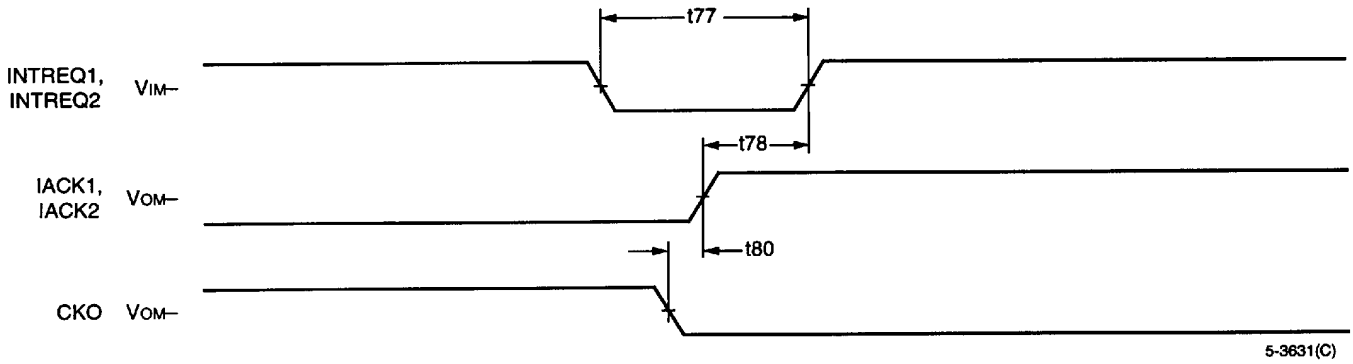


Figure 15. Interrupt Timing

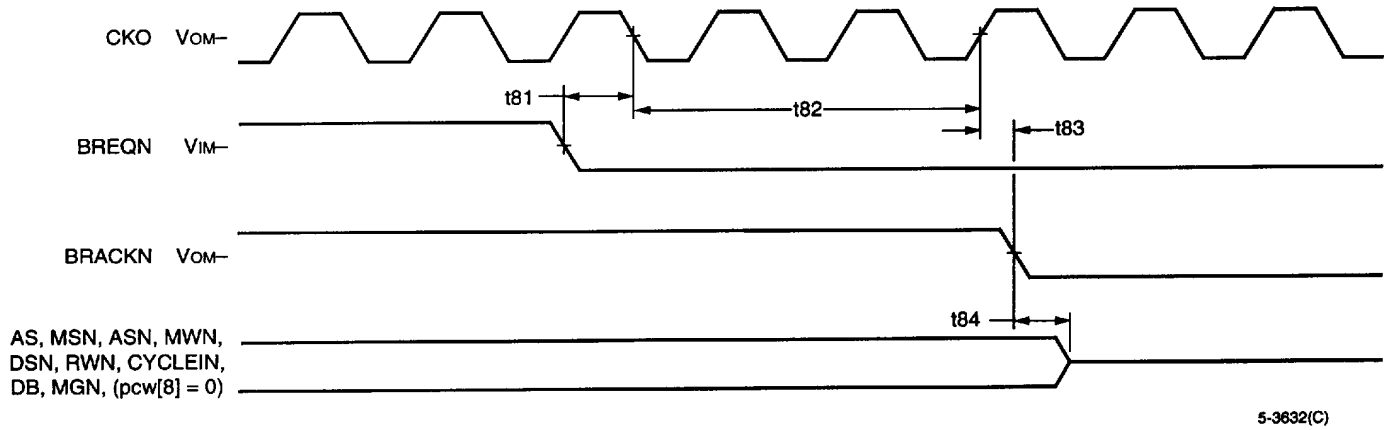


Figure 16. Bus Request Assertion Timing

Timing Diagrams (continued)

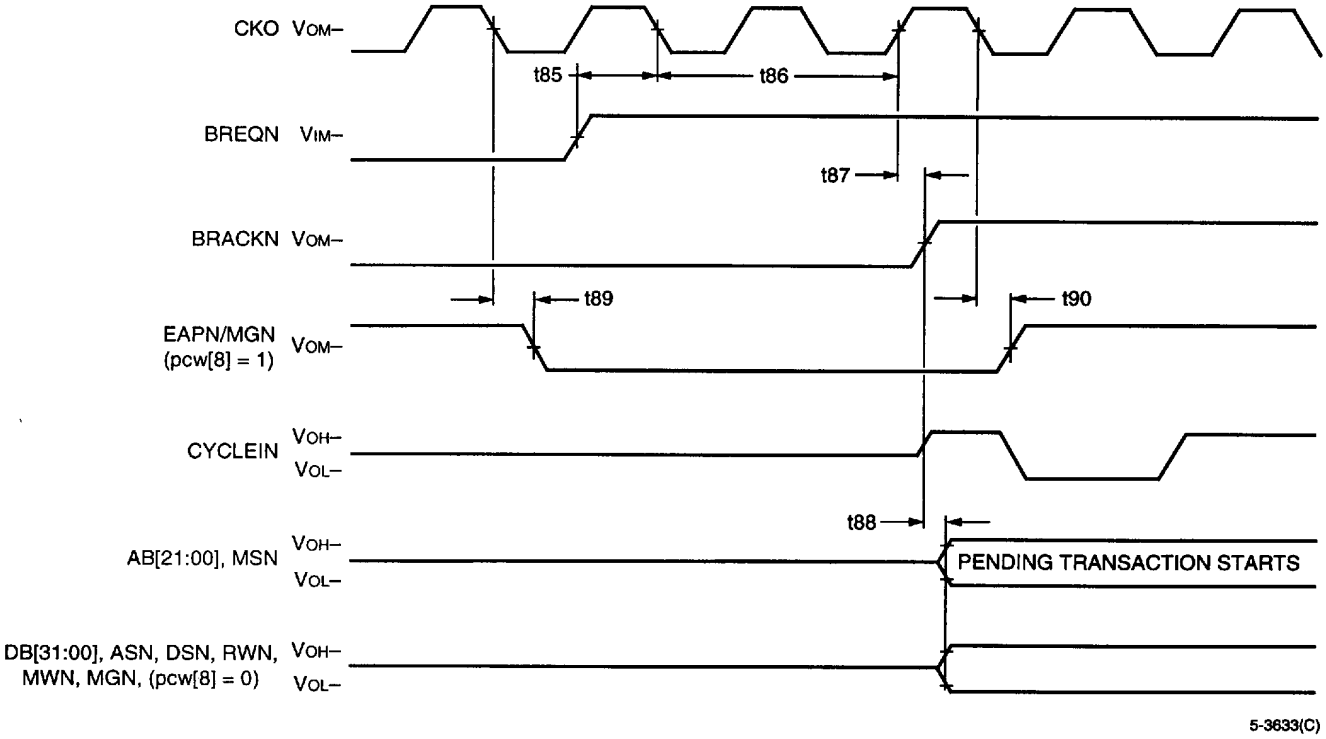


Figure 17. Bus Request Deassertion Timing

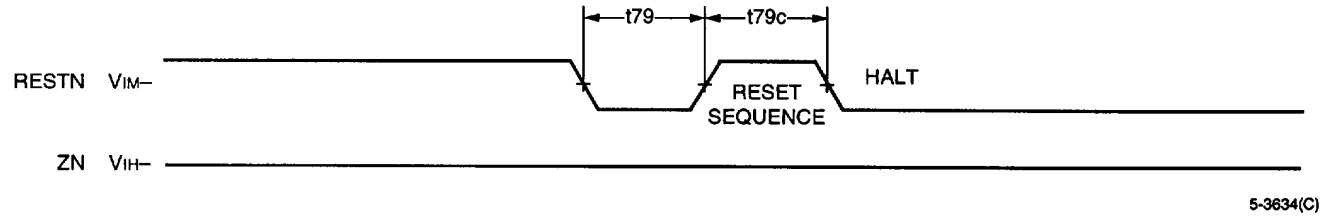


Figure 18. Reset and Enter Halt

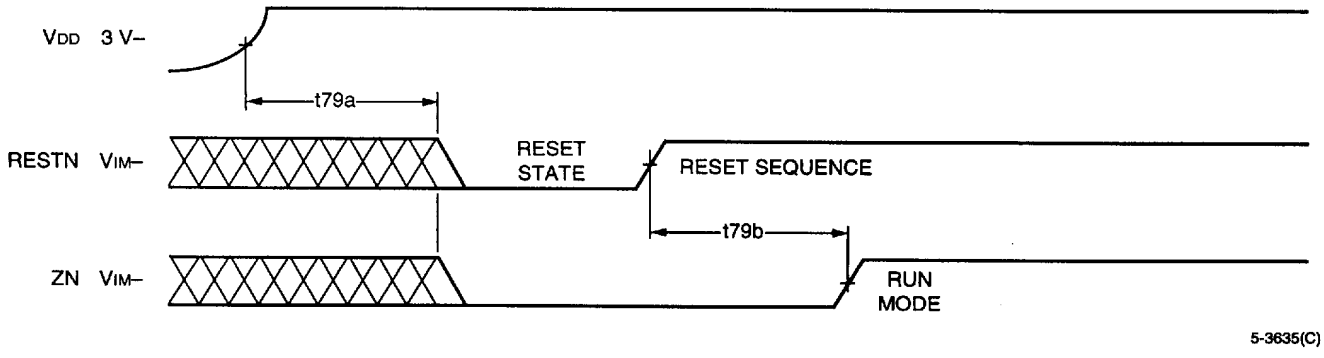
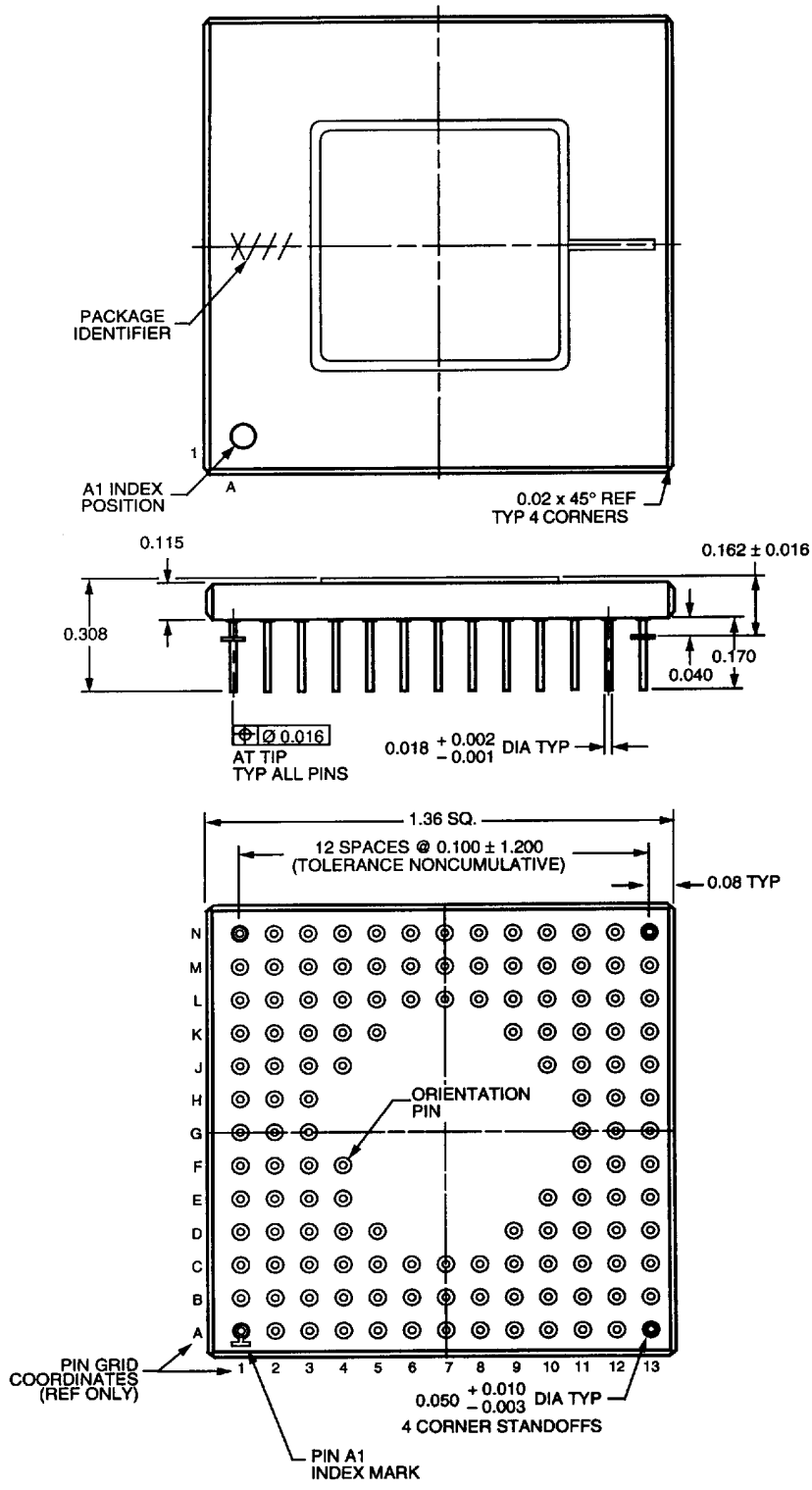


Figure 19. Power-On Reset Requirements

Outline Diagrams

133-Pin CPGA Package (all dimensions are in inches)



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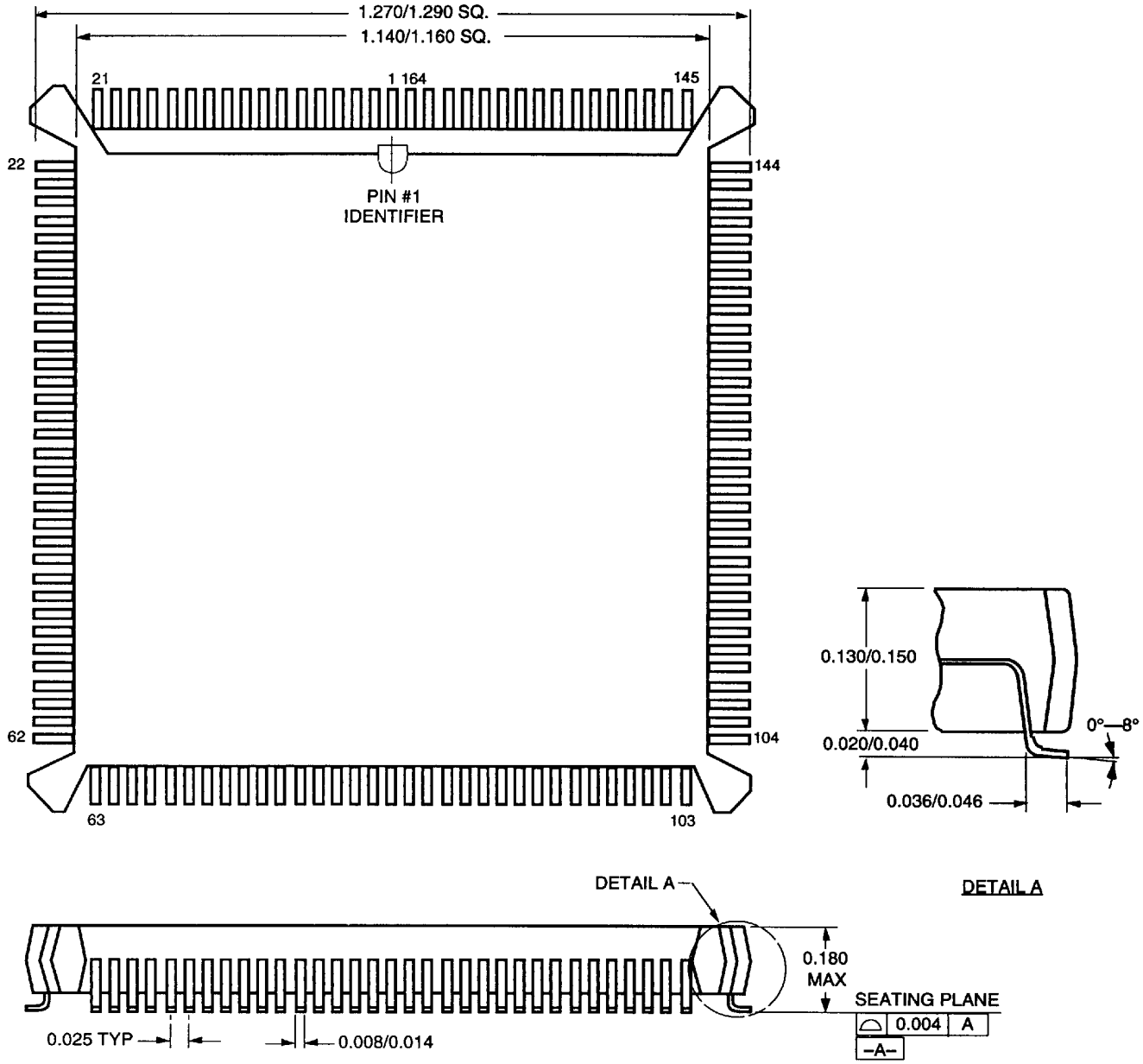
Outlines Diagrams (continued)

164-Pin BQFP Package (all dimensions are in inches)



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