MPEG Playback Clock Generator

Features

- Generates preset MPU and AUDIOCLK frequencies, 3 fixed-frequency clocks, and buffers the input reference frequency
- Supports all frequency requirements for MPEG playback
- Supports both NTSC and PAL crystal frequencies (14.31818 and 17.734476 MHz, respectively)
- Tristate buffer with output enable
- External loop filter for MPU clocks provides smooth, glitch-free frequency transitions
- Low, short-term and long-term jitter
- CMOS technology in 24-pin SOIC
- 5V or 3.3V supply

Description

CH9081 is a triple PLL clock generator designed for high performance video applications. By generating all essential clock signals for MPEG playback, the need for multiple oscillators is eliminated.

CH9081 generates a variety of MPU and 2XMPU clock outputs from a preset ROM table primarily for the use of controllers. The MPU/2XMPU output frequencies can be selected by the frequency select inputs, MPUSEL[2:0].

CH9081 generates three fixed-frequency clocks (40.5 MHz, 27 MHz, and 13.5 MHz) to support video applications.

CH9081's audio clock output (AUDIOCLK) supports all audio frequencies for MPEG and CD requirements. AUDIOCLK frequencies can be selected by the frequency select inputs, AUDIOSEL[1:0].

CH9081 uses either NTSC or PAL crystals in generating the input reference frequency. The NTSC/PAL* pin is used to indicate which crystal is used. When this pin is high (NTSC) a 14.31818 MHz cystal is assumed; when this pin is low (PAL) a 17.734476 MHz cystal is assumed. The input reference frequency and its divide-by-four version are available as buffered outputs.

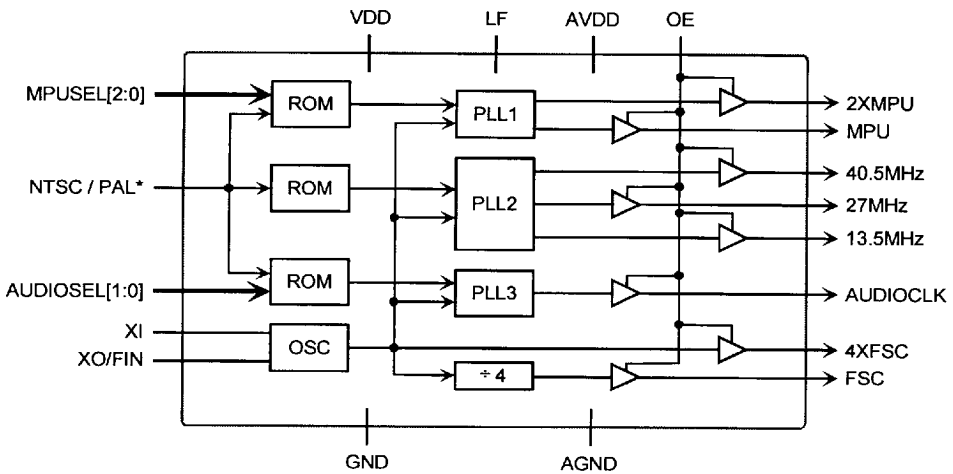

Figure 1: Block Diagram

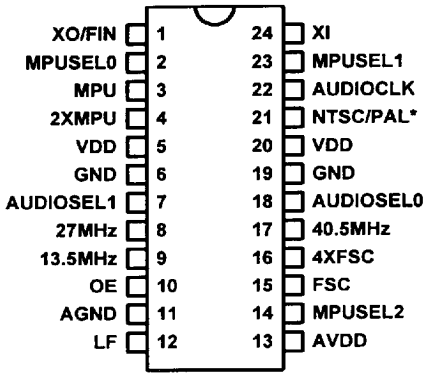

Figure 2: CH9081A

Table 1 • Pin Description CH9081A

Pin	Type	Symbol	Description
1	Out / In	XO / FIN	Crystal output or external FREF input
2, 14, 23	In	MPUSEL0, MPUSEL2, MPUSEL1	MPU clock select inputs
3	Out	MPU	MPU clock output
4	Out	2XMPU	2XMPU clock output
5, 20	Power	VDD	5V or 3.3V supply
6, 19	Power	GND	Ground
7, 18	In	AUDIOSEL[1:0]	Audio clock frequency select inputs
8	Out	27 MHz	27 MHz clock output
9	Out	13.5 MHz	13.5 MHz clock output
10	In	OE	Output enable (active high, internal pull-up)
11	Power	AGND	Analog ground
12	Out	LF	External loop filter
13	Power	AVDD	Analog 5V supply
15	Out	FSC	FSC (sub-carrier frequency) clock output FSC is ¼ of the crystal frequency
16	Out	4XFSC	4XFSC clock output 4XFSC is equal to the crystal frequency
17	Out	40.5 MHz	40.5 MHz clock output
21	In	NTSC / PAL*	Crystal frequency select input
22	Out	AUDIOCLK	Audio clock output
24	In	XI	Crystal input

Table 2 • FSC Clock Output Frequencies (in MHz)

NTSC / PAL*	Crystal Frequency	4XFSC	FSC
0	17.734476	17.734476	4.433619
1	14.31818	14.31818	3.579545

Table 3 • Audio Clock Output Frequencies (in MHz)

AUDIOSEL1	AUDIOSEL0	AUDIOCLK
0	0	8.192
0	1	11.2896
1	0	12.288
1	1	16.9344

Note: If you plan to use a crystal frequency of 14.31818, you must set NTSC/PAL* = 1.
If you plan to use a crystal frequency of 17.734476, you must set NTSC/PAL* = 0.
The frequencies listed in the above table would be identical in either circumstance.

Table 4 • MPU Clock Output Frequencies (in MHz)

MPUSEL2	MPUSEL1	MPUSEL0	2XMPU	MPU
0	0	0	4.0	2.0
0	0	1	16.0	8.0
0	1	0	24.0	12.0
0	1	1	50.0	25.0
1	0	0	60.0	30.0
1	0	1	66.6	33.3
1	1	0	75.0	37.5
1	1	1	80.0	40.0

Note: If you plan to use a crystal frequency of 14.31818, you must set NTSC/PAL* = 1.
If you plan to use a crystal frequency of 17.734476, you must set NTSC/PAL* = 0.
The frequencies listed in the above table would be identical in either circumstance.

Table 5 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	–0.5 TO +7.0	V
VIN	Input voltage on any pin with respect to GND	–0.5 TO VDD+0.5	V
TSTOR	Storage temperature	–55 TO +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6 • DC Specifications (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 12mA	2.4			V
VOL	Output low voltage	VDD = 4.75V, IOL = 12mA			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current	Except AUDIOSEL[1:0] pins		5	20	µA
IPU	Input pull-up current, AUDIOSEL[1:0] pins			30	100	µA
ILK	Input leakage current		–10		10	µA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IDD	Operating current	VDD = 5V MPU = 40 MHz, No load MPU = 80 MHz, No load		25 30		mA

Table 7 • AC Specifications (Operating Conditions: TA = 0°C – 70°C, VDD = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	32	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	30 pF load, VOUT = 0.8V to 2.0V			2	ns
TF	Output clock fall time	30 pF load, VOUT = 0.8V to 2.0V			2	ns
TDC	Duty cycle		45	48/52	55	%
TJCC	Jitter, cycle to cycle	MPU = 50 MHz		TBD		ps
TFT	Frequency transition time	8 – 80 MHz		10		ms
TPU	Power up time	From OFF to 100 MHz		15		ms

Table 8 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 3.0V, IOH = 1.5mA	VDD – 0.5			V
VOL	Output low voltage	VDD = 3.0V, IOL = 3mA			0.5	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current	Except AUDIOSEL[1:0] pins		3		µA
IPU	Input pull-up current, AUDIOSEL[1:0] pins			15		µA
ILK	Input leakage current		–10		10	µA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IDD	Operating current	VDD = 3.3V MPU = 40 MHz, No load MPU = 80 MHz, No load		20 25		mA

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Table 9 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	20	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	30 pF load, VOUT = 0.8V to 2.0V			5	ns
TF	Output clock fall time	30 pF load, VOUT = 0.8V to 2.0V			5	ns
TDC	Duty cycle		45	48/52	55	%
TJCC	Jitter, cycle to cycle	MPU = 50 MHz		TBD		ps
TFT	Frequency transition time	8 – 80 MHz		10		ms
TPU	Power up time	From OFF to 100 MHz		15		ms

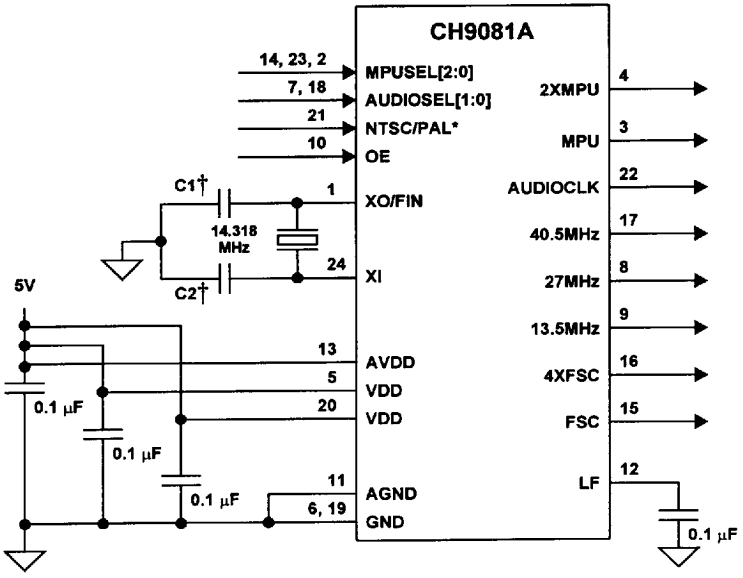

Figure 3: Application Schematic

Note: † The capacitance values depend on crystal manufacturer specifications

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9081A-S	300 mil SOIC	24	5V
CH9081A-S-L	300 mil SOIC	24	3.3V